INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS 4 x 4 MULTIPORT REGISTER,

WITH 3-STATE OUTPUTS,

BASED ON TYPE 40208B

ESCC Detail Specification No. 9301/009

ISSUE 1

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Pages 1 to 54

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space components
coordination group

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Issue 2	June 1993		
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Revision 'C'	April 2001		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all modifications defined in Revision 'A' to Issue 1 and the following DCR's:-		
		Cover Page	: Title amended	23396
		DCN		None
		Para. 1.1	: First sentence amended	23396
		Para. 1.10	: Last sentence rewritten to include ESD Class and Minimum Critical Path Failure Voltage	23385 22314
		Table 1(a)	: Table amended	22398
		Table 1(b)	: No. 9, package soldering temperatures changed	22314
			: Notes - Note 6 added	22314
		Figure 2(a)	: Table corrected	23247/23270
		Figure 2(b)	: "CKT A" deleted from Title	22398
		Figure 2(c)	: Figure deleted in total	22398
		Figure 2(d)	: Title amended to "2(c)"	22398
			: Table corrected	23247
		Notes to Figures	: In Title and Note 1, 2(d) amended to "2(c)"	22398
		Figure 3(a)	: On both packages, "3-State" amended to "ENABLE"	23396
			: On chip carrier package: Pins 12 and 13 designations reversed	23396
		Figure 3(b)	: Notation in Table and Note 1 standardised	23396
		Figure 3(c)	: Pin 11 corrected to read "R1B"	23396
			: Input Protection Network deleted	23396
		Para. 3	: New abbreviations added	23396
		Para. 4.2.2	: PIND Test and Condition added	22360
		Para. 4.5.2	: Third sentence amended to read "...2(c)"	22398
		Tables 2, 3(a), (b)	: Nos. 1 and 2, "dc" added after voltages	23396
			: Nos. 3 to 25, Test Figure amended to "4(a)"	23396
			: Nos. 26 to 39, All Other Inputs: V_{IN} amended to "15Vdc"	22814
			: Nos. 26 to 101, All Test Figures incremented by 1 letter	23396
			: Nos. 70 to 77, V_{IN} (Write Enable and Enable) corrected to "5Vdc"	23396
			: Nos. 86 to 93, All Other Inputs: V_{IN} corrected to "5Vdc"	23396
			: Nos. 94 to 101, V_{IN} (Write/Read) corrected to "0Vdc"	23396
			: Nos. 102 to 109, Test Figure amended to "4(h)"	23396
			: Nos. 102 to 109 and 110 to 117, Characteristics amended	23396
		Table 2	: Nos. 122 to 135, Limits column amended,	22398
			: Nos. 136 to 149, "Circuit A" deleted from first measurement and Circuit B entry deleted in total	22398
			: Nos. 149 to 162, corrected to "150 to 163"	23396
			: Nos. 163 to 171, all numbers incremented by 1	23396
			: Nos. 163 and 164, now Nos. 164 and 165, Characteristics amended	23396
			: Nos. 165 to 168, now Nos. 166 to 169, Test Figure amended to "4(o)"	23396
			: No. 166, now No. 167, V_{DD} corrected to "5Vdc"	23396
			: No. 171, now No. 172, "Note 7" added	22301
		Notes to Table 2	: Note 3 amended to read "...Table 4(a)"	23396
		Figure 4(a)	: Title amended	23396
		Figure 4(b)	: Figure deleted in total	23396

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	Item	Approved DCR No.
		Figures 4(c), (d), (e), (f), (g), (h)	: Renumbered as 4(b), (c), (d), (e), (f), (g)	23396
		Figure 4(c)	: Now 4(b), Figure amended	22814
		Figures 4(e),(f),(g),(h)	: Now Figures 4(d),(e),(f),(g), Input Conditions amended	23396
		Figures 4(g),(h)	: Now Figures 4(f), (g): Output circuit amended	23076
		Figures 4(h)	: New Figure added	23396
		Figure 4(i), (j)	: Input conditions specified	23396
		Figure 4(n)	: Timing Waveforms corrected	23162
		Figure 4(o)	: New Figure added	23396
		Table 4	: Nos. 102 to 109 and 110 to 117, Characteristics amended	23396
		Tables 5(a), (b)	: Titles amended	23162
		Table 5(c)	: Table added	22814
		Figures 5(a), (b)	: Titles amended	23162
		Figure 5(c)	: Figure added	22814
		Paras. 4.8.4 & 4.8.5	: Reference to Table and Figure amended to "5(c)"	23396
		Table 6	: Nos. 70 to 77, "N-Channel" added to Characteristics	23396
			: Nos. 102 to 109 and 110 to 117, Characteristics amended	23396
'A'	March'92	P1. Cover Page		None
		P2A. DCN		None
		P6. Table 1(a)	: Lead Material and/or Finish amended	23465
		P15. Para. 4.2.2	: Deviation deleted, "None" added	21048
		Para. 4.2.4	: Deviation deleted, "None" added	22919
		P16. Para. 4.2.5	: Deviation deleted, "None" added	22919
		Para. 4.4.2	: Material Type and Finishes amended	23465
'B'	Sept. '94	P1. Cover Page		None
		P2A. DCN		None
		P6. Table 1(a)	: Lead Material and/or Finish amended	221049
		P16. Para. 4.3.2	: Weights amended	23539
		Para. 4.4.2	: Lead Finish, Types amended	221049
'C'	Apr. '01	P1. Cover Page	: Page count increased by 1	221602
		P2A. DCN		None
		P4. T of C	: Appendices entry amended	221602
		P5. Para. 1.3	: New sentence added	221602
		P6. Table 1(a)	: Variants 08 and 09 added	221562
		Table 1(b)	: No. 8, Maximum temperature amended	221602
		P9. Figure 2(c)	: In the drawing, Pin No. 28 location corrected	221550
		P10. Notes to Figures	: Title amended	221562
			: Note 1 rewritten	221562
		P10A. Figure 2(d)	: New page added	221562
		P11. Figure 3(a)	: Left-hand drawing Title amended	221562
			: "SO" added to comparison Titles	221562
		P16. Para. 4.3.2	: SO package added to the text	221562
		Para. 4.4.2	: SO package added to the text	221562
		Para. 4.5.2	: SO package added to the text	221562
		P51. Para. 4.8.6	: Last sentence deleted, new text added	221602
		P54. Appendix 'A'	: Appendix added	221602

TABLE OF CONTENTS

Page

TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic CMOS 4 x 4 Multiport Register, having fully buffered 3-state outputs, based on Type 40208B. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the applicable ESA/SCC Generic Specification.

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling. These components are catagorised as Class 1 with a Minimum Critical Path Failure Voltage of 400Volts.

1.11 INPUT PROTECTION NETWORK

Double diode protection shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	FLAT	2(a)	G2 or G8
02	FLAT	2(a)	G4
03	D.I.L.	2(b)	G2 or G8
04	D.I.L.	2(b)	G4
07	CHIP CARRIER	2(c)	2
08	SO CERAMIC	2(d)	G2
09	SO CERAMIC	2(d)	G4

TABLE 1(b) - MAXIMUM RATINGS

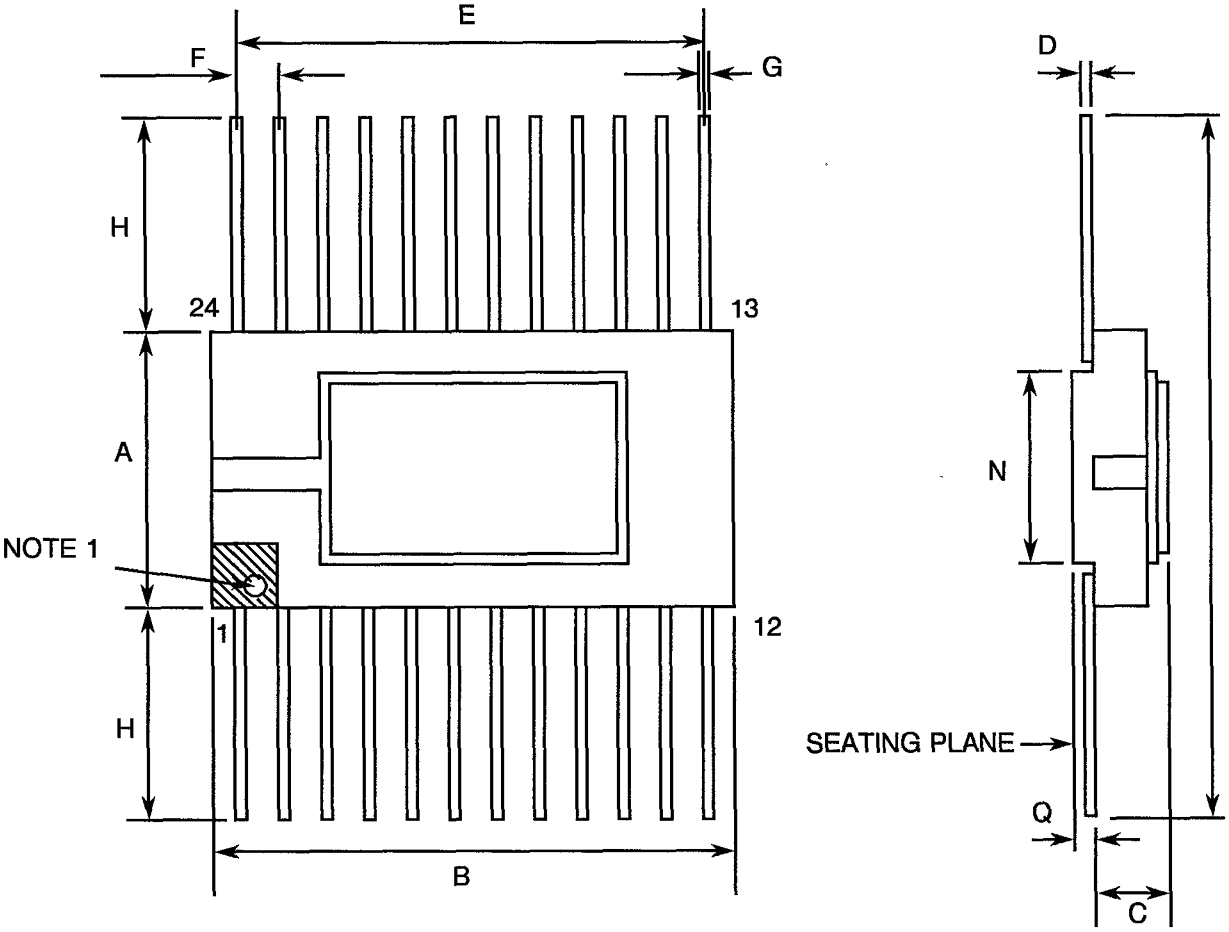
NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	-0.5 to +18	V	Note 1
2	Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.5	V	Note 2 Power on
3	D.C. Input Current	$\pm I_{IN}$	10	mA	-
4	D.C. Output Current	$\pm I_O$	10	mA	Note 3
5	Device Dissipation	P_D	200	mWdc	Per Package
6	Output Dissipation	P_{DSO}	100	mWdc	Note 4
7	Operating Temperature Range	T_{op}	-55 to +125	°C	-
8	Storage Temperature Range	T_{stg}	-65 to +150	°C	-
9	Soldering Temperature	T_{sol}		°C	
	For FP and DIP		+300		Note 5
	For CCP		+245		Note 6

NOTES

1. Device is functional from +3V to +15V with reference to V_{SS}.
2. V_{DD} +0.5V should not exceed +18V.
3. The maximum output current of any single output.
4. The maximum power dissipation of any single output.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
6. Duration 30 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 24-PIN

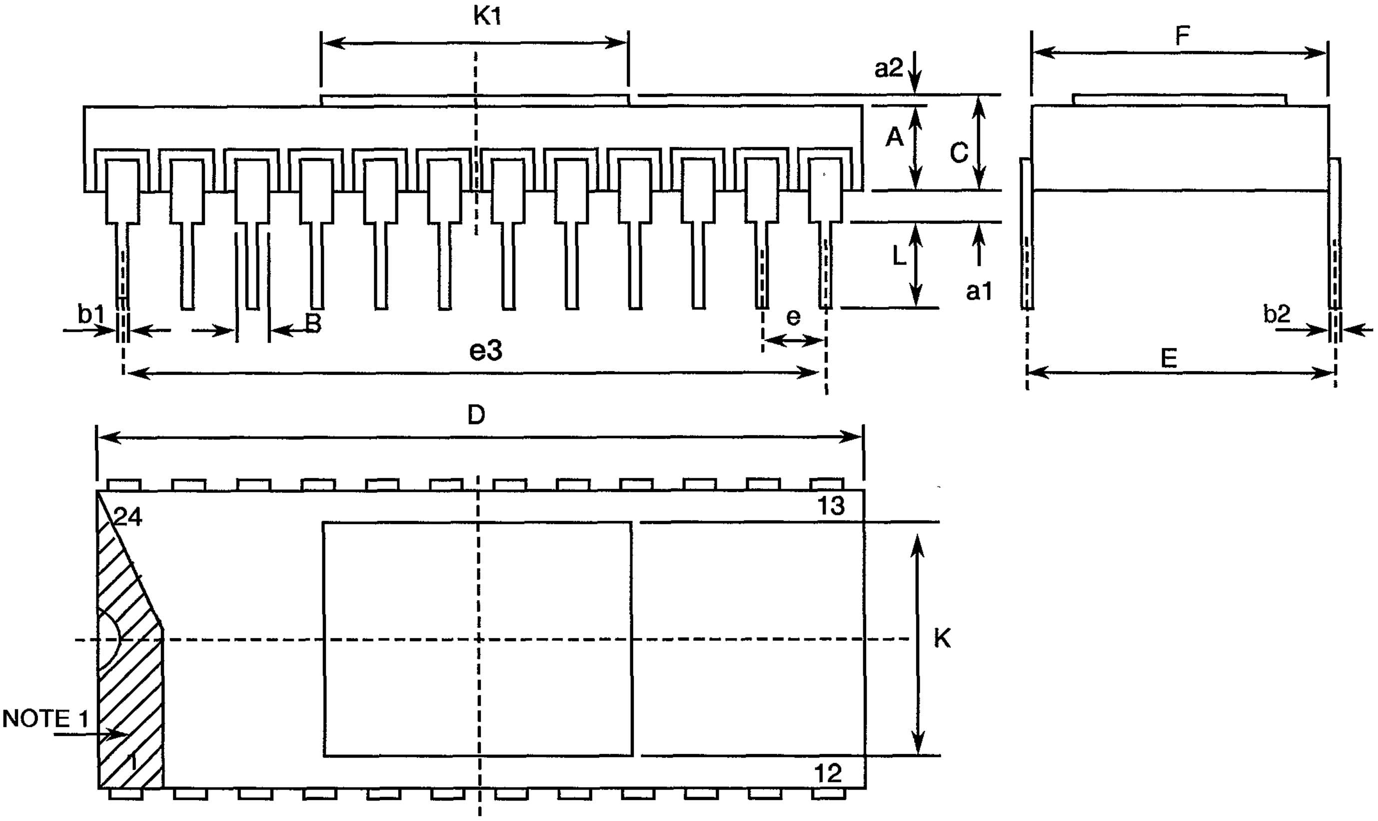


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	10.70	11.30	
B	15.30	15.70	
C	1.45	1.90	
D	0.23	0.30	
E	13.84	14.10	
F	1.22	1.32	4
G	0.45	0.55	3
H	7.25	8.25	
L	25.00	28.00	
N	7.00	TYPICAL	
Q	0.45	0.55	2

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 24-PIN

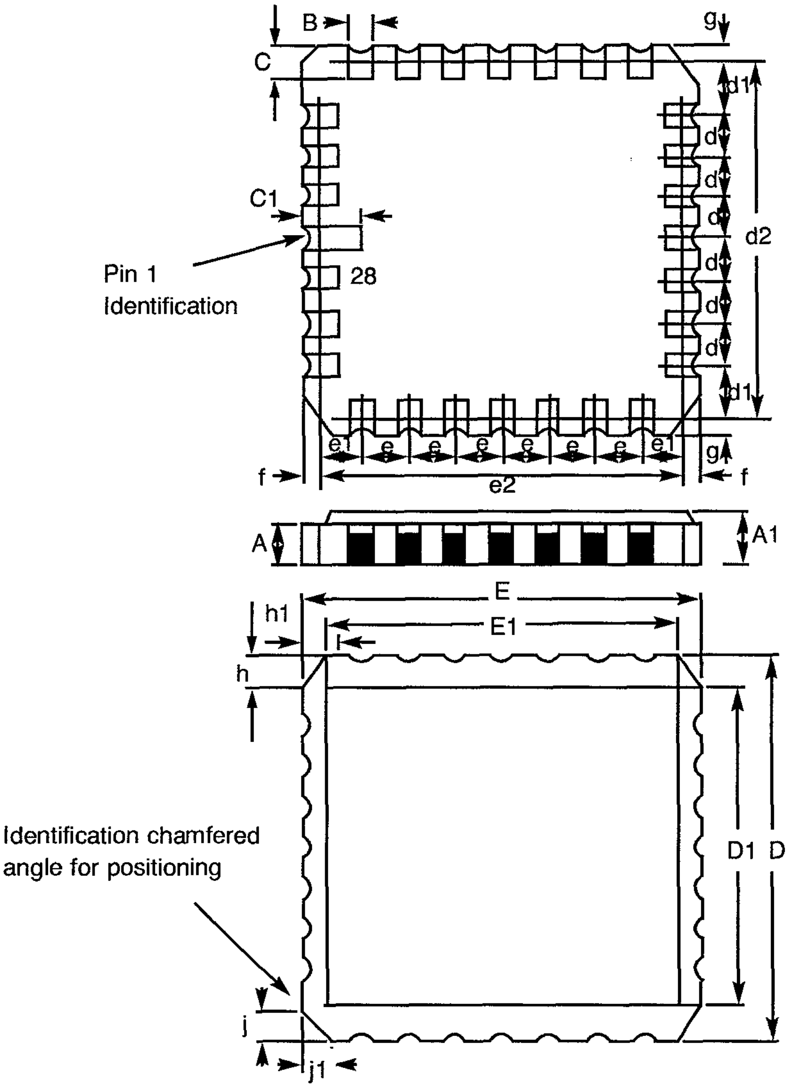


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.931	2.387	
a_1	1.016	1.525	2
a_2	0.274	0.340	
B	1.274	TYPICAL	3
b_1	0.407	0.507	3
b_2	0.229	0.304	3
C	2.205	2.727	
D	30.176	30.784	
E	14.986	15.494	
e	2.413	2.667	4
e_3	27.813	28.067	
F	14.859	15.367	
L	3.000	3.800	
K	12.600	13.000	
k_1	12.600	13.000	

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - CHIP CARRIER - 28-TERMINAL



DIMENSIONS	MILLIMETRES		NOTES
	MIN	MAX	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	3
C	1.06	1.47	3
C_1	1.91	2.41	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27	TYPICAL	4
d2	7.62	TYPICAL	
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27	TYPICAL	4
e2	7.62	TYPICAL	
f, g	-	0.76	
h, h1	1.01	TYPICAL	6
j, j1	0.51	TYPICAL	5

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(d) INCLUSIVE

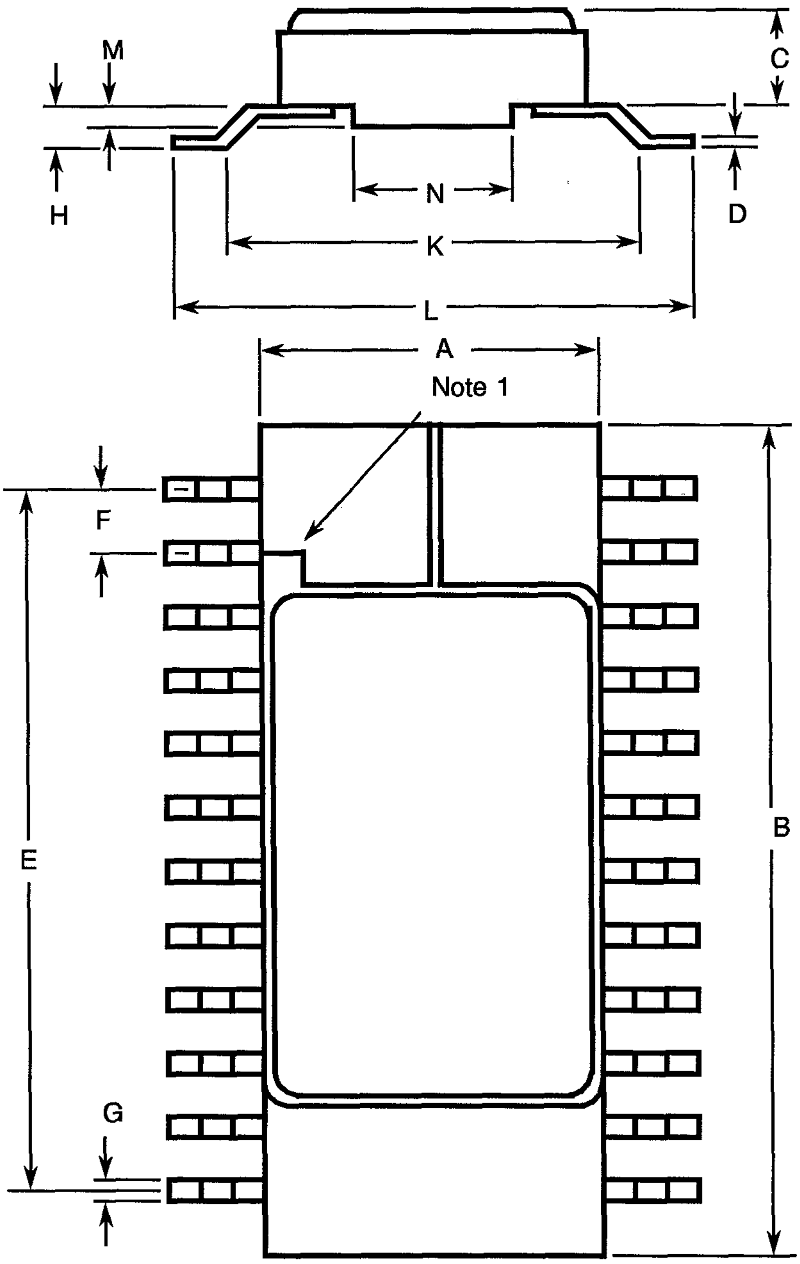
1. Index area; a notch, letter, metallised tab or dot shall be located adjacent to Pin 1 or 2 and shall be within the shaded area shown.

   For chip carrier packages the index shall be as defined in Figure 2(c).

   For SO packages, a dot shall also be located adjacent to Pin 1 on the bottom of the package.
2. The dimension shall be measured from the seating plane to the base plane.
3. All leads or terminals.
4. 24 pin packages : 22 spaces
   28 terminal packages : 16 spaces
5. Index corner only.
6. Three non-index corners.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - SMALL OUTLINE CERAMIC PACKAGE, 24-PIN



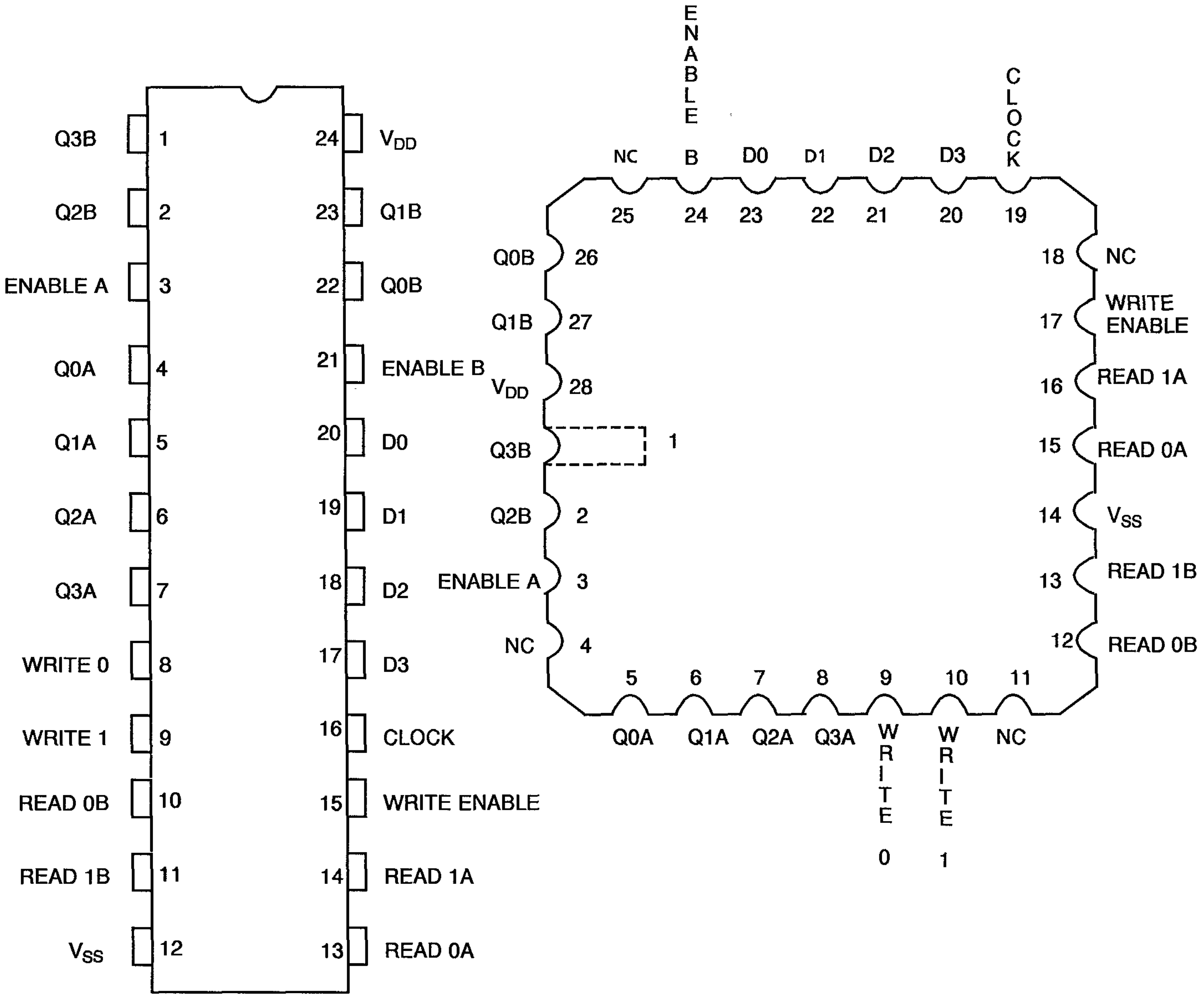
SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	7.30	7.60	
B	15.20	15.60	
C	1.58	1.88	
D	0.17	0.23	3
E	13.82	14.12	
F	1.27 TYPICAL		4
G	0.37	0.47	3
H	0.60	0.90	3
K	9.00 TYPICAL		
L	10	10.65	
M	0.55 TYPICAL		
N	4.31 TYPICAL		

NOTES: See Page 10.

FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE, SO AND FLAT PACKAGES

CHIP CARRIER PACKAGE



TOP VIEW

TOP VIEW

FLAT PACKAGE, SO AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE, SO AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12
CHIP CARRIER PIN OUTS	1	2	3	5	6	7	8	9	10	12	13	14
FLAT PACKAGE, SO AND DUAL-IN-LINE PIN OUTS	13	14	15	16	17	18	19	20	21	22	23	24
CHIP CARRIER PIN OUTS	15	16	17	19	20	21	22	23	24	26	27	28

FIGURE 3(b) - TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	D_n	Q_{nA}	Q_{nB}
	H	S1	S2	S1	S2	S1	S2	H	H	H	H	H
	H	S1	S2	S1	S2	S1	S2	H	H	L	L	L
X	X	X	X	X	X	X	X	L	L	X	Z	Z
	H	L	L	L	H	H	L	H	H	D_n to Word 0	Word 1 out	Word 2 out
	L	L	L	L	H	H	L	H	H	Word 0 not Altered	Word 1 out	Word 2 out
X	X	X	X	H	L	L	H	H	H	X	Word 2 out	Word 1 out
	X	X	X	X	X	X	X	H	H	X	NC	NC

NOTES

1. Logic Level Definitions: L = Low Level, H = High Level, X = Don't Care, Z = High Impedance
2. S1 and S2 refer to input states of either H or L.

FIGURE 3(c) - CIRCUIT SCHEMATIC

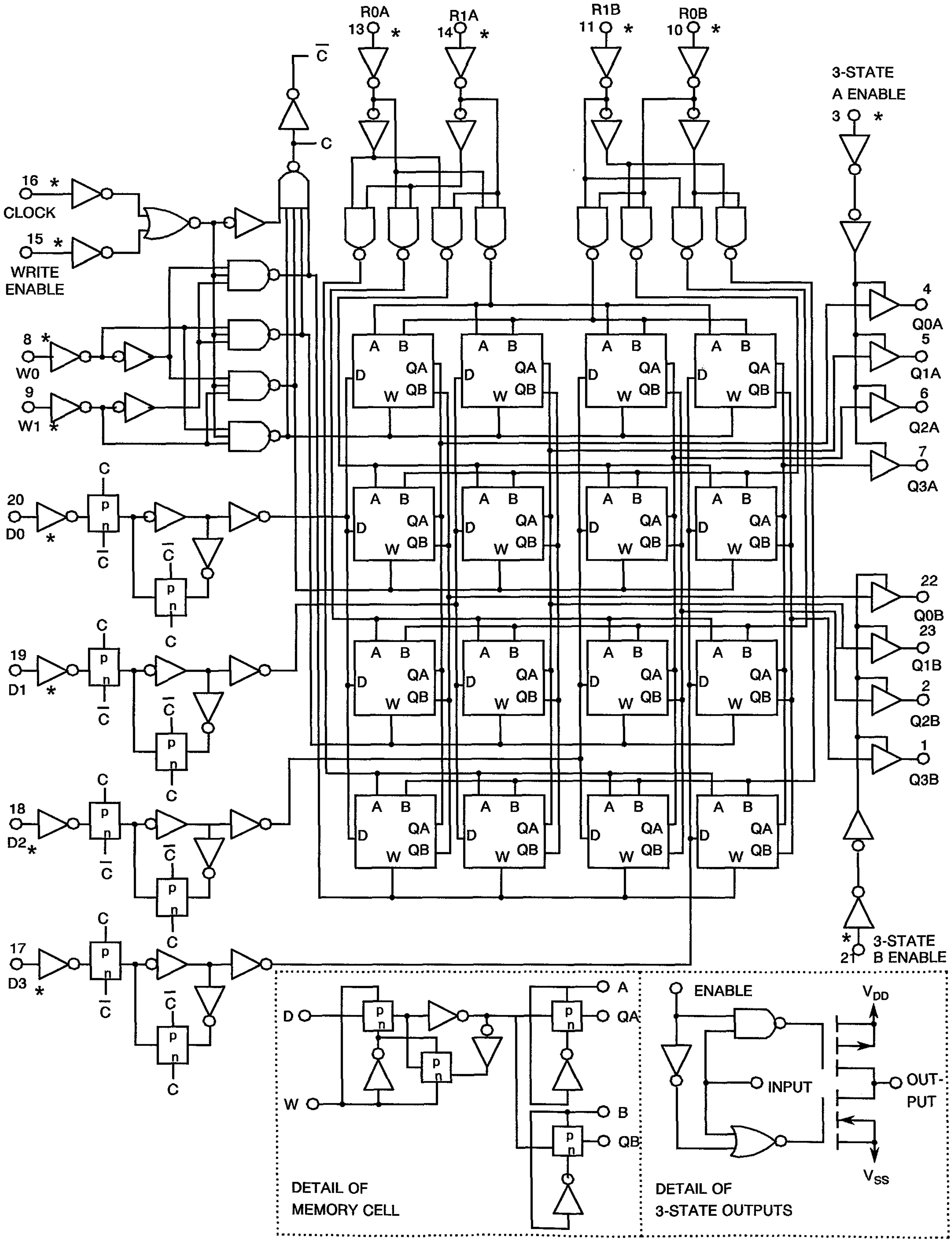


FIGURE 3(d) - FUNCTIONAL DIAGRAM

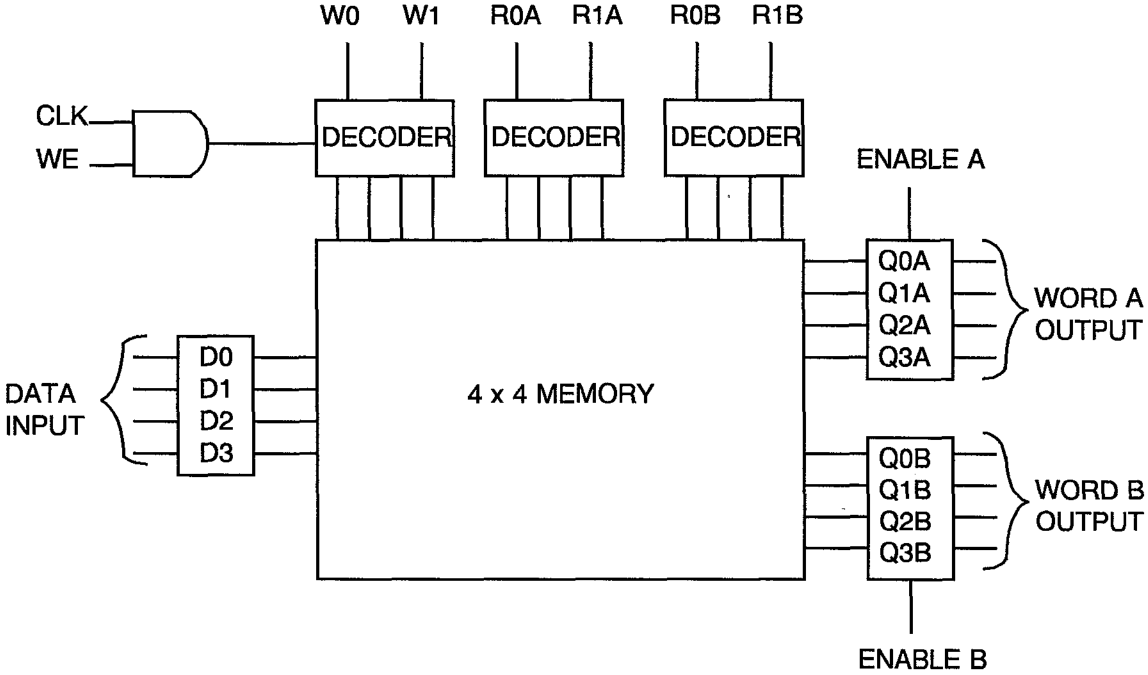
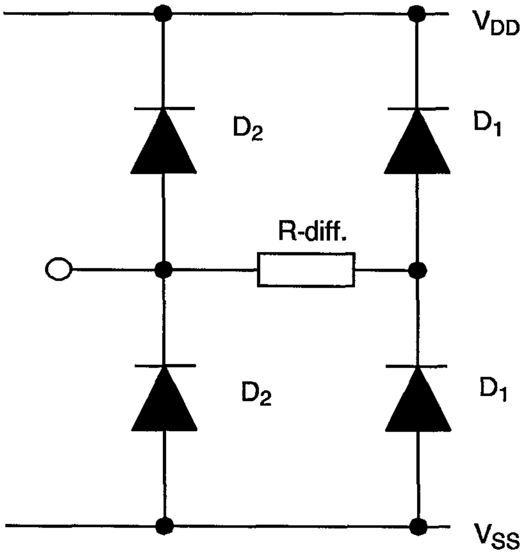


FIGURE 3(e) - INPUT PROTECTION NETWORK



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC} = Input Clamp Voltage
P_{DSO} = Single Output Power Dissipation
CKT = Circuit
I_{OZ} = Output Leakage Current Third State
t_{PHZ} = Propagation Delay, High Output to High Impedance
t_{PZH} = Propagation Delay, High Impedance to High Output
t_{PLZ} = Propagation Delay, Low Output to High Impedance
t_{PZL} = Propagation Delay, High Impedance to Low Output

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalant to the ESA/SCC requirement and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

4.2.3.1 Deviations from High Temperature Reverse Bias (H.T.R.B.)

Prior to operating power burn-in, a high temperature reverse bias (H.T.R.B.) screen at +125°C shall be added for the N-Channel and then for the P-Channel in accordance with Tables 5(a) and 5(b) of this specification. Each exposure to H.T.R.B. shall be 72 hours and Table 4 Parameter Drift Values shall be applied at 0 and 144 hours.

4.2.4 Deviations from Qualification, Environmental and Endurance Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 4.25 grammes for the dual-in-line package, 1.55 grammes for the flat package, 1.1 grammes for the SO package and 0.79 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed or preform-soldered.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with either Type '4' or Type '2 or 8' finish in accordance with ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' in accordance with ESA/SCC Basic Specification No. 23500. For SO ceramic packages, the material shall be Type 'G' with either Type '2' or Type '4' finish in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line, flat and SO packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

930100901B

Detail Specification Number — 9301009
Type Variant, as applicable — 01
Testing Level (B or C, as appropriate) — B

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_{amb} = +22±3 °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at T_{amb} = +125(+0-5) °C and -55(+5-0) °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at +22±3 °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. and Burn-in

The requirements for H.T.R.B. and Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and Burn-in shall be as specified in Tables 5(a), 5(b) and 5(c) of this specification.

4.7.3 Electrical Circuits for H.T.R.B and Burn-in

Circuits for use in performing the H.T.R.B. and Burn-in tests are shown in Figures 5(a), 5(b) and 5(c) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
3 to 25	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 3 (Pin D/F 24) (Pin C 28)	-	1.0	µA
26 to 39	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0Vdc All Other Inputs: V_{IN} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	-50	nA
40 to 53	Input Current High Level	I_{IH}	3010	4(c)	V_{IN} (Under Test) = 15Vdc All Other Inputs: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	50	nA
54 to 61	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IN} (Write Enable & Enable) = 15Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	0.05	V

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
62 to 69	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 15Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	14.95	-	V
70 to 77	Output Drive Current N-Channel	I_{OL1}	-	4(f)	V_{IN} (Write Enable & Enable) = 5Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 0.4Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	0.51	-	mA
78 to 85	Output Drive Current N-Channel	I_{OL2}	-	4(f)	V_{IN} (Write Enable & Enable) = 15Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 1.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	3.4	-	mA
86 to 93	Output Drive Current P-Channel	I_{OH1}	-	4(g)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 5Vdc V_{OUT} = 4.6Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-0.51	-	mA

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
94 to 101	Output Drive Current P-Channel	I_{OH2}	-	4(g)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 15Vdc V_{OUT} = 13.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-3.4	-	mA
102 to 109	Output Leakage Current Third State (1)	I_{OZ1}	-	4(h)	V_{IN} (Enable) = 0Vdc All Other Inputs: V_{IN} = 15Vdc V_{OUT} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	0.4	µA
110 to 117	Output Leakage Current Third State (2)	I_{OZ2}	-	4(h)	V_{IN} (Enable) = 0Vdc All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	-0.4	µA
118	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	-	4(a)	V_{IL} = 1.5Vdc V_{IH} = 3.5Vdc V_{DD} = 5 Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}	-			-	0.5	

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
119	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL2}	-	4(a)	V_{IL} = 4Vdc V_{IH} = 11Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH2}	-			-	1.5	
120	Threshold Voltage N-Channel	V_{THN}	-	4(i)	Clock Input at Ground All Other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10μA (Pin D/F 12) (Pin C 14)	-0.7	-3.0	V
121	Threshold Voltage P-Channel	V_{THP}	-	4(j)	Clock Input at Ground All Other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10μA (Pin D/F 24) (Pin C 28)	0.7	3.0	V
122 to 135	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(k)	I_{IN} (Under Test) = -100μA V_{DD} = Open, V_{SS} = 0Vdc All Other Pins Open (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	-2.0	V
136 to 149	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(l)	V_{IN} (Under Test) = 6Vdc V_{SS} = Open, R = 30kΩ; (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	3.0	-	V

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
150 to 163	Input Capacitance	C_{IN}	3012	4(m)	V_{IN}(Not under Test) = 0Vdc V_{DD} = V_{SS} = 0Vdc Note 6 (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	7.5	pF
164	Propagation Delay Low to High (Clock to Output)	t_{PLH}	3003	4(n)	V_{IN} (Under Test) = Pulse Generator V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Notes 7 and 8 Pins D/F Pins C 16 to 1 19 to 1	-	670	ns
165	Propagation Delay High to Low (Clock to Output)	t_{PHL}	3003	4(n)	V_{IN} (Under Test) = Pulse Generator V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Notes 7 and 8 Pins D/F Pins C 16 to 1 19 to 1	-	670	ns
166	Propagation Delay High Impedance to Low Output	t_{PZL}	3003	4(o)	V_{IN} (Under Test) = Pulse Generator V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Notes 7 and 8 Pins D/F Pins C 21 to 2 24 to 2	-	210	ns
167	Propagation Delay Low Output to High Impedance	t_{PLZ}	3003	4(o)	V_{IN} (Under Test) = Pulse Generator V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Notes 7 and 8 Pins D/F Pins C 21 to 2 24 to 2	-	210	ns
168	Propagation Delay High Impedance to High Output	t_{PZH}	3003	4(o)	V_{IN} (Under Test) = Pulse Generator V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Notes 7 and 8 Pins D/F Pins C 21 to 2 24 to 2	-	150	ns

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
169	Propagation Delay High Output to High Impedance	t_{PHZ}	3003	4(o)	V_{IN} (Under Test) = Pulse Generator V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Notes 7 and 8 Pins D/F Pins C 21 to 2 24 to 2	-	150	ns
170	Transition Time Low to High	t_{TLH}	3004	4(n)	V_{IN} (Under Test) = Pulse Generator V_{IN}(All Other Inputs) = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 7 (Pin D/F 1) (Pin C 1)	-	150	ns
171	Transition Time High to Low	t_{THL}	3004	4(n)	V_{IN} (Under Test) = Pulse Generator V_{IN}(All Other Inputs) = 5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 7 (Pin D/F 1) (Pin C 1)	-	150	ns
172	Maximum Clock Frequency	$f_{(CL)}$	-	-	Clock = Pulse Generator V_{DD} = 5Vdc, V_{SS} = 0Vdc Notes 7 and 9 (Pin D/F 16) (Pin C 19)	1.5	-	MHz

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

NOTES

1. GO-NO-GO Test, each pattern of Test Table 4(a).
   $V_{OH} \geq V_{DD}$ - 0.5Vdc $V_{OL} \leq 0.5$Vdc
2. Maximum time to output comparator strobe 300µsec.
3. Test each pattern of Table 4(a).
4. Interchange of forcing and measuring function is permitted.
5. This is performed as a Functional Test in which extreme V_{IN} conditions are applied and output voltage is measured.
6. Measurement performed on a sample basis LTPD 7, or less, with a Capacitance Bridge connected between each input under test and V_{SS}, only for Lots where LAT Level 2 is to be performed. (For LTPD sampling plan, see Annexe I of ESA/SCC 9000).
7. Measurement performed on a sample basis, LTPD 7 or less, (see Annexe I of ESA/SCC 9000).
8. Before commencement of test, load all stages with Low or High in accordance with Test Table 4(a) and measure propagation time at change.
9. A pulse, having the following conditions, shall be applied to the clock input: V_P = 0Vdc to V_{DD}Vdc. Maximum clock frequency $f_{(CL)}$ requirement is considered met if proper output stage changes occur with the pulse repetition rate set to that given in the "Limits" column.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
3 to 25	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 3 (Pin D/F 24) (Pin C 28)	-	30	µA
26 to 39	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0Vdc All Other Inputs: V_{IN} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	-100	nA
40 to 53	Input Current High Level	I_{IH}	3010	4(c)	V_{IN} (Under Test) = 15Vdc All Other Inputs: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	100	nA
54 to 61	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IN} (Write Enable & Enable) = 15Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	0.05	V

NOTES: See Page 24.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
62 to 69	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 15Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	14.95	-	V
70 to 77	Output Drive Current N-Channel	I_{OL1}	-	4(f)	V_{IN} (Write Enable & Enable) = 5Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 0.4Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	0.36	-	mA
78 to 85	Output Drive Current N-Channel	I_{OL2}	-	4(f)	V_{IN} (Write Enable & Enable) = 15Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 1.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	2.4	-	mA
86 to 93	Output Drive Current P-Channel	I_{OH1}	-	4(g)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 5Vdc V_{OUT} = 4.6Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-0.36	-	mA

NOTES: See Page 24.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
94 to 101	Output Drive Current P-Channel	I_{OH2}	-	4(g)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 15Vdc V_{OUT} = 13.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-2.4	-	mA
102 to 109	Output Leakage Current Third State (1)	I_{OZ1}	-	4(h)	V_{IN} (Enable) = 0Vdc All Other Inputs: V_{IN} = 15Vdc V_{OUT} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	12	µA
110 to 117	Output Leakage Current Third State (2)	I_{OZ2}	-	4(h)	V_{IN} (Enable) = 0Vdc All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	-12	µA
118	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	-	4(a)	V_{IL} = 1.5Vdc V_{IH} = 3.5Vdc V_{DD} = 5 Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}	-			-	0.5	

NOTES: See Page 24.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
119	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL2}	-	4(a)	V_{IL} = 4Vdc V_{IH} = 11Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH2}	-			-	1.5	
120	Threshold Voltage N-Channel	V_{THN}	-	4(i)	Clock Input at Ground All Other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10µA (Pin D/F 12) (Pin C 14)	-0.3	-3.5	V
121	Threshold Voltage P-Channel	V_{THP}	-	4(j)	Clock Input at Ground All Other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10µA (Pin D/F 24) (Pin C 28)	0.3	3.5	V

NOTES: See Page 24.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
3 to 25	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 3 (Pin D/F 24) (Pin C 28)	-	1.0	µA
26 to 39	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0Vdc All Other Inputs: V_{IN} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	-50	nA
40 to 53	Input Current High Level	I_{IH}	3010	4(c)	V_{IN} (Under Test) = 15Vdc All Other Inputs: V_{IN} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 3-8-9-10-11-13-14-15-16-17-18-19-20-21) (Pins C 3-9-10-12-13-15-16-17-19-20-21-22-23-24)	-	50	nA
54 to 61	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IN} (Write Enable & Enable) = 15Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	0.05	V

NOTES: See Page 24.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
62 to 69	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 15Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	14.95	-	V
70 to 77	Output Drive Current N-Channel	I_{OL1}	-	4(f)	V_{IN} (Write Enable & Enable) = 5Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 0.4Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	0.64	-	mA
78 to 85	Output Drive Current N-Channel	I_{OL2}	-	4(f)	V_{IN} (Write Enable & Enable) = 15Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 1.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	4.2	-	mA
86 to 93	Output Drive Current P-Channel	I_{OH1}	-	4(g)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 5Vdc V_{OUT} = 4.6Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-0.64	-	mA

NOTES: See Page 24.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
94 to 101	Output Drive Current P-Channel	I_{OH2}	-	4(g)	V_{IN} (Write/Read) = 0Vdc Clock Input from Low to High All Other Inputs: V_{IN} = 15Vdc V_{OUT} = 13.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-4.2	-	mA
102 to 109	Output Leakage Current Third State (1)	I_{OZ1}	-	4(h)	V_{IN} (Enable) = 0Vdc All Other Inputs: V_{IN} = 15Vdc V_{OUT} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	0.4	µA
110 to 117	Output Leakage Current Third State (2)	I_{OZ2}	-	4(h)	V_{IN} (Enable) = 0Vdc All Other Inputs: V_{IN} = 0Vdc V_{OUT} = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	-	-0.4	µA
118	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	-	4(a)	V_{IL} = 1.5Vdc V_{IH} = 3.5Vdc V_{DD} = 5 Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}	-			-	0.5	

NOTES: See Page 24.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
119	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL2}	-	4(a)	V_{IL} = 4Vdc V_{IH} = 11Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH2}	-			-	1.5	
120	Threshold Voltage N-Channel	V_{THN}	-	4(i)	Clock Input at Ground All Other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10µA (Pin D/F 12) (Pin C 14)	-0.7	-3.5	V
121	Threshold Voltage P-Channel	V_{THP}	-	4(j)	Clock Input at Ground All Other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10µA (Pin D/F 24) (Pin C 28)	0.7	3.5	V

NOTES: See Page 24.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - FUNCTIONAL AND QUIESCENT CURRENT TEST TABLE

PATTERN NO.	PIN NUMBERS																						I_{DD} TEST NO.	D.C. SUPPLY	
	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23		12	24
0	X	X	1	X	X	X	X	0	0	0	0	0	0	1	0	0	0	0	0	1	X	X		0	V_{DD}
1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	↓	↓
2	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0			
3	0	0	1	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	1	0	0			
4	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	2		
5	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0			
6	0	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0			
7	0	0	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0			
8	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0			
9	0	0	1	0	0	0	0	1	0	1	1	0	0	0	0	1	1	1	1	1	0	0			
10	0	0	1	0	0	0	0	1	0	0	1	1	0	0	1	1	1	1	1	1	0	0	3		
11	0	0	1	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	1	0	0	4		
12	0	0	1	0	0	0	0	1	1	0	0	1	1	0	1	0	0	0	1	1	0	0			
12a	0	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	1	0	0			
13	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0			
14	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	5		
15	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0			
16	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	1	1	0	0			
17	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1	0	0			
18	0	0	1	1	1	0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	0			
19	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0	0	0	1	1	1	0	0			
20	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	1	1	0	0			
21	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	1	1	1	1	6		
22	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	0	0			
23	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	1	1	0	0	7		
24	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1			
25	0	0	1	1	1	1	0	0	0	1	0	0	0	1	0	1	1	1	1	1	0	0			
26	0	0	1	0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	0	0	8		
27	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1			
28	0	0	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	1	1	0	0	9		
29	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0	0	0	1	1	0	0			
30	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1	1	10		
31	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	0	0	0	1	1	1	0			
32	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	1	1	1	0	0			
33	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	0	0	1	1	1	0	0			
34	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0	1	1	1	1	1			
35	0	0	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	1	1	1	1	1	11		
36	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	1	1	1	1	0	0			
37	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	0	1	1	1	1	0	0			
38	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1	1			
39	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	1	1	1	1	1	1	12		
40	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0			
41	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	0	0			

NOTES: See Page 37.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(a) - FUNCTIONAL AND QUIESCENT CURRENT TEST TABLE (CONTINUED)

PATTERN NO.	PIN NUMBERS																						IDD TEST NO.	D.C. SUPPLY	
	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23		12	24
42	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1		0	V_{DD}
43	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1			
44	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	1	1	0	0			
45	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0	0	13		
46	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	0	0	0	1	1	1	1	14		
47	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	0	0	1	1	1	1			
48	0	0	1	1	0	0	0	0	1	0	1	0	1	1	0	0	0	1	1	1	1	0			
49	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1	1	1	0	0			
50	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	0	0	1	1	1	1	1			
51	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	0	1	1	1	1	1	15		
52	0	0	1	1	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1	1	1	1			
53	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1	1	1	0	0			
54	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	0	1	1	1	1	1	1			
55	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	1	1	1			
56	0	1	1	1	1	1	0	0	1	0	1	0	1	1	0	1	1	1	1	1	1	1	16		
57	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	1	0	0			
58	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1			
59	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	1	1	1	1	1	1	1			
60	1	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	0	0	1	1	1	1			
61	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0	17		
62	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0	0	1	1	1	1			
63	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	0	0	1	1	1	1			
64	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0	0	1	1	1	1	1			
65	0	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	0	18		
66	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1			
67	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	0	1	1	1	1	1			
68	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0	1	1	1	1	1	1	19		
69	0	0	1	1	1	0	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1			
70	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	1	1	1	1	1	1			
71	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	1	1	1	1	1	1	20		
72	1	1	1	1	1	1	0	1	1	0	1	0	1	1	0	1	1	1	1	1	1	1			
73	0	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1			
74	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	21		
75	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1		↓	↓

NOTES: See Page 37.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(a) - FUNCTIONAL AND QUIESCENT CURRENT TEST TABLE (CONTINUED)

PATTERN NO.	PIN NUMBERS																						I_{DD} TEST NO.	D.C. SUPPLY	
	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23		12	24
76	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0	1	1	1	1	1	1		0	V_{DD}
77	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1			
78	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	1	1	1	1	1	1			
79	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	1	1	1	1	1	1			
80	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0	0	1	1	1	1	1			
81	0	1	1	1	1	1	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1			
82	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1			
83	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	0	1	1	1	1	1			
84	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0	0	0	1	1	1	1			
85	0	0	1	1	1	0	0	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1			
86	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0	0	1	1	1	1			
87	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	0	0	1	1	1	1			
88	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	0	0	0	0	1	1	1			
89	0	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0			
90	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1			
91	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1			
92	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0	1	1	1	0	1	1	1			
93	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0			
94	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	0	1	1	1			
95	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	1	1	1	0	1	1	1			
96	1	1	1	0	1	1	1	0	1	0	1	0	1	1	0	1	1	0	0	1	0	1			
97	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0	0	1	0	0			
98	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	1	1	1			
99	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	1	1	0	0	1	1	1			
100	1	1	1	0	0	1	1	0	1	0	1	0	1	1	0	1	0	0	0	1	0	0			
101	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	1	0	0			
102	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	0	0	0	1	1	1			
103	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	1	0	0	0	1	1	1			
104	1	0	1	0	0	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	0	0			
105	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0			
106	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	0	0	0	0	1	1	1			
107	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	0	0	0	1	1	1			

NOTES: See Page 37.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(a) - FUNCTIONAL AND QUIESCENT CURRENT TEST TABLE (CONTINUED)

PATTERN NO.	PIN NUMBERS																						I_{DD} TEST NO.	D.C. SUPPLY	
	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23		12	24
108	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	0	1	1	1	1	0	0		0	V_{DD}
109	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	0	1	1	1	1	0	0		↓	↓
110	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1	1		↓	↓
111	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	1	1	1	1	1	1		↓	↓
112	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	1	1	1	0	0		↓	↓
113	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	0	0	1	1	1	0	0		↓	↓
114	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0	1	1	1	1	1		↓	↓
115	0	0	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	1	1	1	1	1		↓	↓
116	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	1	1	0	0		↓	↓
117	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	1	1	0	0		↓	↓
118	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1	1		↓	↓
119	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	0	0	0	1	1	1	0		↓	↓
120	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0		↓	↓
121	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	1	0	0		↓	↓
122	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	1		↓	↓
123	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	1	0	0		↓	↓
124	0	0	1	0	0	0	0	1	0	0	1	0	1	1	0	1	1	1	0	1	0	0		↓	↓
125	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	0	1	0	0		↓	↓
126	1	1	1	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1		↓	↓
127	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	1	1	0	1	0	0		↓	↓
128	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	1	0	0	1	0	0		↓	↓
129	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	1	0	0		↓	↓
130	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0		↓	↓
131	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	0	1	0	0		↓	↓
132	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	1	0	0		↓	↓
133	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	1	0	0		↓	↓
134	1	0	1	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0		↓	↓
135	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0	0		↓	↓
136	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	1	0	0		↓	↓
137	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	0	0		↓	↓
138	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0		↓	↓
139	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0		↓	↓
140	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	1	1	0	0		↓	↓

NOTES: See Page 37.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(a) - FUNCTIONAL AND QUIESCENT CURRENT TEST TABLE (CONTINUED)

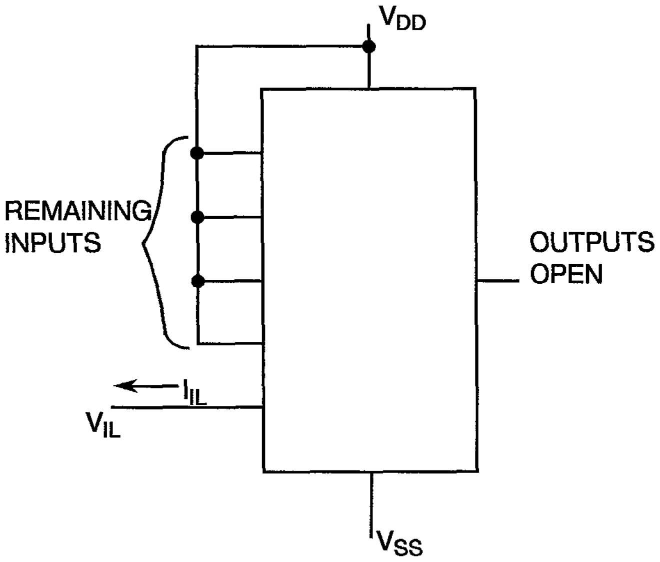
PATTERN NO.	PIN NUMBERS																						I_{DD} TEST NO.	D.C. SUPPLY	
	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23		12	24
141	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	0	0		0	V_{DD}
142	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0		↓	↓
143	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0		↓	↓
144	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1		↓	↓
145	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1		↓	↓
146	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0		↓	↓
147	Z	Z	0	Z	Z	Z	Z	0	0	0	0	0	0	1	0	1	1	1	1	0	Z	Z	22	↓	↓
148	Z	Z	0	Z	Z	Z	Z	0	0	0	0	0	0	1	1	1	1	1	1	0	Z	Z	23	↓	↓
149	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1		↓	↓

NOTES

1. Figure 4(a) illustrates one series of test patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: 1 = V_{IH} = V_{DD}, 0 = V_{IL} = V_{SS}, Z = High Impedance.

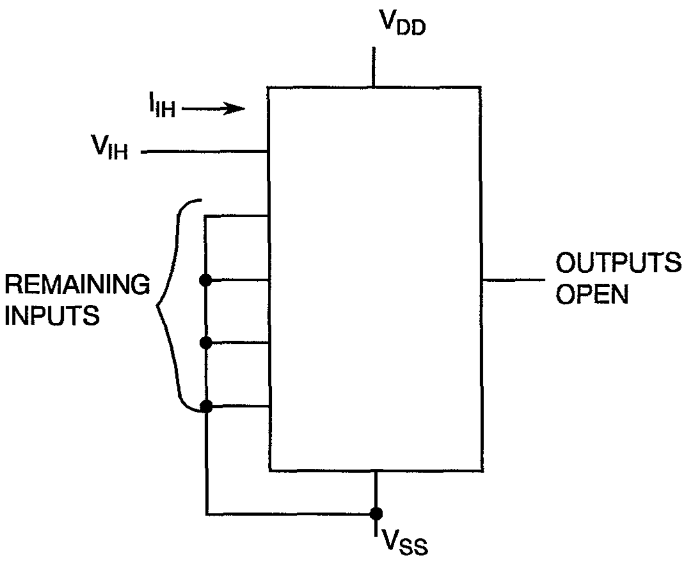
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - LOW LEVEL INPUT CURRENT



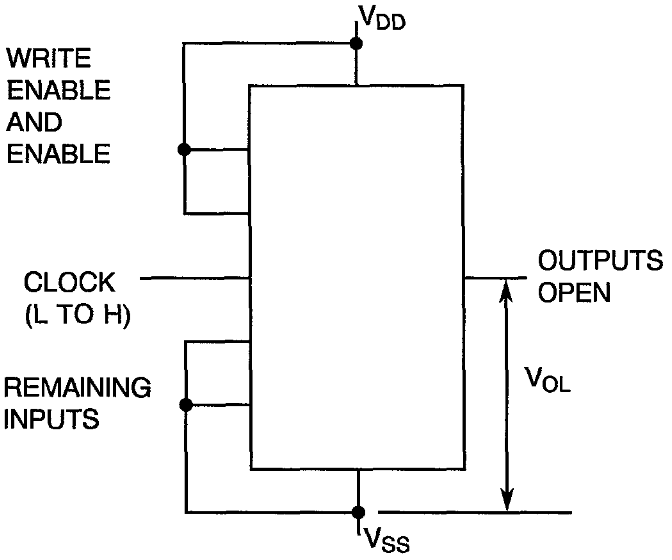
NOTES
1. Each input to be tested separately.

FIGURE 4(c) - HIGH LEVEL INPUT CURRENT



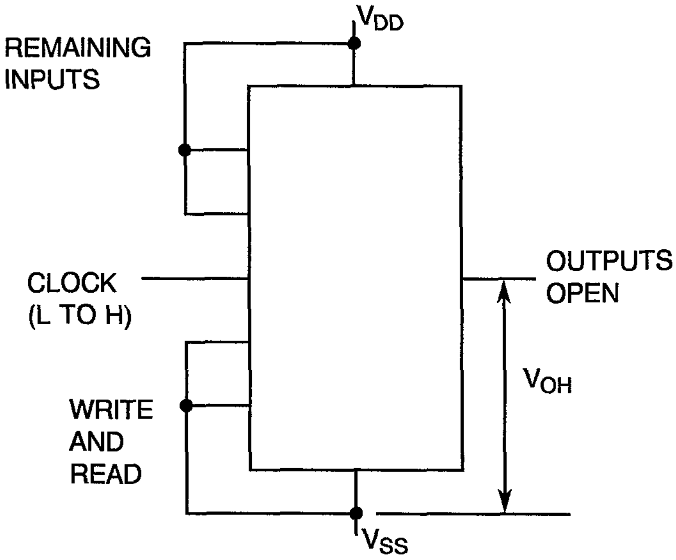
NOTES
1. Each input to be tested separately.

FIGURE 4(d) - LOW LEVEL OUTPUT VOLTAGE



NOTES
1. Each output to be tested separately.

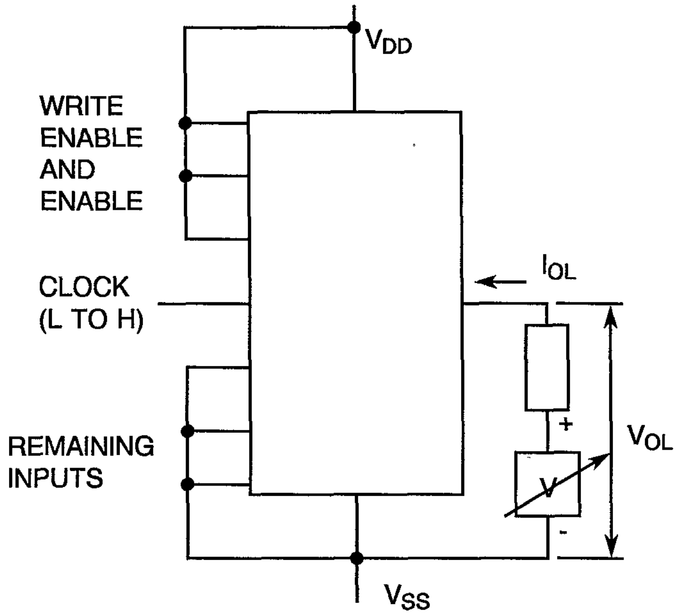
FIGURE 4(e) - HIGH LEVEL OUTPUT VOLTAGE



NOTES
1. Each output to be tested separately.

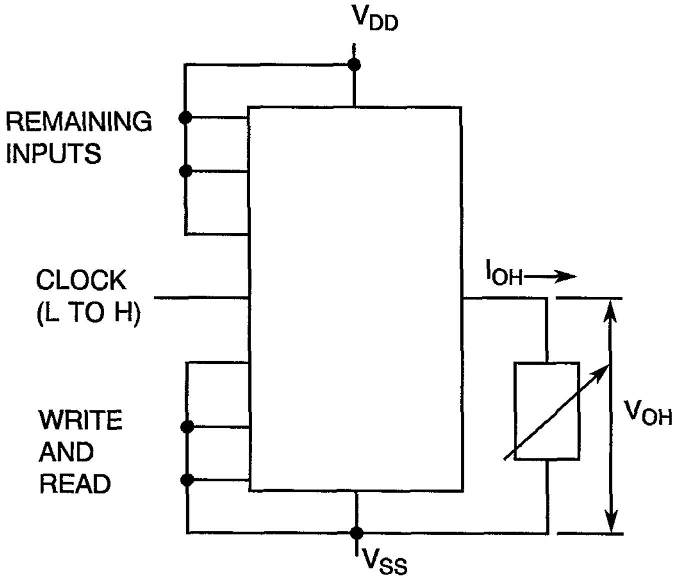
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(f) - LOW LEVEL OUTPUT CURRENT



NOTES
1. Each output to be tested separately.

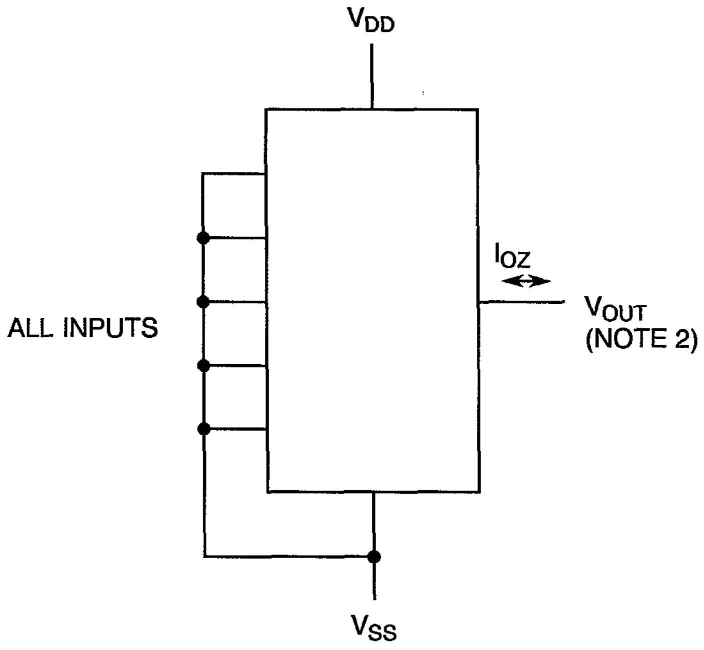
FIGURE 4(g) - HIGH LEVEL OUTPUT CURRENT



NOTES
1. Each output to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES

1. Each output to be tested separately.
2. I_{OZ} is measured with the following output conditions:
   (i) Output under test connected to V_{DD}. Remaining outputs open.
   (ii) Output under test connected to V_{SS}. Remaining outputs open.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - THRESHOLD VOLTAGE N-CHANNEL

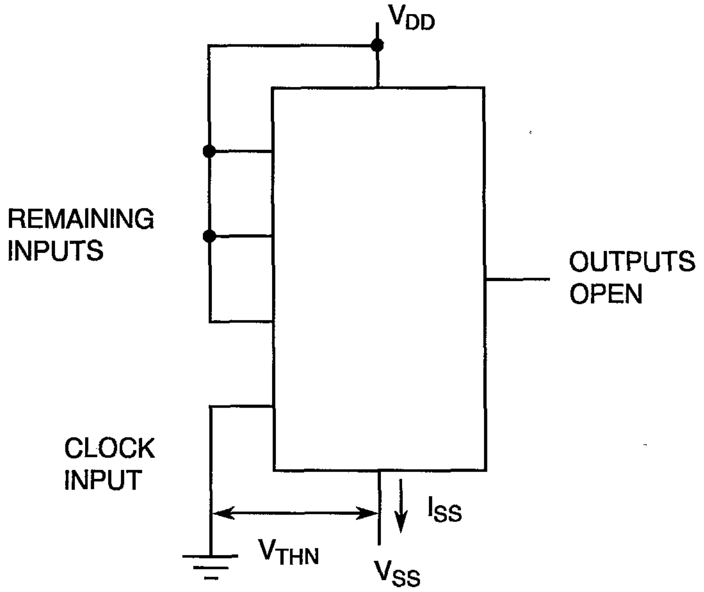


FIGURE 4(j) - THRESHOLD VOLTAGE P-CHANNEL

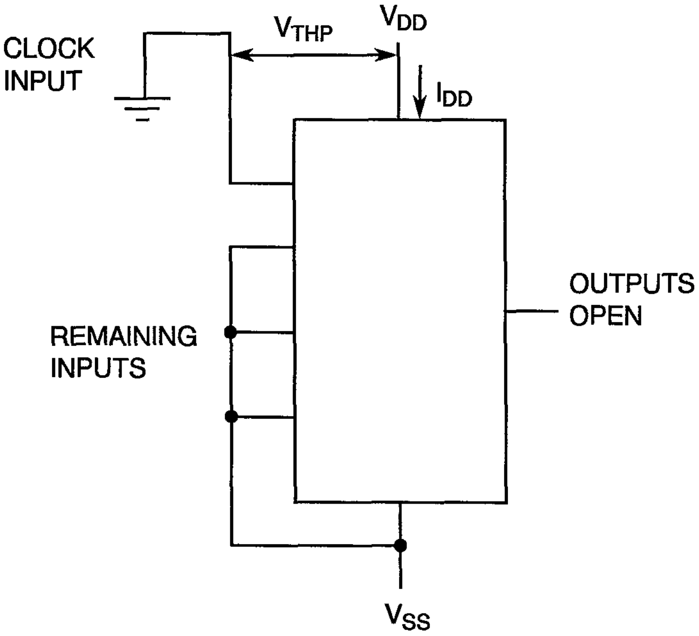
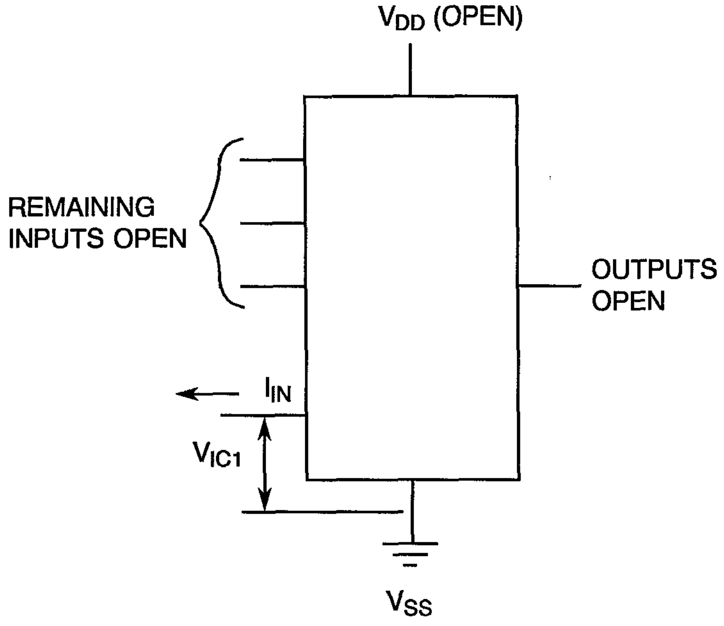


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

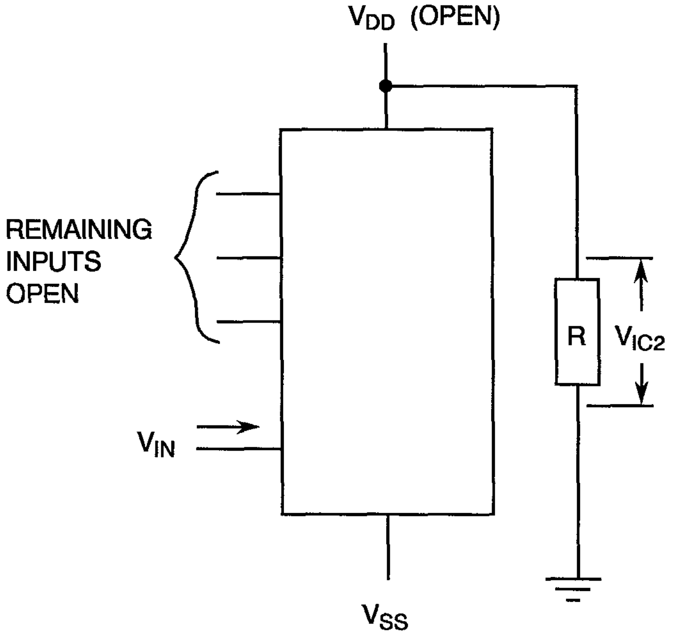
FIGURE 4(k) - INPUT CLAMP VOLTAGE (V_{SS})



NOTES

1. Each input to be tested separately.

FIGURE 4(l) - INPUT CLAMP VOLTAGE (V_{DD})

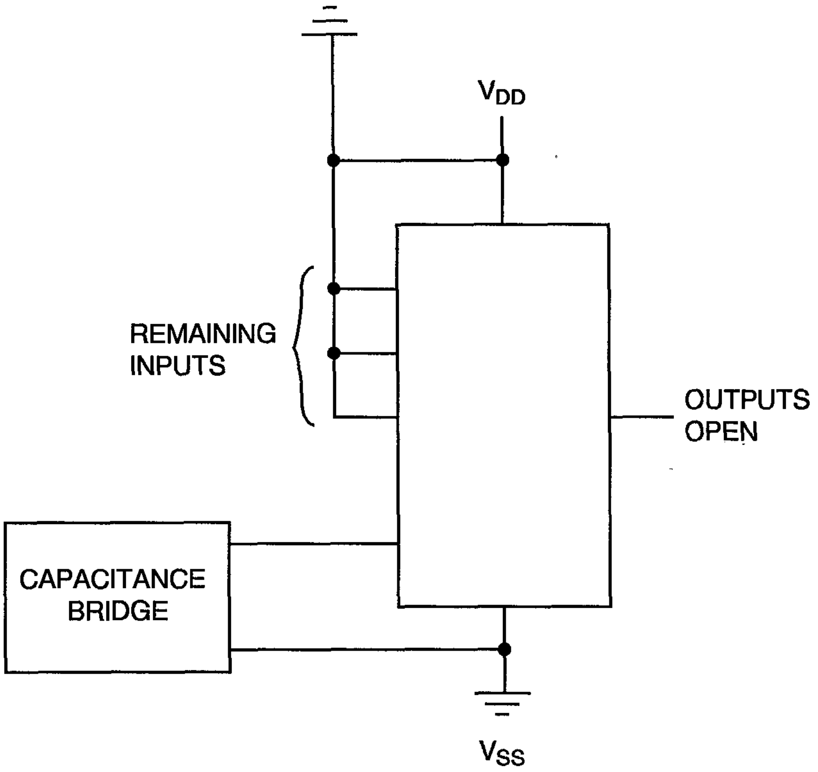


NOTES

1. Each input to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

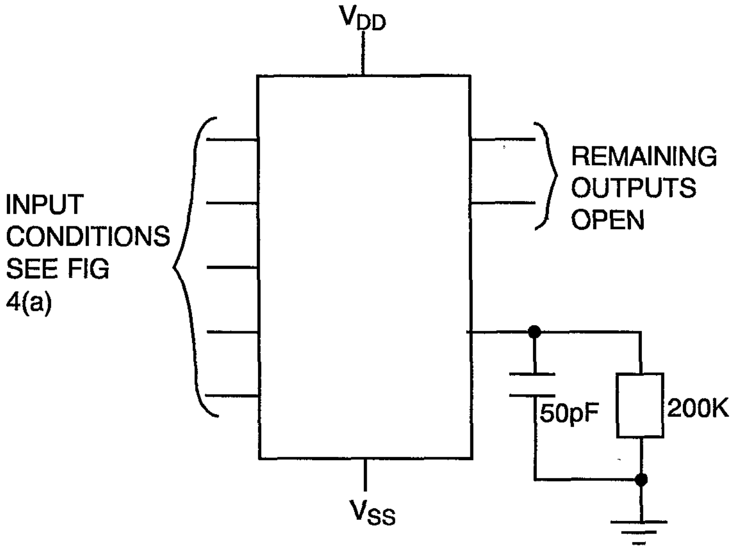
FIGURE 4(m) - INPUT CAPACITANCE



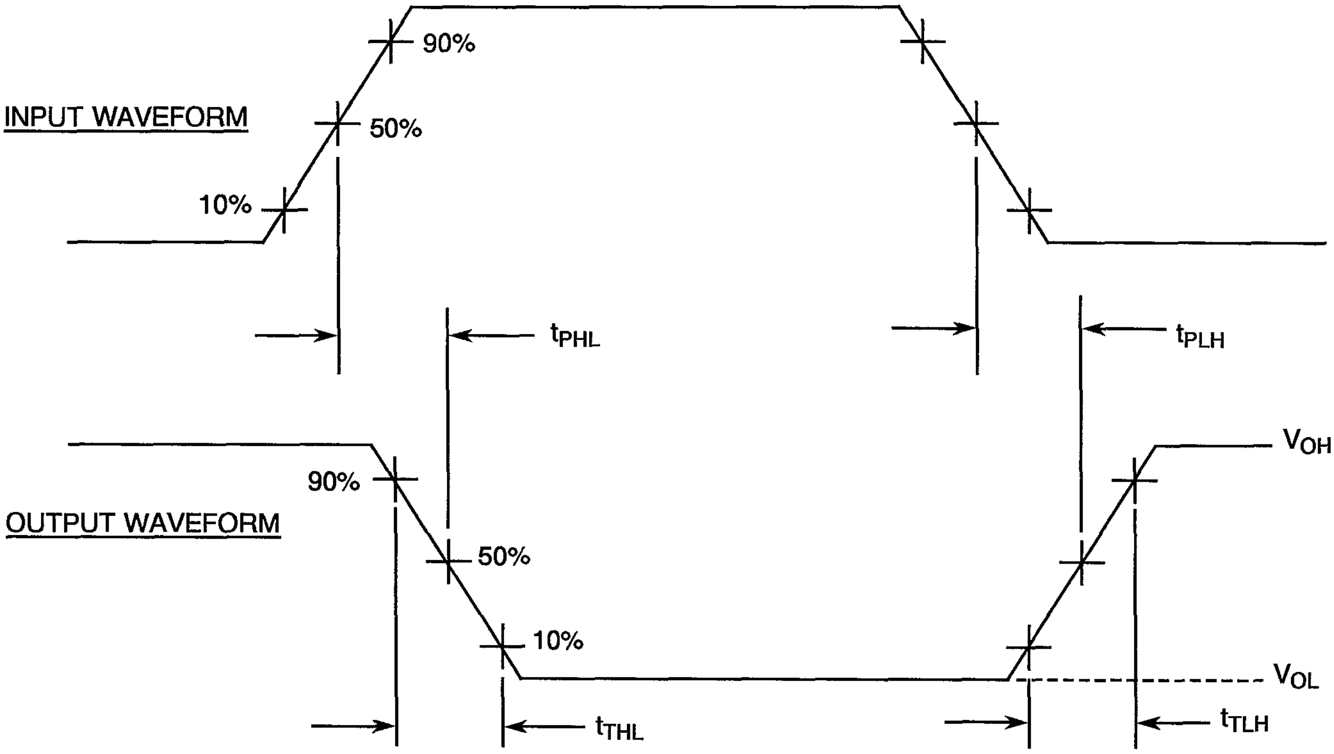
NOTES
1. Each input to be tested separately.
2. f = 100kHz to 1MHz

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(n) - PROPAGATION DELAY AND TRANSITION TIME



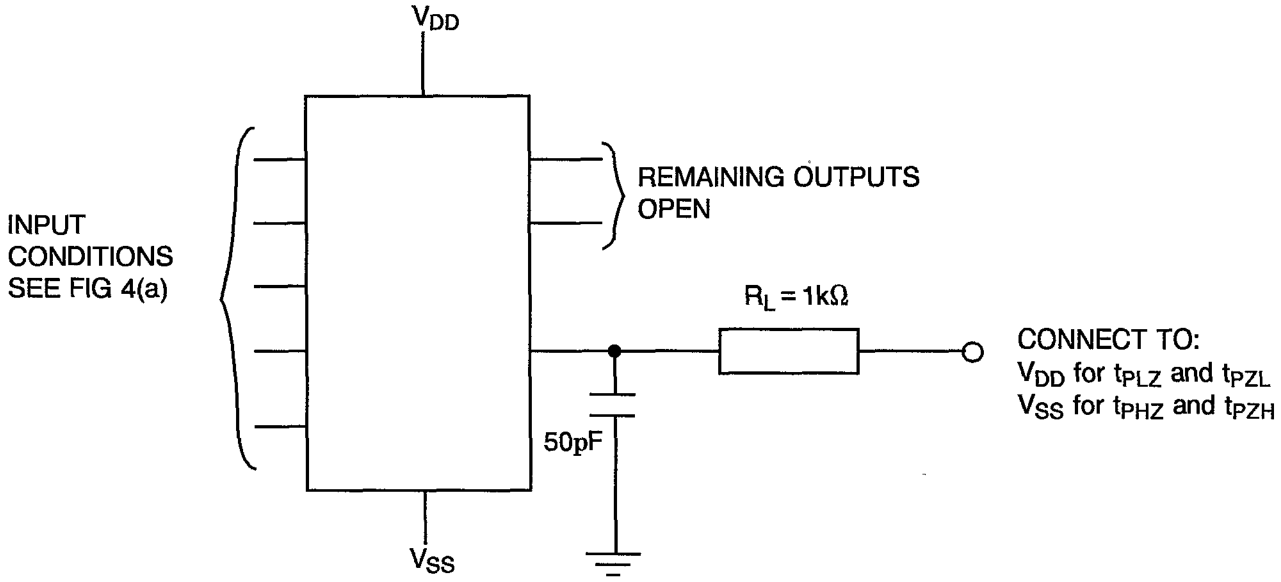
VOLTAGE WAVEFORMS



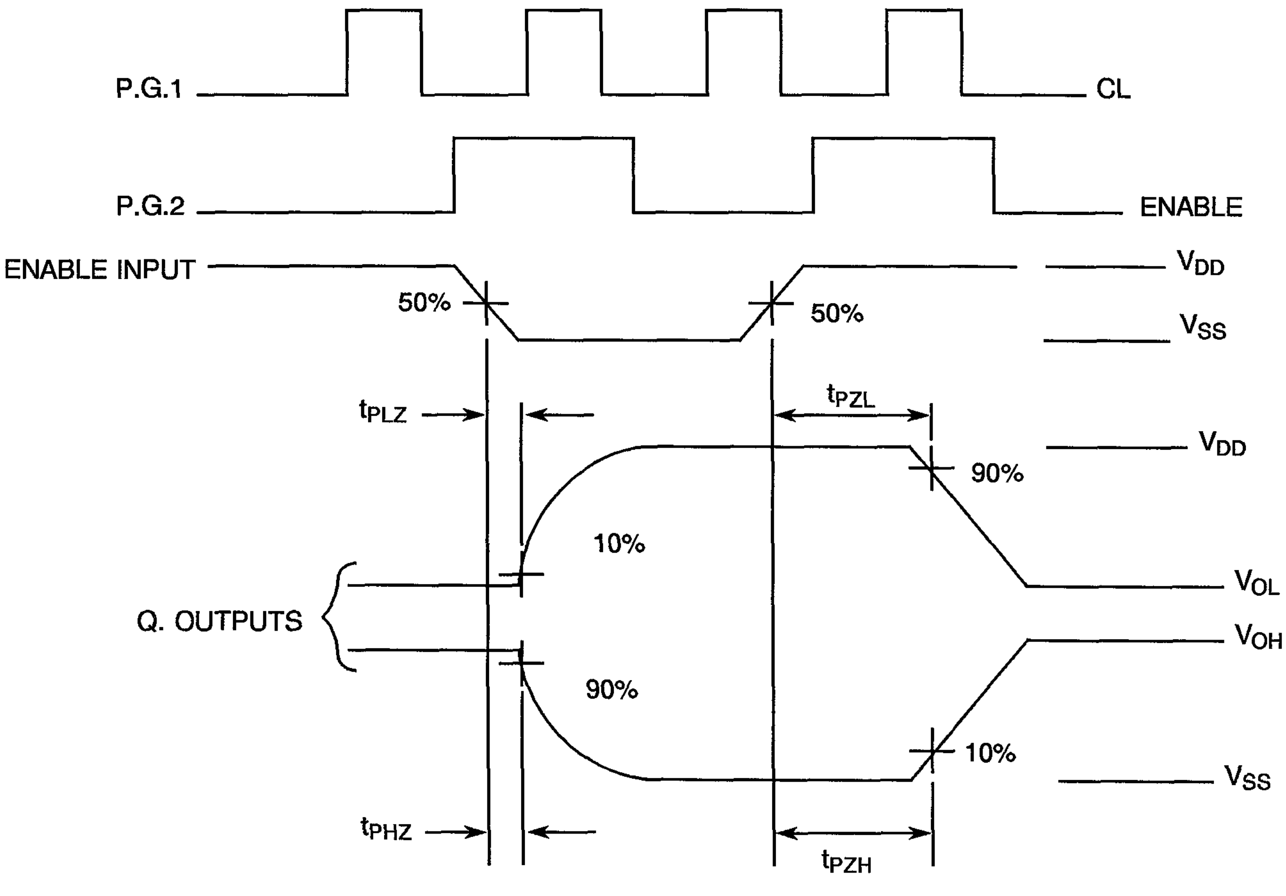
NOTES 1. Pulse Generator - $V_P = 0$ to V_{DD}, t_r and $t_f \leq 15ns$, $f = 500kHz$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(o) - PROPAGATION DELAY OUTPUT TO HIGH IMPEDANCE



VOLTAGE WAVEFORM



NOTES 1. Pulse Generator - $V_P = 0$ to V_{DD}, t_r and $t_f \leq 15ns$, $f = 500kHz$.

TABLE 4 - PARAMETER DRIFT VALUES

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
3 to 25	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±150	nA
70 to 77	Output Drive Current N-Channel	I_{OL1}	As per Table 2	As per Table 2	±15 (1)	%
86 to 93	Output Drive Current P-Channel	I_{OH1}	As per Table 2	As per Table 2	±15 (1)	%
102 to 109	Output Leakage Current Third State (1)	I_{OZ1}	As per Table 2	As per Table 2	±60	nA
110 to 117	Output Leakage Current Third State (2)	I_{OZ2}	As per Table 2	As per Table 2	±60	nA
120	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.3	V
121	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.3	V

NOTES 1. Percentage of limit value if voltage is the measurement function.

TABLE 5(a) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	V_{OUT}	Open	-
3	Inputs - (Pins D/F 3-9-11-13-15-17-19-21) (Pins C 3-10-13-15-17-20-22-24)	V_{IN}	V_{DD}	Vdc
4	Inputs - (Pins D/F 8-10-14-16-18-20) (Pins C 9-12-16-19-21-23)	V_{IN}	Ground	Vdc
5	Positive Supply Voltage (Pin D/F 24) (Pin C 28)	V_{DD}	15	Vdc
6	Negative Supply Voltage (Pin D/F 12) (Pin C 14)	V_{SS}	Ground	Vdc

NOTES 1. Input Load = Protection Resistor = 2kΩ minimum to 47kΩ maximum.

TABLE 5(b) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	V_{OUT}	Open	-
3	Inputs - (Pins D/F 3-9-11-13-15-17-19-21) (Pins C 3-10-13-15-17-20-22-24)	V_{IN}	Ground	Vdc
4	Inputs - (Pins D/F 8-10-14-16-18-20) (Pins C 9-12-16-19-21-23)	V_{IN}	V_{DD}	Vdc
5	Positive Supply Voltage (Pin D/F 24) (Pin C 28)	V_{DD}	15	Vdc
6	Negative Supply Voltage (Pin D/F 12) (Pin C 14)	V_{SS}	Ground	Vdc

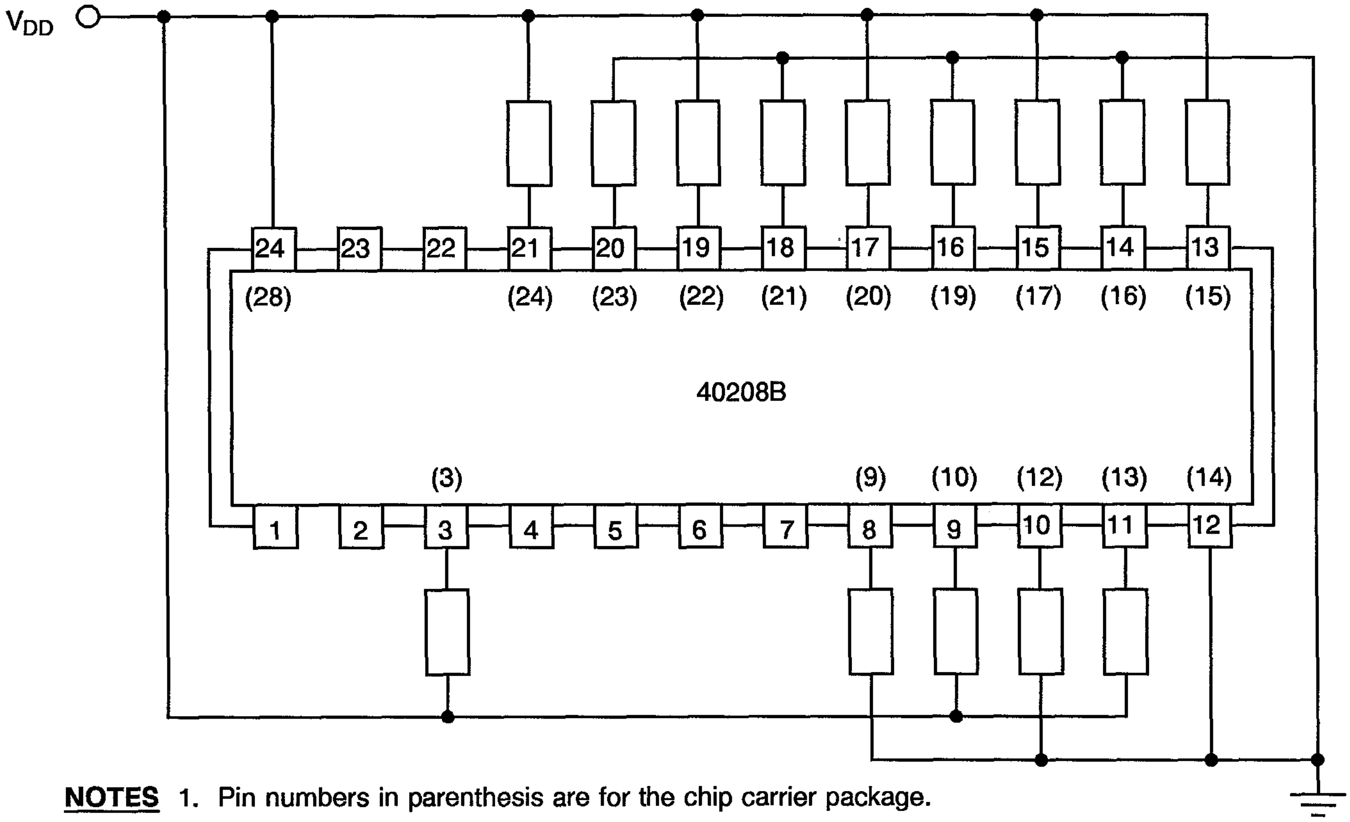
NOTES 1. Input Load = Protection Resistor = 2kΩ minimum to 47kΩ maximum.

TABLE 5(c) - CONDITIONS FOR BURN-IN DYNAMIC

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0-5)	°C
2	Outputs - (Pins D/F 1-2-4-5-6-7-22-23) (Pins C 1-2-5-6-7-8-26-27)	V_{OUT}	$V_{DD/2}$	Vdc
3	Inputs - (Pins D/F 3-15-21) (Pins C 3-17-24)	V_{IN}	V_{DD}	Vdc
4	Inputs - (Pins D/F 8-10-14-16-19-20) (Pins C 9-12-16-19-22-23)	V_{IN}	V_{GEN1}	Vac
5	Inputs - (Pins D/F 9-11-13-17-18) (Pins C 10-13-15-20-21)	V_{IN}	V_{GEN2}	Vac
6	Pulse Voltage	V_{GEN}	0 to V_{DD}	Vac
7	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	50k, 50% Duty Cycle 25k, 50% Duty Cycle	Hz
8	Positive Supply Voltage (Pin D/F 24) (Pin C 28)	V_{DD}	15	Vdc
9	Negative Supply Voltage (Pin D/F 12) (Pin C 14)	V_{SS}	Ground	Vdc

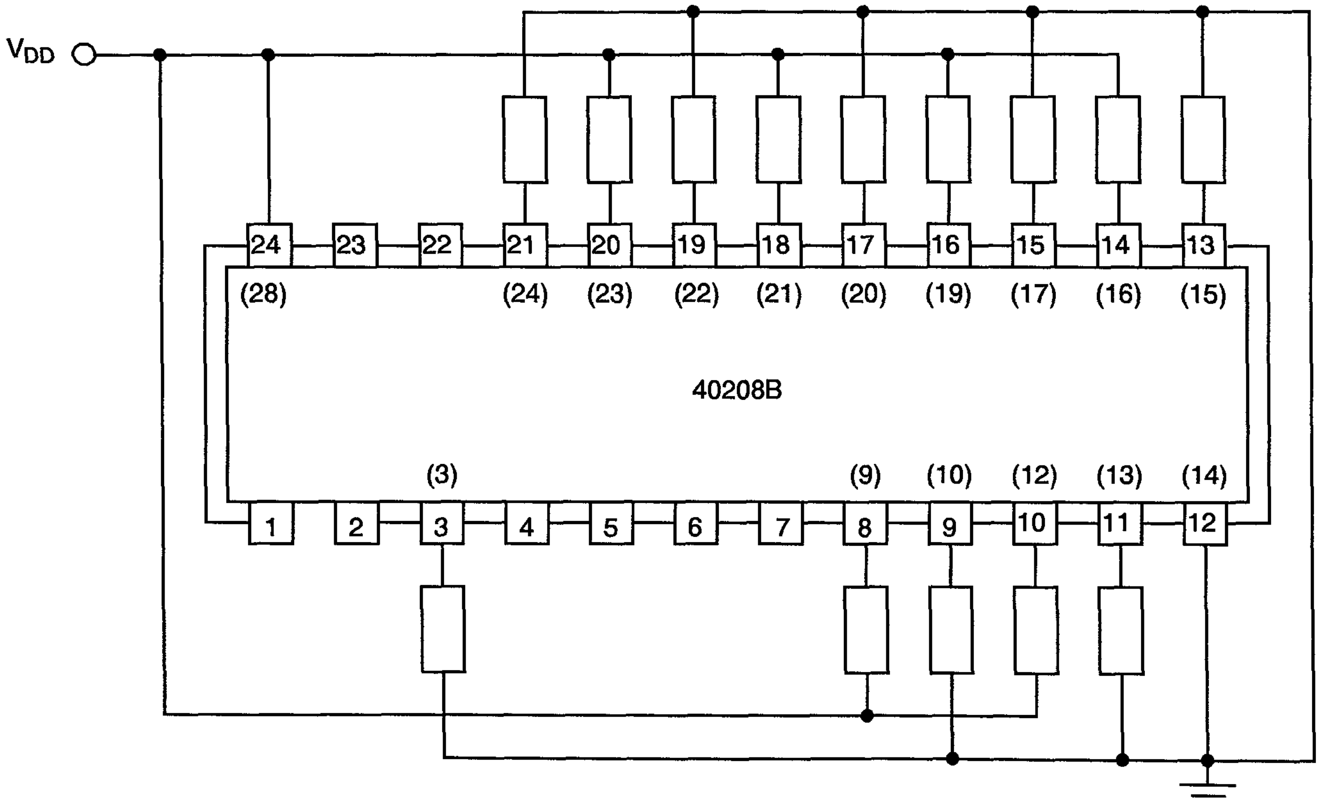
NOTES 1. Input Load = Output Load = 2kΩ minimum to 47kΩ maximum.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS



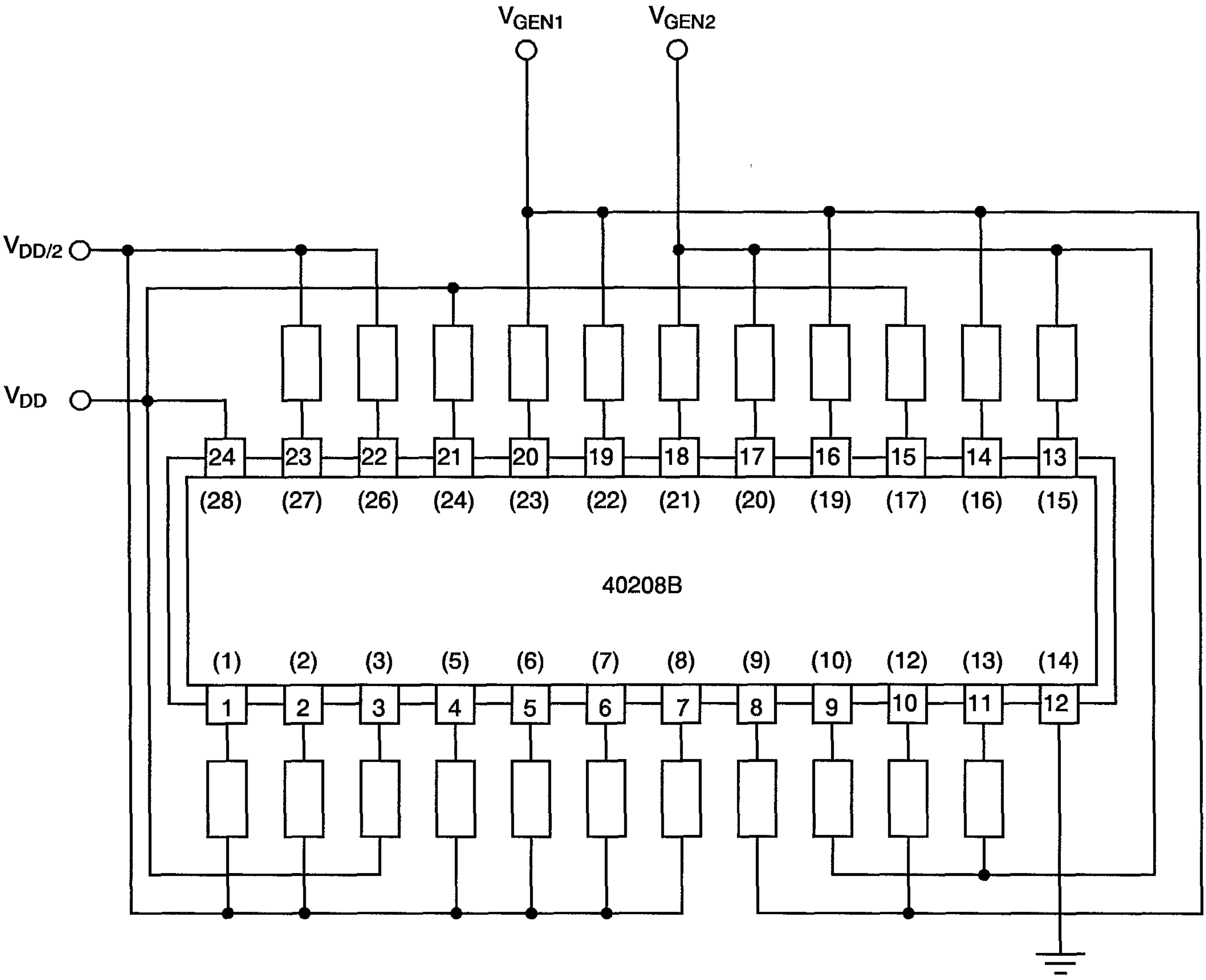
NOTES 1. Pin numbers in parenthesis are for the chip carrier package.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS



NOTES 1. Pin numbers in parenthesis are for the chip carrier package.

FIGURE 5(c) - ELECTRICAL CIRCUIT FOR BURN-IN DYNAMIC



NOTES 1. Pin numbers in parenthesis are for the chip carrier package.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at T_{amb} = +22 ± 3 °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at T_{amb} = +22 ± 3 °C.

4.8.4 Conditions for Operating Life Test

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(c) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)			UNIT
						MIN	MAX	
1	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
3 to 25	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±150	-	-	nA
26 to 39	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	-	-50	nA
40 to 53	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	-	50	nA
54 to 61	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	-	0.05	V
62 to 69	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	-	14.95	-	V
70 to 77	Output Drive Current N-Channel	I_{OL1}	As per Table 2	As per Table 2	±15 (1)	-	-	%
78 to 85	Output Drive Current N-Channel	I_{OL2}	As per Table 2	As per Table 2	±15 (1)	-	-	%
86 to 93	Output Drive Current P-Channel	I_{OH1}	As per Table 2	As per Table 2	±15 (1)	-	-	%
94 to 101	Output Drive Current P-Channel	I_{OH2}	As per Table 2	As per Table 2	±15 (1)	-	-	%
102 to 109	Output Leakage Current Third State (1)	I_{OZ1}	As per Table 2	As per Table 2	±60	-	-	nA
110 to 117	Output Leakage Current Third State (2)	I_{OZ2}	As per Table 2	As per Table 2	±60	-	-	nA

NOTES 1. Percentage of limit value if voltage is the measurement function.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONTINUED)

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)			UNIT
						MIN	MAX	
118	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	As per Table 2	As per Table 2	-	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}			-	-	0.5	
120	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.3	-	-	V
121	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.3	-	-	V

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATION
Para. 4.2.3	Para. 9.23, High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Para. 9.24, Power Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.4	Para. 9.21.1, Operating Life during Qualification Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.5	Para. 9.21.2, Operating Life during Lot Acceptance Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.