# INTEGRATED CIRCUITS, SILICON MONOLITHIC, HCMOS ASYNCHRONOUS NEGATIVE-EDGE-TRIGGERED 12-BIT BINARY COUNTER, WITH FULLY BUFFERED OUTPUTS

## BASED ON TYPE 54HC4040

## ESCC Detail Specification No. 9204/069


| | |
|---|---|
| Issue 2 | September 2003 |


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**DOCUMENTATION CHANGE NOTICE**

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| DCR No. | CHANGE DESCRIPTION |
|---|---|
| 46 | Specification upissued to incorporate editorial and technical changes per DCR. |

**TABLE OF CONTENTS**

## 1. GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

### 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

### 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

### 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

#### 1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 920406901B
- Detail Specification Reference: 9204069
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: F (as required)

#### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

| Variant Number | Based on Type | Case | Terminal Material and /or Finish | Weight max g | Total Dose Radiation Level Letter |
|---|---|---|---|---|---|
| 01 | 54HC4040 | FP | G2 or G8 | 0.7 | F [50kRAD(Si)] |
| 02 | 54HC4040 | FP | G4 | 0.7 | F [50kRAD(Si)] |
| 05 | 54HC4040 | CCP | 2 | 0.6 | F [50kRAD(Si)] |
| 10 | 54HC4040 | DIP | G2 | 2.2 | F [50kRAD(Si)] |
| 11 | 54HC4040 | DIP | G4 | 2.2 | F [50kRAD(Si)] |
| 12 | 54HC4040 | SO | G2 | 0.7 | F [50kRAD(Si)] |
| 13 | 54HC4040 | SO | G4 | 0.7 | F [50kRAD(Si)] |

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the purchase order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the applicable ESCC Generic Specification.

| Characteristics | Symbols | Maximum Ratings | Units | Remarks |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to 7 | V | Note 1 |
| Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$ +0.5 | V | Notes 1, 2 |
| Output Voltage | $V_{OUT}$ | -0.5 to $V_{DD}$ +0.5 | V | Notes 1, 3 |
| Device Power Dissipation (Continuous) | $P_D$ | 300 | mW | Note 4 |
| Supply Current | $I_{DDop}$ | 50 | mA | |
| Operating Temperature Range | $T_{op}$ | -55 to +125 | $^oC$ | $T_{amb}$ |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | $^oC$ | |
| Soldering Temperature<br>For FP, DIP and SO<br>For CCP | $T_{sol}$ | <br>+265<br>+245 | $^oC$ | <br>Note 5<br>Note 6 |

**NOTES:**

1. Device is functional for $2V \leq V_{DD} \leq 6V$.
2. Input current limited to $I_{IC}=\pm 20mA$.
3. Output current limited to $I_{OUT}=\pm 25mA$.
4. The maximum device dissipation is determined by $I_{DDop}$ max (50mA)x6V.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
6. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

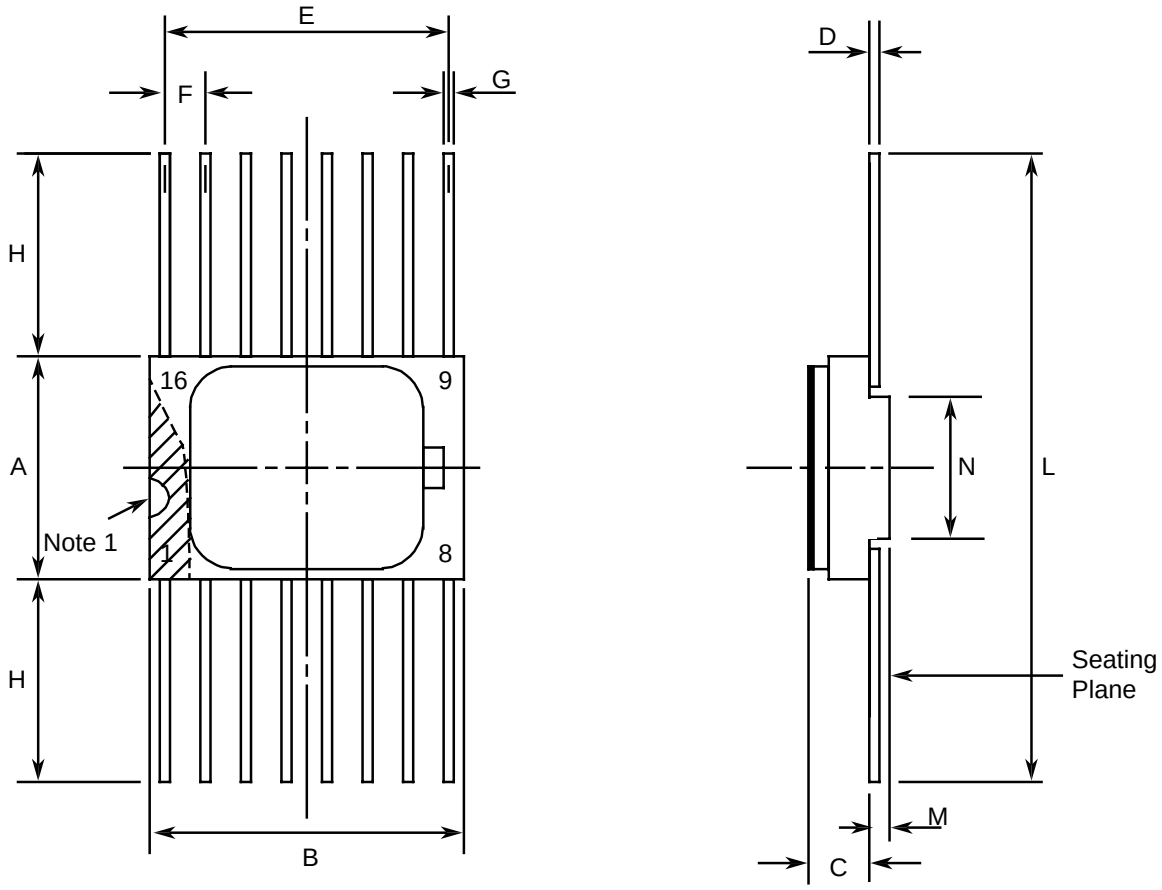
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2500 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

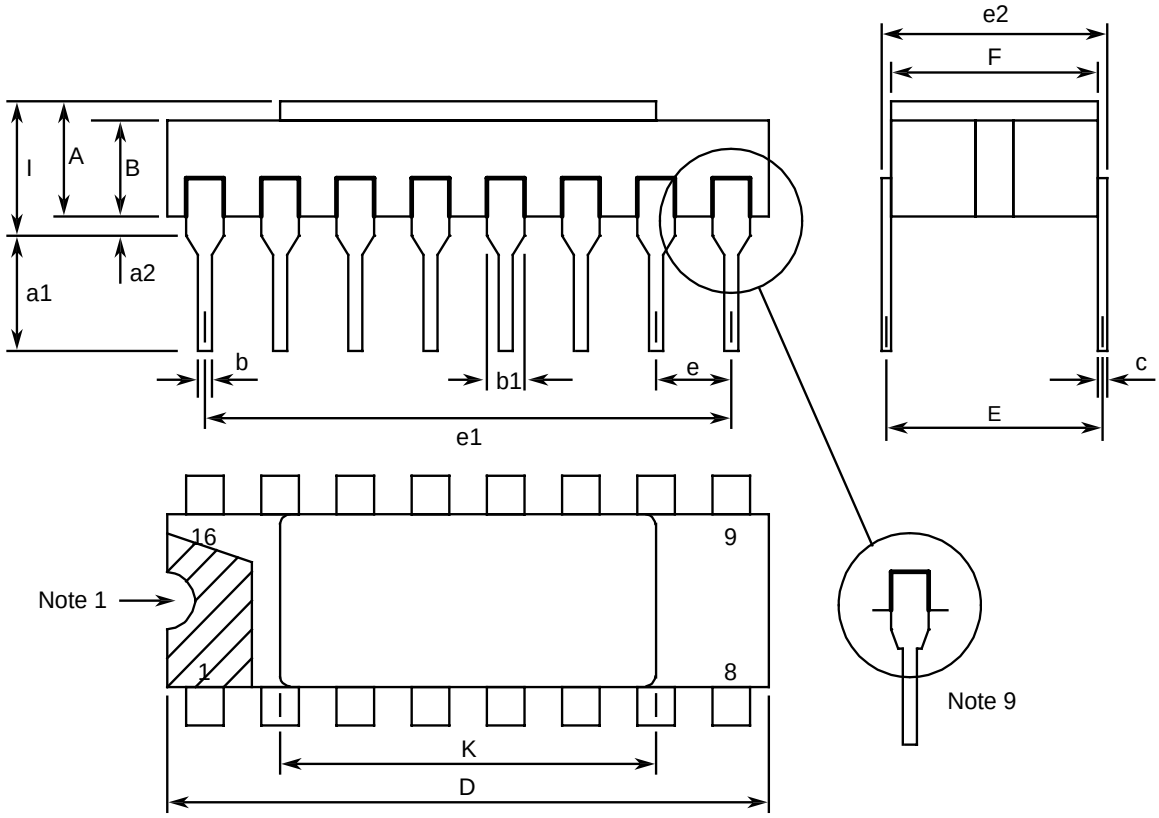
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 16 Pin




| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| A | 6.75 | 7.06 | |
| B | 9.76 | 10.14 | |
| C | 1.49 | 1.95 | |
| D | 0.1 | 0.15 | 5 |
| E | 8.76 | 9.01 | |
| F | 1.27 TYPICAL | | 3, 6 |
| G | 0.38 | 0.48 | 5 |
| H | 6 | - | 5 |
| L | 18.75 | 22 | |
| M | 0.33 | 0.43 | |
| N | 4.32 TYPICAL | | |

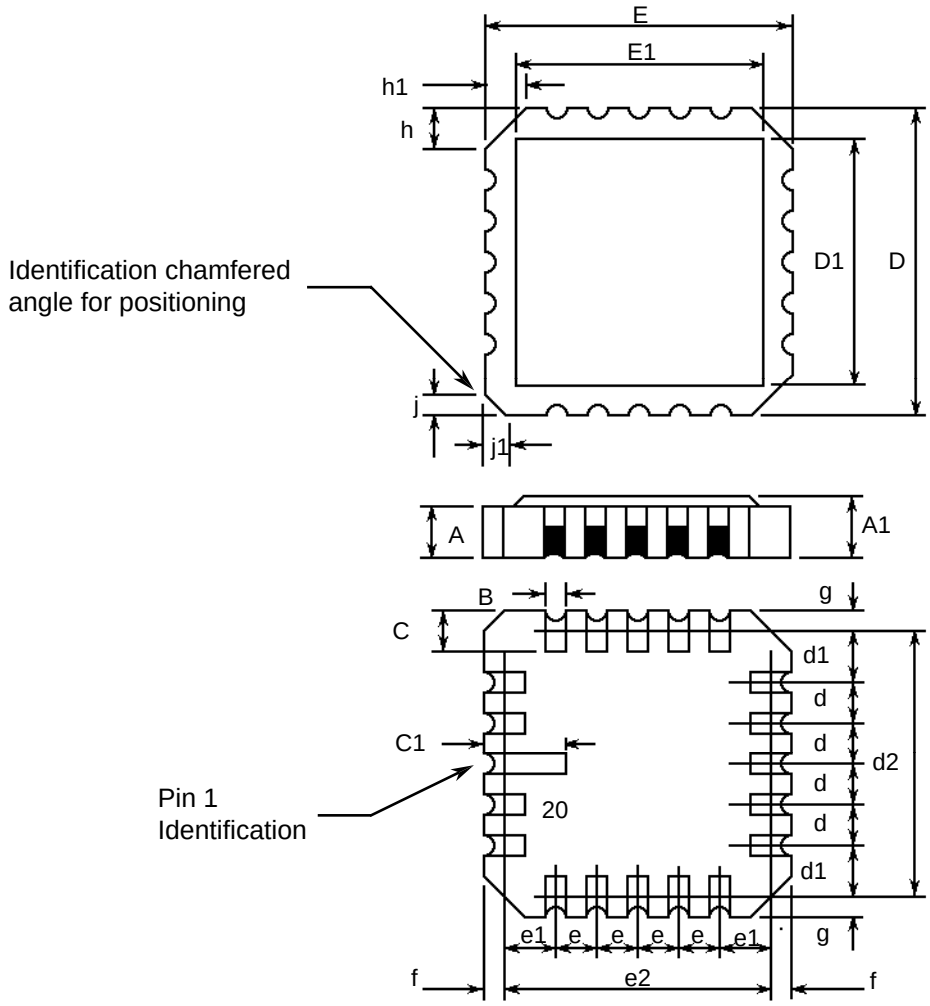
1.7.2 Dual-in-line Package (DIP) - 16 Pin




| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| A | 2.1 | 2.71 | |
| a1 | 3 | 3.7 | |
| a2 | 0.63 | 1.14 | 2 |
| B | 1.82 | 2.39 | |
| b | 0.4 | 0.5 | 5 |
| b1 | 1.14 | 1.5 | 5 |
| c | 0.2 | 0.3 | 5 |
| D | 20.06 | 20.58 | |
| E | 7.36 | 7.87 | |
| e | 2.54 TYPICAL | | 4, 6 |
| e1 | 17.65 | 17.9 | |
| e2 | 7.62 | 8.12 | |
| F | 7.29 | 7.7 | |
| I | - | 3.83 | |

| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| K | 10.9 | 12.1 | |

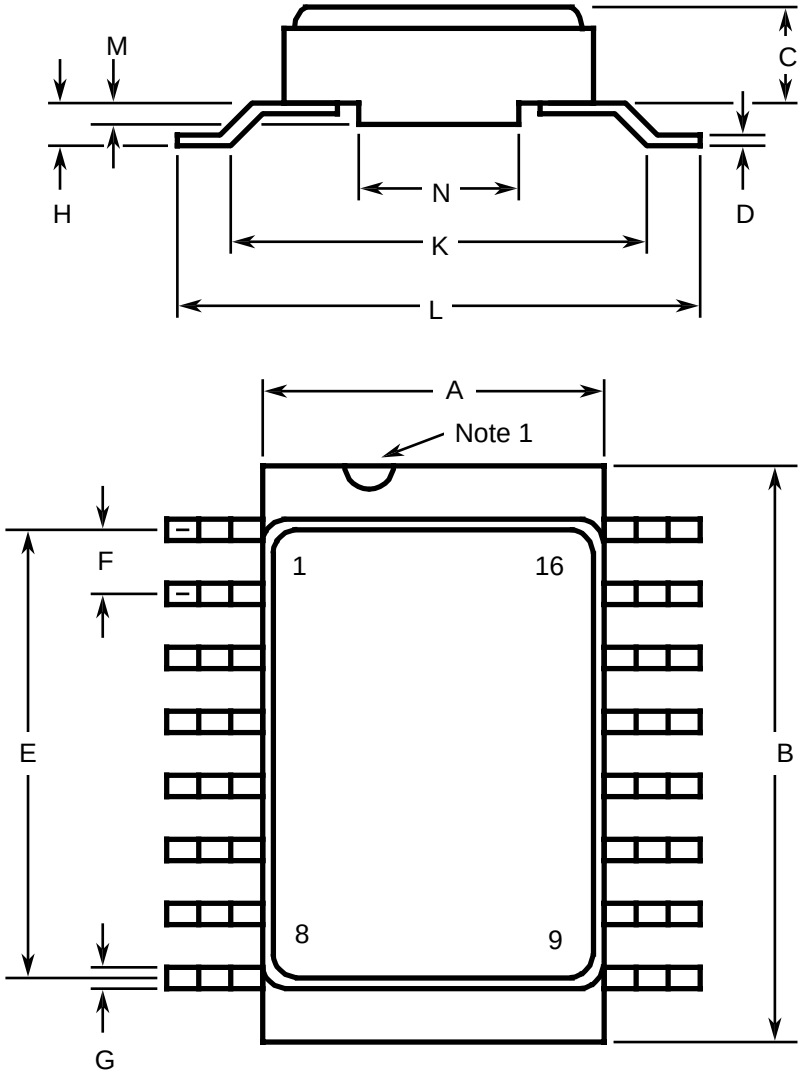
1.7.3 Chip Carrier Package (CCP) - 20 Terminal




| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| A | 1.14 | 1.95 | |
| A1 | 1.63 | 2.36 | |
| B | 0.55 | 0.72 | 5 |
| C | 1.06 | 1.47 | 5 |
| C1 | 1.91 | 2.41 | |
| D | 8.67 | 9.09 | |

| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| D1 | 7.21 | 7.52 | |
| d, d1 | 1.27 TYPICAL | | 3, 6 |
| d2 | 7.62 TYPICAL | | |
| E | 8.67 | 9.09 | |
| E1 | 7.21 | 7.52 | |
| e, e1 | 1.27 TYPICAL | | 3, 6 |
| e2 | 7.62 TYPICAL | | |
| f, g | - | 0.76 | |
| h, h1 | 1.01 TYPICAL | | 8 |
| j, j1 | 0.51 TYPICAL | | 7 |

1.7.4 Small Outline Ceramic Package (SO) - 16 Pin




| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| A | 6.75 | 7.06 | |
| B | 9.76 | 10.14 | |
| C | 1.49 | 1.95 | |
| D | 0.1 | 0.15 | 5 |
| E | 8.76 | 9.01 | |
| F | 1.27 TYPICAL | | 3, 6 |
| G | 0.38 | 0.48 | 5 |
| H | 0.6 | 0.9 | 5 |

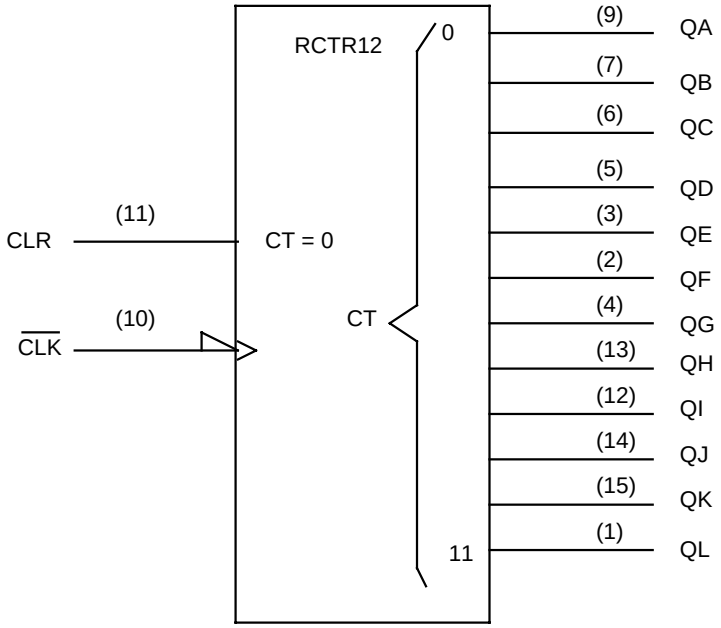
| Symbols | Dimensions mm | | Notes |
|---|---|---|---|
| | Min | Max | |
| K | 9 TYPICAL | | |
| L | 10 | 10.65 | |
| M | 0.33 | 0.43 | |
| N | 4.31 TYPICAL | | |

1.7.5 Consolidated Notes

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces for flat, dual-in-line and small outline packages.
   16 spaces for chip carrier packages.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only.



1.9 PIN ASSIGNMENT

| Pin | Function | | Pin | Function | |
|---|---|---|---|---|---|
| | FP, DIP and SO | CCP | | FP, DIP and SO | CCP |
| 1 | QL Output | - | 11 | CLR Input (Clear) | - |
| 2 | QF Output | QL Output | 12 | QI Output | QA Output |
| 3 | QE Output | QF Output | 13 | QH Output | $\overline{CLK}$ Input (Clock) |
| 4 | QG Output | QE Output | 14 | QJ Output | CLR Input (Clear) |
| 5 | QD Output | QG Output | 15 | QK Output | QI Output |
| 6 | QC Output | - | 16 | $V_{DD}$ | - |
| 7 | QB Output | QD Output | 17 | - | QH Output |
| 8 | $V_{SS}$ | QC Output | 18 | - | QJ Output |
| 9 | QA Output | QB Output | 19 | - | QK Output |
| 10 | $\overline{CLK}$ Input (Clock) | $V_{SS}$ | 20 | - | $V_{DD}$ |

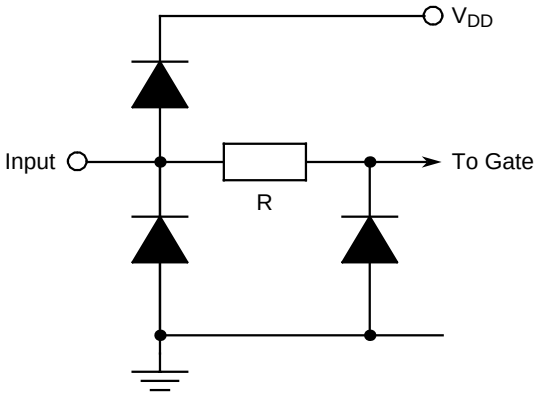
1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
2. ↑ = Transition, Low to High, ↓ = Transition, High to Low.

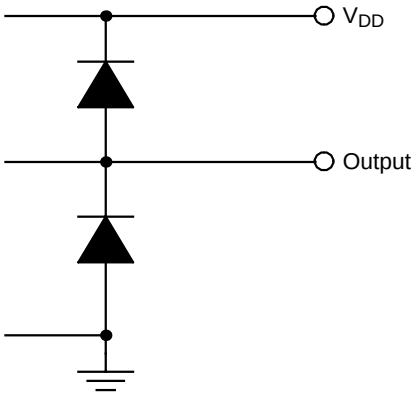
| INPUTS | | OUTPUTS Q |
|---|---|---|
| $\overline{CLK}$ | CLR | |
| X | H | ALL OUTPUTS = L |
| ↑ | L | NO CHANGE |
| ↓ | L | ADVANCE TO NEXT STATE |

1.11 PROTECTION NETWORKS

INPUT PROTECTION




OUTPUT PROTECTION




## 2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the applicable ESCC Generic Specification. Permitted deviations from the applicable Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes

are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb}$=+22 ± 3°C.

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table without Load<br>$V_{IL}$=0.3V,$V_{IH}$=1.5V<br>$V_{DD}$=2V,$V_{SS}$=0V<br>$t_r$<1µs, Note 2 | - | - | - |
| Functional Test 2 | - | 3014 | Verify Truth Table without Load<br>$V_{IL}$=0.9V,$V_{IH}$=3.15V<br>$V_{DD}$=4.5V,$V_{SS}$=0V<br>$t_r$=$t_f$<500ns<br>Note 2 | - | - | - |
| Functional Test 3 | - | 3014 | Verify Truth Table without Load<br>$V_{IL}$=1.2V,$V_{IH}$=4.2V<br>$V_{DD}$=6V,$V_{SS}$=0V<br>$t_r$=$t_f$<400ns<br>Note 2 | - | - | - |
| Quiescent Current | $I_{DD}$ | 3005 | $V_{IL}$=0V,$V_{IH}$=6V<br>$V_{DD}$=6V,$V_{SS}$=0V<br>All Outputs Open<br>Note 3 | - | 400 | nA |
| Low Level Input Current | $I_{IL}$ | 3009 | $V_{IN}$ (Under Test)=0V<br>$V_{IN}$ (Remaining Inputs)=6V<br>$V_{DD}$=6V,$V_{SS}$=0V | - | -50 | nA |
| High Level Input Current | $I_{IH}$ | 3010 | $V_{IN}$ (Under Test)=6V<br>$V_{IN}$ (Remaining Inputs)=0V<br>$V_{DD}$=6V,$V_{SS}$=0V | - | 50 | nA |
| Low Level Output Voltage 1 | $V_{OL1}$ | 3007 | $V_{IL}$=0.3V, $V_{IH}$=1.5V,<br>$I_{OL}$=20µA<br>$V_{DD}$=2V, $V_{SS}$=0V | - | 100 | mV |
| Low Level Output Voltage 2 | $V_{OL2}$ | 3007 | $V_{IL}$=0.9V, $V_{IH}$=3.15V,<br>$I_{OL}$=20µA<br>$V_{DD}$=4.5V, $V_{SS}$=0V | - | 100 | mV |
| Low Level Output Voltage 3 | $V_{OL3}$ | 3007 | $V_{IL}$=1.2V, $V_{IH}$=4.2V,<br>$I_{OL}$=20µA<br>$V_{DD}$=6V, $V_{SS}$=0V | - | 100 | mV |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Low Level Output Voltage 4 | $V_{OL4}$ | 3007 | $V_{IL}$=0.9V, $V_{IH}$=3.15V, $I_{OL}$=4mA $V_{DD}$=4.5V, $V_{SS}$=0V | - | 260 | mV |
| Low Level Output Voltage 5 | $V_{OL5}$ | 3007 | $V_{IL}$=1.2V, $V_{IH}$=4.2V, $I_{OL}$=5.2mA $V_{DD}$=6V, $V_{SS}$=0V | - | 260 | mV |
| High Level Output Voltage 1 | $V_{OH1}$ | 3006 | $V_{IL}$=0.3V, $V_{IH}$=1.5V, $I_{OH}$=-20µA $V_{DD}$=2V, $V_{SS}$=0V | 1.9 | - | V |
| High Level Output Voltage 2 | $V_{OH2}$ | 3006 | $V_{IL}$=0.9V, $V_{IH}$=3.15V, $I_{OH}$=-20µA $V_{DD}$=4.5V, $V_{SS}$=0V | 4.4 | - | V |
| High Level Output Voltage 3 | $V_{OH3}$ | 3006 | $V_{IL}$=1.2V, $V_{IH}$=4.2V, $I_{OH}$=-20µA $V_{DD}$=6V, $V_{SS}$=0V | 5.9 | - | V |
| High Level Output Voltage 4 | $V_{OH4}$ | 3006 | $V_{IL}$=0.9V, $V_{IH}$=3.15V, $I_{OH}$=-4mA $V_{DD}$=4.5V, $V_{SS}$=0V | 3.98 | - | V |
| High Level Output Voltage 5 | $V_{OH5}$ | 3006 | $V_{IL}$=1.2V, $V_{IH}$=4.2V, $I_{OH}$=-5.2mA $V_{DD}$=6V, $V_{SS}$=0V | 5.48 | - | V |
| Threshold Voltage N-Channel | $V_{THN}$ | - | CLR Input at Ground All Other Inputs: $V_{IN}$=5V $V_{DD}$=5V, $I_{SS}$=-10µA | -0.45 | -1.45 | V |
| Threshold Voltage P-Channel | $V_{THP}$ | - | CLR Input at Ground All Other Inputs: $V_{IN}$=-5V $V_{SS}$=-5V, $I_{DD}$=10µA | 0.45 | 1.35 | V |
| Input Clamp Voltage (to $V_{SS}$) | $V_{IC1}$ | - | $I_{IN}$ (Under Test)= -0.1mA $V_{DD}$=Open, $V_{SS}$=0V All Other Pins Open | -400 | -900 | mV |
| Input Clamp Voltage (to $V_{DD}$) | $V_{IC2}$ | - | $I_{IN}$ (Under Test)= 0.1mA $V_{DD}$=0V, $V_{SS}$=Open All Other Pins Open | 400 | 900 | mV |
| Input Capacitance | $C_{IN}$ | 3012 | $V_{IN}$ (Not Under Test)=0V $V_{DD}$= $V_{SS}$=0V f = 100 kHz to 1 MHz Note 4 | - | 10 | pF |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Propagation Delay Low to High 1, $\overline{CLK}$ to QA | $t_{PLH1}$ | 3003 | $V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{DD}$=4.5V, $V_{SS}$=0V Note 5 | - | 30 | ns |
| Propagation Delay High to Low 1, $\overline{CLK}$ to QA | $t_{PHL1}$ | 3003 | $V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{DD}$=4.5V, $V_{SS}$=0V Note 5 | - | 30 | ns |
| Propagation Delay High to Low 2, CLR to QA | $t_{PHL2}$ | 3003 | $V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{DD}$=4.5V, $V_{SS}$=0V Note 5 | - | 42 | ns |
| Transition Time Low to High QA | $t_{TLH}$ | 3004 | $V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{DD}$=4.5V, $V_{SS}$=0V Note 5 | - | 15 | ns |
| Transition Time High to Low QA | $t_{THL}$ | 3004 | $V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{DD}$=4.5V, $V_{SS}$=0V Note 5 | - | 15 | ns |
| Maximum Clock Frequency | $f_{(CLK)}$ | - | Clock= Pulse Generator $V_{DD}$=4.5V,$V_{SS}$=0V Note 6,7 | 30 | - | MHz |

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at $T_{amb}$=+125 (+0 -5) $^{o}$C and $T_{amb}$=- 55(+5-0)$^{o}$C.

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table without Load $V_{IL}$=0.3V,$V_{IH}$=1.5V $V_{DD}$=2V,$V_{SS}$=0V $t_r$<1µs, Note 2 | - | - | - |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Functional Test 2 | - | 3014 | Verify Truth Table without Load<br>$V_{IL}$=0.9V,$V_{IH}$=3.15V<br>$V_{DD}$=4.5V,$V_{SS}$=0V<br>$t_r$=$t_f$<500ns<br>Note 2 | - | - | - |
| Functional Test 3 | - | 3014 | Verify Truth Table without Load<br>$V_{IL}$=1.2V,$V_{IH}$=4.2V<br>$V_{DD}$=6V,$V_{SS}$=0V<br>$t_r$=$t_f$<400ns<br>Note 2 | - | - | - |
| Quiescent Current | $I_{DD}$ | 3005 | $V_{IL}$=0V,$V_{IH}$=6V<br>$V_{DD}$=6V,$V_{SS}$=0V<br>All Outputs Open<br>Note 3 | - | 8 | µA |
| Low Level Input Current | $I_{IL}$ | 3009 | $V_{IN}$ (Under Test)=0V<br>$V_{IN}$ (Remaining Inputs)=6V<br>$V_{DD}$=6V,$V_{SS}$=0V | - | -1 | µA |
| High Level Input Current | $I_{IH}$ | 3010 | $V_{IN}$ (Under Test)=6V<br>$V_{IN}$ (Remaining Inputs)=0V<br>$V_{DD}$=6V,$V_{SS}$=0V | - | 1 | µA |
| Low Level Output Voltage 1 | $V_{OL1}$ | 3007 | $V_{IL}$=0.3V, $V_{IH}$=1.5V,<br>$I_{OL}$=20µA<br>$V_{DD}$=2V, $V_{SS}$=0V | - | 100 | mV |
| Low Level Output Voltage 2 | $V_{OL2}$ | 3007 | $V_{IL}$=0.9V, $V_{IH}$=3.15V,<br>$I_{OL}$=20µA<br>$V_{DD}$=4.5V, $V_{SS}$=0V | - | 100 | mV |
| Low Level Output Voltage 3 | $V_{OL3}$ | 3007 | $V_{IL}$=1.2V, $V_{IH}$=4.2V,<br>$I_{OL}$=20µA<br>$V_{DD}$=6V, $V_{SS}$=0V | - | 100 | mV |
| Low Level Output Voltage 4 | $V_{OL4}$ | 3007 | $V_{IL}$=0.9V, $V_{IH}$=3.15V,<br>$I_{OL}$=4mA<br>$V_{DD}$=4.5V, $V_{SS}$=0V | - | 400 | mV |
| Low Level Output Voltage 5 | $V_{OL5}$ | 3007 | $V_{IL}$=1.2V, $V_{IH}$=4.2V,<br>$I_{OL}$=5.2mA<br>$V_{DD}$=6V, $V_{SS}$=0V | - | 400 | mV |
| High Level Output Voltage 1 | $V_{OH1}$ | 3006 | $V_{IL}$=0.3V, $V_{IH}$=1.5V,<br>$I_{OH}$=-20µA<br>$V_{DD}$=2V, $V_{SS}$=0V | 1.9 | - | V |
| High Level Output Voltage 2 | $V_{OH2}$ | 3006 | $V_{IL}$=0.9V, $V_{IH}$=3.15V,<br>$I_{OH}$=-20µA<br>$V_{DD}$=4.5V, $V_{SS}$=0V | 4.4 | - | V |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| High Level Output Voltage 3 | $V_{OH3}$ | 3006 | $V_{IL}$=1.2V, $V_{IH}$=4.2V, $I_{OH}$=-20µA $V_{DD}$=6V, $V_{SS}$=0V | 5.9 | - | V |
| High Level Output Voltage 4 | $V_{OH4}$ | 3006 | $V_{IL}$=0.9V, $V_{IH}$=3.15V, $I_{OH}$=-4mA $V_{DD}$=4.5V, $V_{SS}$=0V | 3.7 | - | V |
| High Level Output Voltage 5 | $V_{OH5}$ | 3006 | $V_{IL}$=1.2V, $V_{IH}$=4.2V, $I_{OH}$=-5.2mA $V_{DD}$=6V, $V_{SS}$=0V | 5.2 | - | V |
| Input Clamp Voltage (to $V_{SS}$) | $V_{IC1}$ | - | $I_{IN}$ (Under Test)= -0.1mA $V_{DD}$=Open, $V_{SS}$=0V All Other Pins Open | -0.1 | -1.2 | V |
| Input Clamp Voltage (to $V_{DD}$) | $V_{IC2}$ | - | $I_{IN}$ (Under Test)= 0.1mA $V_{DD}$=0V, $V_{SS}$=Open All Other Pins Open | 0.1 | 1.2 | V |

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Functional tests shall be performed with f = 10 kHz (min). The Maximum time to output comparator strobe=30µs.
3. Quiescent Current shall be tested using the following input conditions:
   (a) CLR = $V_{IH}$ ; $\overline{CLK}$ = $V_{IL}$
   (b) CLR = $V_{IL}$ ; $\overline{CLK}$ = $V_{IL}$
   (c) CLR = $V_{IL}$ ; 2047 pulses applied to $\overline{CLK}$ to configure outputs QA to QK to a high level.
   (d) CLR = $V_{IL}$ ; 2047 additional pulses applied to $\overline{CLK}$ to configure outputs QA to QL to a high level.
4. Guaranteed but not tested.
5. Measurements shall be performed as a go-no-go test on a 100% basis. Read and record measurements shall be performed on a sample of 5 components.
   The pulse generator shall have the following characteristics:
   $V_{GEN}$ = 0 to $V_{DD}$; f = 1 MHz minimum; $t_r$ and $t_f \leq$ 6 ns (10% to 90%); duty cycle = 50%; $Z_{out}$ = 50Ω
   Output load capacitance $C_L$ = 50pF ± 5% including scope probe, wiring and stray capacitance without component in the test fixture.
   Propagation delay shall be measured referenced to the 50% input and output voltages.
   Transition time shall be measured referenced to the 10% and 90% output voltage.
6. Read and record measurements shall be performed on a sample of 5 components.
7. A pulse, having the following conditions, shall be applied to the clock input: $V_P$ = 0V to $V_{DD}V_{dc}$.
   Maximum clock frequency $f_{(CLK)}$ requirement shall be considered as met if proper output state changes occur with the pulse repetition rate set to that given in the “Limits” column.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{amb}$ =+22±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Electrical Measurements at Room Temperature.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|---|---|---|---|---|---|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Quiescent Current | $I_{DD}$ | ±120 | - | 400 | nA |
| Low Level Input Current | $I_{IL}$ | ±20 | - | -50 | nA |
| High Level Input Current | $I_{IH}$ | ±20 | - | 50 | nA |
| Low Level Output Voltage 4 | $V_{OL4}$ | ±26 | - | 260 | mV |
| High Level Output Voltage 4 | $V_{OH4}$ | ±0.2 | 3.98 | - | V |
| Threshold Voltage N-Channel | $V_{THN}$ | ±0.3 | -0.45 | -1.45 | V |
| Threshold Voltage P-Channel | $V_{THP}$ | ±0.3 | 0.45 | 1.35 | V |

**NOTES:**
Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{amb}$ =+22±3$^{o}$C.

The test methods and test conditions shall be as per the corresponding test defined in Electrical Measurements at Room Temperature.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|---|---|---|---|---|---|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Functional Test 1 | - | - | - | - | - |
| Functional Test 2 | - | - | - | - | - |
| Functional Test 3 | - | - | - | - | - |
| Quiescent Current | $I_{DD}$ | ±120 | - | 400 | nA |
| Low Level Input Current | $I_{IL}$ | ±20 | - | -50 | nA |
| High Level Input Current | $I_{IH}$ | ±20 | - | 50 | nA |
| Low Level Output Voltage 4 | $V_{OL4}$ | ±26 | - | 260 | mV |
| Low Level Output Voltage 5 | $V_{OL5}$ | ±26 | - | 260 | mV |
| High Level Output Voltage 4 | $V_{OH4}$ | ±0.2 | 3.98 | - | V |
| High Level Output Voltage 5 | $V_{OH5}$ | ±0.2 | 5.48 | - | V |
| Threshold Voltage N-Channel | $V_{THN}$ | ±0.3 | -0.45 | -1.45 | V |
| Threshold Voltage P-Channel | $V_{THP}$ | ±0.3 | 0.45 | 1.35 | V |

**NOTES:**
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.

## 2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

### 2.6.1 N-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +125 (+0 -5) | $^{o}C$ |
| Outputs Q | $V_{OUT}$ | Open or $V_{SS}$ | - |
| Inputs $\overline{CLK}$, CLR | $V_{IN}$ | $V_{SS}$ | V |
| Positive Supply Voltage | $V_{DD}$ | 6 (+0 -0.5) | V |
| Negative Supply Voltage | $V_{SS}$ | 0 | V |
| Duration | t | 72 | Hours |

**NOTES:**
1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.6.2 P-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +125 (+0 -5) | $^{o}C$ |
| Outputs Q | $V_{OUT}$ | Open or $V_{DD}$ | - |
| Inputs $\overline{CLK}$, CLR | $V_{IN}$ | $V_{DD}$ | V |
| Positive Supply Voltage | $V_{DD}$ | 6 (+0 -0.5) | V |
| Negative Supply Voltage | $V_{SS}$ | 0 | V |
| Duration | t | 72 | Hours |

**NOTES:**
1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.7 POWER BURN-IN CONDITIONS

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +125 (+0 -5) | $^{o}C$ |
| Outputs Q | $V_{OUT}$ | $V_{DD}$ | V |
| Input CLR | $V_{IN}$ | $V_{SS}$ | V |
| Input $\overline{CLK}$ | $V_{IN}$ | $V_{GEN}$ | V |
| Pulse Voltage | $V_{GEN}$ | 0V to $V_{DD}$ | V |
| Pulse Frequency Square Wave | $f_{GEN}$ | 100k ± 10%<br>50 ± 15% Duty Cycle<br>$t_r=t_f\leq400ns$ | Hz |
| Positive Supply Voltage | $V_{DD}$ | 6 (+0 -0.5) | V |
| Negative Supply Voltage | $V_{SS}$ | 0 | V |

**NOTES:**
1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for power burn-in.

2.9 TOTAL DOSE RADIATION TESTING

2.9.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the purchase order.

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | + 22 ± 3 | $^{o}C$ |
| Outputs Q | $V_{OUT}$ | Open | - |
| Inputs $\overline{CLK}$,CLR | $V_{IN}$ | $V_{DD}$ | V |
| Positive Supply Voltage | $V_{DD}$ | 6 ± 0.3 | V |
| Negative Supply Voltage | $V_{SS}$ | 0 | V |

**NOTES:**
1. Input Protection Resistor = 680Ω min to 47kΩ max.

2.9.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at $T_{amb}$ = +22 ± 3°C.
The test methods and test conditions shall be as per the corresponding test defined in Electrical Measurements at Room temperature.

The parameters to be measured during and on completion of irradiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

| Characteristics | Symbols | Limits | | | Units |
|---|---|---|---|---|---|
| | | Drift Values Δ | Absolute | | |
| | | | Min | Max | |
| Quiescent Current | $I_{DD}$ | - | - | 40 | µA |
| Threshold Voltage N-Channel | $V_{THN}$ | ±0.6 | -0.4 | -1.5 | V |
| Threshold Voltage P-Channel | $V_{THP}$ | ±0.6 | 0.4 | 1.4 | V |

**APPENDIX 'A'**

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|---|---|
| Deviations from Screening Tests - Chart F3 | External Visual Inspection: The criteria applicable to chip out are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).<br><br>High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.<br><br>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255. |
| Deviations from Qualification and Periodic Tests - Chart F4 | External Visual Inspection: The criteria applicable to chip out are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).<br><br>Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. |
| Deviations from Electrical Measurements at High and Low Temperatures | Electrical Measurements at High and Low Temperatures may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperature Electrical Measurements per the detail specification.<br><br>A summary of the pilot lot testing shall be provided if required by the purchase order. |
| Deviations from Room Temperature Electrical Measurements | All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the detail specification.<br><br>A summary of the pilot lot testing shall be provided if required by the purchase order. |