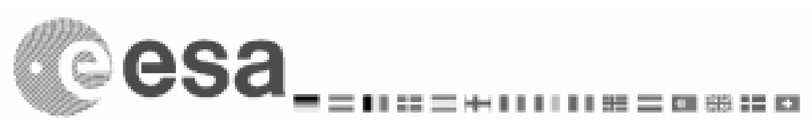
INTERNAL VISUAL INSPECTION

OF INTEGRATED CIRCUITS

ESCC Basic Specification No. 2049000

ISSUE 1

October 2002



Document Custodian: European Space Agency - see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

European Space Agency, Copyright © 2002. All rights reserved.

The European Space Agency disclaims any liability or responsibility, to any person or entity, with respect to any loss or damage caused, or allleged to be caused, directly or indirectly by the use and application of this ESCC publication.

This publication, without the prior permission of the European Space Ageny and provided that it is not used for a commercial purpose, may be:

- copied in whole in any medium without alteration or modification.
- copied in part, in any medium, provided that the ESCC document identification, comprising the ESCC symbol, document number and document issue, is removed.

european space agency
agence spatiale européenne

Pages 1 to 47

INTERNAL VISUAL INSPECTION

OF INTEGRATED CIRCUITS

ESA/SCC Basic Specification No. 2049000

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	May 1992	[signature]	[signature]

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.

TABLE OF CONTENTS

		Page
1.	**SCOPE**	5
2.	**GENERAL REQUIREMENTS**	5
2.1	Applicability	5
2.2	Procedure	5
2.3	Magnification	5
2.4	Mounting Fixtures	5
3.	**DETAILED REQUIREMENTS**	5
3.1	General	5
3.2	Sequence of Inspection	6
3.3	Definitions	6
4.	**TEST CRITERIA**	9
4.1	Metallisation Defects, "High Magnification"	10
4.1.1	Metallisation Scratches	10
4.1.2	Metallisation Voids	11
4.1.3	Metallisation Corrosion	13
4.1.4	Metallisation Non-adherence	13
4.1.5	Metallisation Probing	13
4.1.6	Metallisation Bridging	13
4.1.7	Metallisation Alignment	13
4.1.8	Excess Metallisation on Back Face Metallisation	14
4.1.9	GaAs Back Face Metallisation	14
4.2	Diffusion Faults, "High Magnification"	16
4.3	Passivation Layer(s) Faults, "High Magnification"	17
4.4	Glassivation Defects, "High Magnification"	18
4.5	Dielectric Isolation, "High Magnification"	19
4.6	Film Resistor, "High Magnification"	20
4.7	Laser Trimmed Thin Film Resistors, "High Magnification"	22
4.8	Scribing and Die Defects, "High Magnification"	26
4.9	Bond Inspection, "Low Magnification"	30
4.9.1	General	30
4.9.2	Wedge Bonds	33
4.9.3	Tailless Bonds	34
4.9.4	Gold Ball Bonds	34
4.9.5	Rebonds	36
4.9.6	Beam Lead	36
4.10	Internal Leads, "Low Magnification"	39
4.10.1	Wires	39
4.10.2	Beam Lead Construction	40
4.10.3	Up-Bonding	41
4.10.4	Down-Bonding	41
4.11	Die Mounting	44
4.11.1	Die Mounting, "Low Magnification", Eutectic	44
4.11.2	Die Mounting, "Low Magnification", Non-eutectic, Inorganic	44
4.11.3	Die Orientation	46
4.11.4	Insulating Island Mounting Defects	46
4.12	Foreign Material	46
4.13	Package, Header or Can Defects	47

TABLES Page

I	Magnification Checklist	9

FIGURES

I	Scratch Criteria	10
II	Void Criteria	11
III	MOS Scratch and Void Criteria	12
IV	Bond Pad Terminology	13
V	MOS Gate Alignment	15
VI	Diffusion Faults	16
VII	Passivation Faults	17
VIII	Laser Trimmed Glassivation Defects	18
IX	Dielectric Isolation Defects	19
X	Scratch and Void Criteria for Untrimmed Resistors	20
XI	Thin Film Resistor Contact Area	21
XII	Laser Trimmed Thin Film Resistors	23
XIII	Scratch and Void Criteria for Trimmed Resistors	24
XIV	Block Resistor Criteria	25
XV	Scribing and Die Defects	27
XVI	Beam Lead Die Defaults	28
XVII	Scribing and Die Defects	29
XVIII	Bond Dimensions	31
XIX	Bonds at Metallisation Exit	32
XX	Torn and Incomplete Bonds	34
XXI	Ball Bonds	35
XXII	Beam Lead Bond Area and Location	37
XXIII	Criteria for Wire(s) Crossing Wire(s)	38
XXIV	Loop Between Double Bond	40
XXV	Up-Bonding	42
XXVI	Down-Bonding	43
XXVII	Balling of Die Attach Material	45

1. SCOPE

This specification, to be read in conjunction with ESA/SCC Basic Specification No. 20400 (Internal Visual Inspection), contains additional requirements for integrated circuits which shall be applied to each device. An integrated circuit is defined as a microcircuit consisting exclusively of elements formed in situ on, or within, a single semiconductor substrate with at least one of the elements formed within the substrate. The inspection limit, using optical microscopy, is a line width of 1μm. For line widths $<2\mu m$ the track separation must be $\geq 3\mu m$ to ensure adequate optical resolution.

2. GENERAL REQUIREMENTS

2.1 APPLICABILITY

The following criteria may not be varied or modified after commencing any inspection stage. Any ambiguity or proposed minor deviation shall be referred to the Qualifying Space Agency for resolution and approval.

2.2 PROCEDURE

All components shall be submitted to examination immediately prior to sealing or encapsulation, or immediately after decapping, in an area where the standard of cleanliness is not less than that of the assembly area.

All items shall be examined in such a manner that a minimum of handling and movement of the component is involved.

2.3 MAGNIFICATION

"High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface.

"Low magnification" inspection shall be performed with either a monocular, binocular, or stereomicroscope, and the inspection performed within an angle of 30° from the perpendicular to the die surface with the device under suitable illumination.

2.4 MOUNTING FIXTURES

Suitable fixtures may be used to assist in the inspection process provided they do not in themselves cause damage to the device.

3. DETAILED REQUIREMENTS

3.1 GENERAL

The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable Detail Specification. The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device, process or technology, it has been indicated. A component shall be rejected if it exhibits one or more of the defects listed within this specification.

The lot inspected shall be homogeneous. A component shall therefore also be rejected if it exhibits a significant deviation, within the limits of this specification, from the rest of the lot. However, such components shall not be counted as a failure in any other lot definition.

3.2 SEQUENCE OF INSPECTION

The order in which the criteria are presented is not a required order of examination and may be varied at the discretion of the Manufacturer, or Inspector.

When inverted die mounting techniques are employed, or for VLSI devices, the inspection criteria that cannot be performed after mounting shall be conducted prior to attachment of the die.

3.3 DEFINITIONS

Active Circuit Area: all areas of functional circuit elements, operating metallisation or any connected combinations, excluding beam leads.

Block Resistor: a thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and which shall be identified in the approved Manufacturer's pre-encapsulation visual implementation document.

Channel: an area lying between the drain and the source of FET structures.

Contact Window: an opening in the passivation, usually covered by metallisation, where electrical contact is made with an underlying layer.

Coupling (Air) Bridge: a raised layer of metallisation used for interconnection that is isolated from the surface of the die.

Crazing: the presence of numerous minute cracks in the referenced material.

Detritus: fragments of original or laser modified resistor material remaining in the kerf.

Dielectric Isolation: electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolation barrier such as semiconductor oxide.

Diffusion Well: a volume (or region) formed in a semiconductor material by a diffusion process (n- or p- type) and isolated from the surrounding semiconductor material by a n-p or p-n junction or by a dielectric material (dielectric isolation, coplanar process, SOS, SOI).

Down Bonding: a wire bonding operation carried out from the die down to the post.

Foreign Material: any material that is foreign to the microcircuit or package, or any non-foreign material that is displaced from its original or intended position within the microcircuit package. Foreign material shall be considered to be attached when it cannot be removed by a gas blow of nitrogen at 140kPa applied for a minimum of three seconds from a distance of 50mm. The diameter of the nozzle shall not be less than 1mm in diameter.

- Conductive foreign material: any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection.

- Particles: embedded in the glassivation when there is evidence of colour fringing around the periphery of the particle.

Functional Circuit Elements: diodes, transistors, cross-unders, capacitors, and resistors.

Gate Oxide: the oxide, or other dielectric, that separates gate metallisation (or other material used for the gate electrode) from the channel of MOS structures.

Glassivation: the top layer(s) of transparent insulating material that covers the active circuit area including metallisation, except bonding pad areas and beam leads.

Glassivation Cracks: fissures in the glassivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallised areas.

Hybrid Microcircuit: a microcircuit consisting of elements which are a combination of film microcircuit type and the semiconductor types, or a combination of one or both of the types with discrete parts. Hybrids do not fall within the scope of this specification but are defined to clarify the limits of the document.

Inverted Mounting: a technique whereby thickened, extended, bonding pads enables upside down mounting on a suitable substrate, such as thin/thick film.

Junction: the outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material. An active junction is any p/n junction intended to conduct current during normal operation of the circuit element (i.e. collector to base).

Kerf: that portion of the component area from which material has been removed or modified by trimming or cutting.

Line of Separation: the visible distance or space between two features that are observed not to touch at the magnification in use.

Metal Semiconductor Field Effect Transistor (MESFET): a FET in which the metal semiconductor rectifying contact is used for the gate electrode. Typically the structure is fabricated in gallium arsenide and the term GaAs MESFET may be used. Both depletion (D-MESFET) and enhancement (E-MESFET) type devices have been manufactured.

Metallisation Non-adherance: unintentional separation of material from an underlying substance, excluding air bridges, and undercutting by design.

Multilayered Metallisation (Conductors): two or more layers of metal or any other material used for interconnections that are not isolated from each other by insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

Multilevel Metallisation (Conductors): two or more layers of metal or any other material used for interconnections that are isolated from each other by insulating material (also referred to as interlevel dielectric).

Narrowest Resistor Width: the narrowest portion of a given resistor prior to trimming.

Operating Metallisation (Conductors): all metal or any other material used for interconnection except metallised scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.

Original Width: the width dimension or distance that is intended by design (e.g., original metal width, original diffusion width, original beam width, etc.).

Package Post: a generic term used to describe the bonding location on the package.

Passivation: the silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal, or between metal levels on multilevel devices.

Passivation Step: an abrupt change of level of the passivation, such as a contact window, or operating metallisation cross over.

Peripheral Metal: all metal that lies immediately adjacent to, or over, the scribe grid.

Rebond: a second bond made between two pads, or a pad and a bonding terminal, to replace the original bonded wire, which has either been removed, leaving the welded portion of the bond attached to the pad or bonding terminal, or which failed to adhere at the first bonding attempt.

Scratch: any tearing defect, discontinuity or tooling mark in or on the metallisation, detected at the specified power, whether or not the bare semiconductor material and/or the oxide is exposed. Probe marks in the surface of the metallisation are considered as scratches.

Shooting Metal: defined as metal (e.g. aluminium, gold) expulsion of various shapes and lengths from under the wire bond at the bonding pad.

Substrate: the supporting structural material into and/or upon which the passivation, metallisation and circuit elements are placed.

Substrate Via: a small hole formed through the wafer and metallised, causing electrical connection to be made from the side of the wafer on which the circuitry is formed, to the back face of the wafer.

Thick film: that conductive/resistive/dielectric system that is a film greater than 5µm thick.

Thin Film: that conductive/resistive/dielectric system that is a film equal to or less than 5 µm thick.

Up Bonding: a wire bonding operation carried out from the die up to the post.

Via metallisation: that which connects the metallisation of one level to another.

Void: any region in the metallisation, not caused by a scratch,where bare semiconductor material or passivation is visible within the design areas of the metallisation.
In the case of die mounting, a void is the absence of die attach material in the defined areas.
In the case of glassivation, a void is the absence of glassivation over any active circuit area of the die.

4. TEST CRITERIA

The internal visual examination shall be conducted on each microcircuit and each integrated circuit chip. The requirements contained in Paras. 4.4, 4.5 and 4.6 shall apply to appropriate microcircuit areas where glassivation, dielectric isolation or film resistors are used.

GaAs devices shall be inspected to all of the applicable criteria. High power magnification for individual features of GaAs microwave devices shall be dependent on the feature size.

TABLE I - MAGNIFICATION CHECKLIST

The following magnifications are given as a guideline only. For line widths, below 1.5µm, or where additional verification is required, increased magnification to 1000X may be used, if necessary.

DEFECT	MAGNIFICATION	PARA.
Metallisation Defects	100X - 400X	4.1
Diffusion Faults	100X - 400X	4.2
Passivation Layer(s) Faults	100X - 400X	4.3
Glassivation Defects	100X - 200X	4.4
Dielectric Isolation	100X - 200X	4.5
Film Resistor	100X - 200X	4.6
Laser Trimmed Thin Film Resistor	100X - 200X	4.7
Scribing and Die Defects	100X - 200X	4.8
Bond Inspection	30X - 60X	4.9
Internal Leads	30X - 60X	4.10
Die Mounting	30X - 60X	4.11
Foreign Material, Die Inspections	100X - 400X	4.12
Foreign Material, Lid Inspections	30X - 60X	
Package, Header or Can Defects	As Required	4.13

4.1 METALLISATION DEFECTS, "HIGH MAGNIFICATION"

No device shall be acceptable that exhibits the following defects in the operating metallisation:

4.1.1 Metallisation Scratches

(a) Scratch in the metallisation excluding bonding pads and beam leads that leaves less than 50% of the original metal width undisturbed (See Figure I). For GaAs microwave devices, scratches in the gate stripe or gate insertion metallisation.

(b) Scratch in the metallisation over a passivation step that leaves less than 75% of the original metal width at the step undisturbed.

(c) Scratch in the bonding pad or fillet area that reduces the metallisation path width connecting the bond to the interconnecting metallisation to less than 50% of the narrowest entering interconnect metallisation stripe width (See Figure IV). If two or more stripes enter a bonding pad, each shall be considered separately.

(d) Scratch in the metallisation, over the gate oxide (See Figure III), applicable to MOS structures.

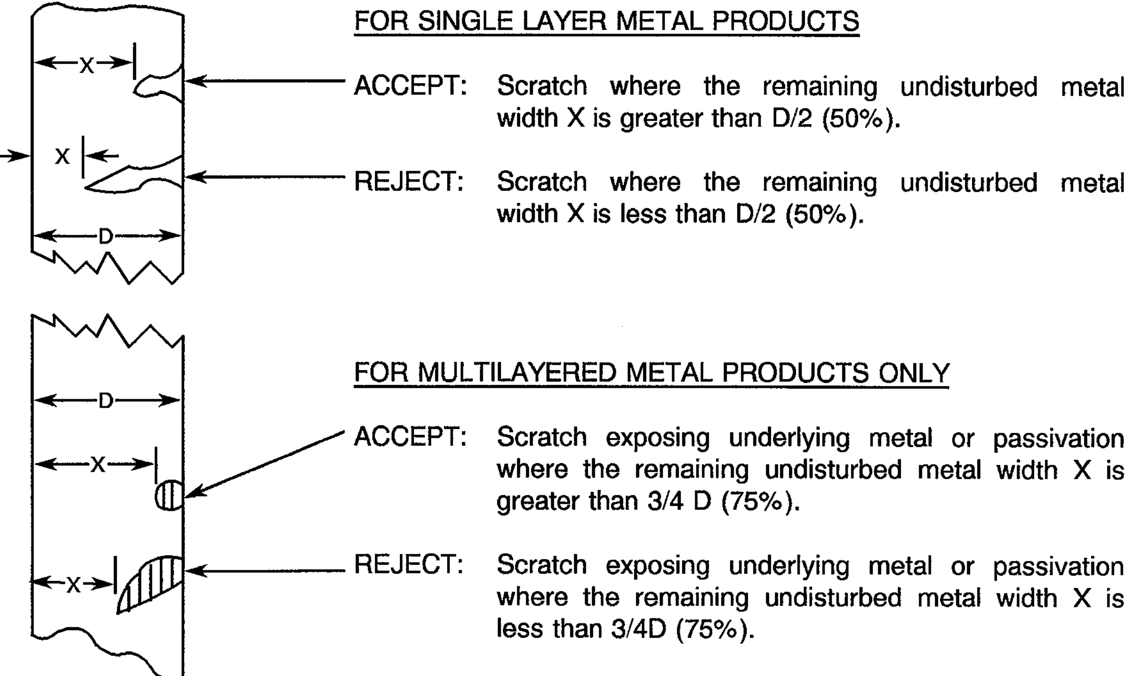
(e) Scratch in multilayered metallisation excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75% of the original metal width undisturbed (See Figure I).

(f) Scratch, probe marks, etc., in the bonding pad area that exposes underlying passivation or substrate, and leaves less than 75% of the unglassivated metallisation area undisturbed.

(g) Scratch in the metallisation that exposes the dielectric material of a thin film capacitor or cross over (not applicable to air bridges).

(h) For GaAs devices, any tear in the air bridge, or a scratch, that lowers the air bridge arch over active metallisation.

FIGURE I - SCRATCH CRITERIA



4.1.2 Metallisation Voids

(a) Void(s) in the metallisation that leaves less than 75% of the original metal width undisturbed (See Figure II).

(b) Void(s) in the metallisation over a passivation step that leaves less than 75% of the original metal width, at the step, undisturbed (See Figure II).

(c) Void(s) in the metallisation over the gate oxide that leaves less than 75% of the metallisation length (L) or width (W) between source and drain diffusions undisturbed (See Figure III), applicable to MOS structures.

(d) Void(s) that leave less than 75% of the metallisation area over the gate oxide undisturbed, applicable to MOS structures.

(e) Void(s) in the bonding pad area that leaves less than 75% of its original unglassivated metallisation area undisturbed.

(f) Void(s) in the bonding pad or fillet area that reduces the metallisation path width connecting the bond to the interconnecting metallisation to less than 75% of the narrowest entering metallisation stripe width (See Figure 4). If two or more stripes enter a bonding pad, each shall be considered separately. When a fillet area exists, it is considered as part of the entering/exiting metallisation stripe.

(g) Void(s) in the metallisation area of a thin film capacitor that leave less than 75% of the designed metallisation area undisturbed.

(h) For GaAs microwave devices, voids in the gate stripe.

(i) Void(s), or missing metallisation on the back face metallisation, where applicable, where the defective area is greater than 20%.

FIGURE II - VOID CRITERIA

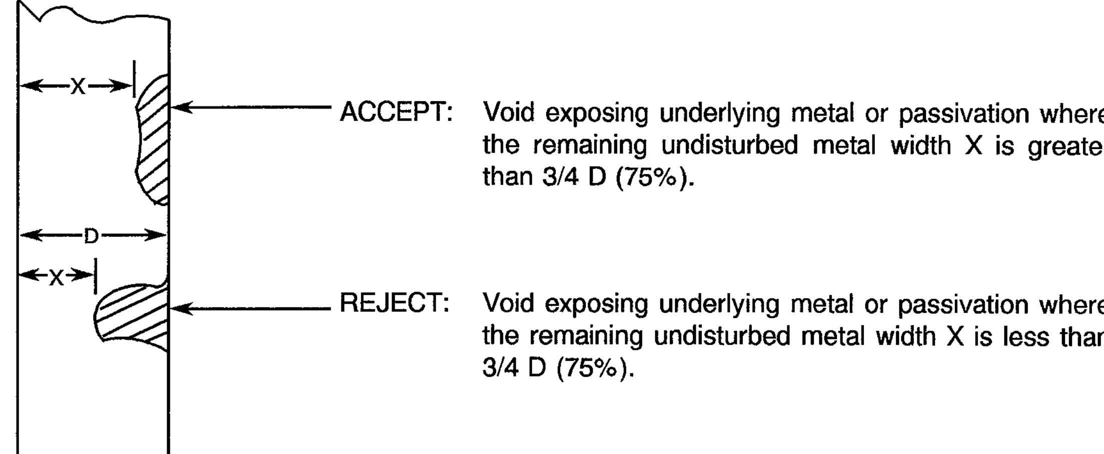
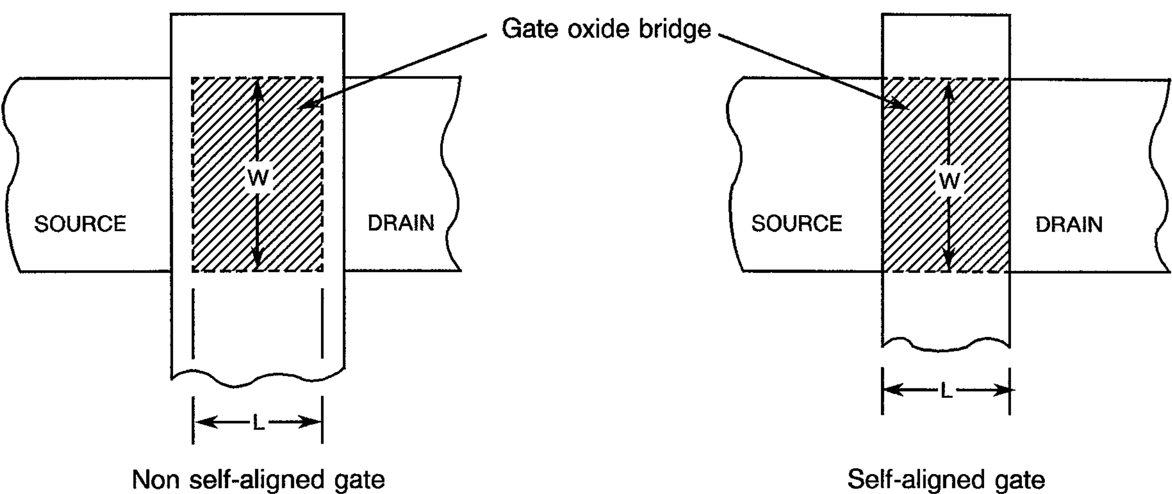
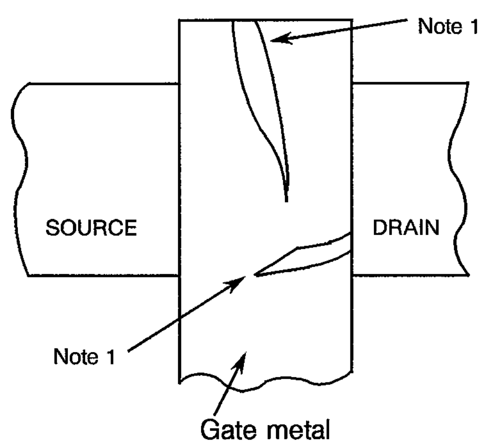


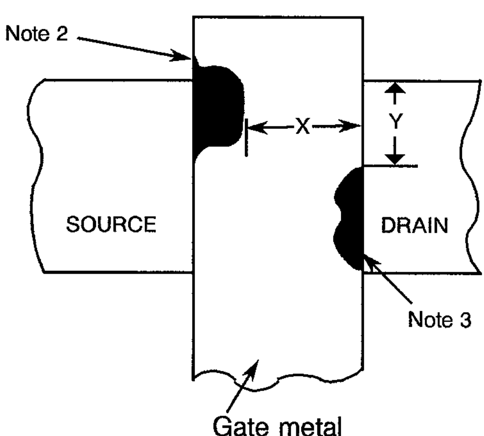
FIGURE III - MOS SCRATCH AND VOID CRITERIA



NOTES

1. When standard metallisation scratch and void criterion is applied to the gate area, the dimensions W and L shall be considered as the original channel width and length respectively.

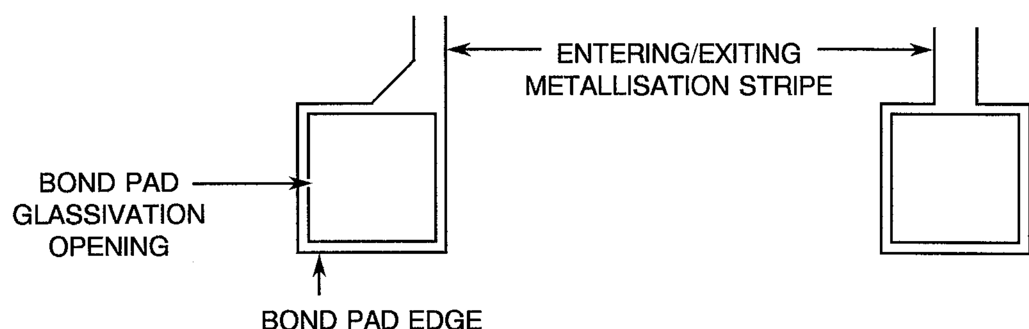




NOTES

1. REJECT: Scratch(es) in the metallisation over the gate oxide.
2. REJECT: Void exposing underlying oxide where the remaining undisturbed metal width X is less than 3/4L (75%).
3. REJECT: Void exposing underlying oxide where the remaining undisturbed metal width Y is less than 3/4W (75%).

FIGURE IV - BOND PAD TERMINOLOGY



4.1.3 Metallisation Corrosion

Any metallisation corrosion. Metallisation having any localised discoloured area shall be closely examined and rejected unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.

4.1.4 Metallisation Non-adherence

Any metallisation lifting, peeling, or blistering.

4.1.5 Metallisation Probing

Criteria contained in Para. 4.1.1 shall apply as limitations on probing damage.

4.1.6 Metallisation Bridging

(a) Any metallisation bridging where the separation between metallisation paths is reduced to less than 50% of the original design.

(b) Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) if it reduces the original separation between unglassivated operating metallisation, or scribe line and the bonding pad, to less than 6.25µm or 50% of the design separation, whichever is less.

(c) For GaAs devices, gate metallisation which is designed with the gate stripe offset to the side; this criteria shall apply only to the side with the large offset. If a clear line of separation is not discernable, device functional testing at wafer level shall suffice.

4.1.7 Metallisation Alignment

(a) Contact window that has less than 75% of its area covered by metallisation.

(b) Contact window that has less than a continuous 50% of its perimeter covered by metallisation.

(c) Contact window that has less than 75% of its perimeter on two adjacent sides covered by metallisation, applicable to MOS structures.

NOTES

1. When, by design, metal is completely contained in a contact window or does not cover the entire contact perimeter, the criteria defined in alineas (a), (b) and (c) for perimeter coverage can be deleted.

(d) A metallisation path not intended to cover a contact window that is not separated from the contact window by a line of separation.

(a) Any exposure of the gate oxide, i.e. oxide not covered by gate electrode in the area between source to drain diffusions, applicable to MOS structures (See Figure V).

(b) Any exposure of the gate oxide bridge that leaves less than 75% of the metallisation coincident with the source and drain diffusion junction line undisturbed, applicable to MOS structures.

(c) For MOS structures containing a diffused guard ring, gate metallisation not coincident with, or extending over, the diffused guard ring (See Figure V).

4.1.8 Excess Metallisation on Back Face Metallisation

Remaining metallisation on the back face of monolithic beam lead devices, likely to result in a short circuit.

4.1.9 GaAs Back Face Metallisation

GaAs inspection shall be performed with low magnification. (Verification at high magnification is permitted). No devices shall be acceptable that exhibit the following.

(a) Evidence of metal corrosion, lifting, peeling, blistering.

(b) Voids or scratches that expose underlying metal or substrate whose cumulative areas are more than 25% of the cell area or device area.

NOTES

1. Absence of gold in the die separation area (saw street) of devices with electroplated back face metallisation is not a cause for rejection. Small voids at edges due to die separation are acceptable if they comprise less than 10% of the back face area.

(c) Any voids or scratches in the substrate via metallisation that affects more than 25% of the metallisation, or cause unintended isolation of the metallisation path.

FIGURE V - MOS GATE ALIGNMENT

ACCEPT

Field oxide line
SOURCE
DRAIN
Field oxide line

REJECT

Note 1
SOURCE
DRAIN
Field oxide line

Gate:
Self-aligning

ACCEPT

SOURCE
DRAIN

REJECT

Note 1
SOURCE
DRAIN

Metal gate:
Non self-aligning

ACCEPT

SOURCE
DRAIN

REJECT

Note 2
SOURCE
DRAIN

Guard ring
Guard ring
Metal gate

NOTES

1. REJECT: Gate oxide exposed from source to drain.
2. REJECT: Gate does not coincide with, or extend over, the guard ring.

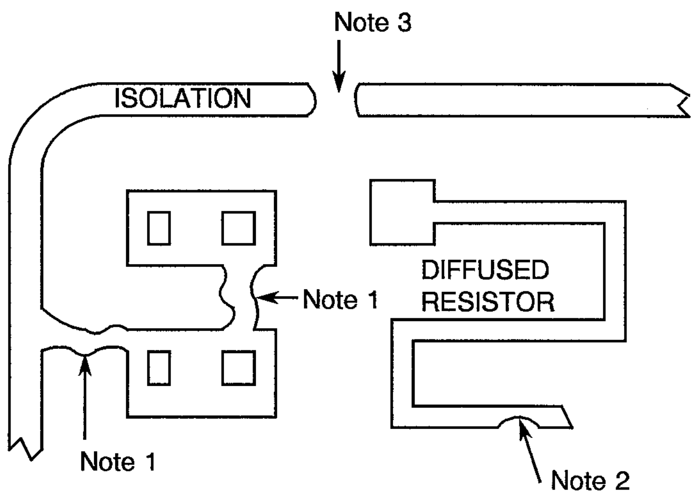
4.2 DIFFUSION FAULTS, "HIGH MAGNIFICATION"

No device shall be acceptable that exhibits the following:

(a) Any diffusion fault that allows bridging between diffused areas (See Figure VI).

(b) Any isolation diffusion that is discontinuous (except isolation walls around unused areas or unused bonding pads) or any other diffused area with less than 25% (50% for resistors) of the original diffusion width that remains (See Figure VI).

FIGURE VI - DIFFUSION FAULTS



NOTES
1. REJECT: Diffusion fault between diffused areas.
2. REJECT: Diffused resistor with less than 50% of the original width remaining.
3. REJECT: Discontinuous isolation diffusion.

4.3 PASSIVATION LAYER(S) FAULTS, "HIGH MAGNIFICATION"

No device shall be acceptable that exhibits the following:

(a) Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallisation, (See Figure VII). Multiple lines indicate that the fault can have sufficient depth to penetrate down to bare semiconductor material, unless by design for GaAs devices.

This criteria can be excluded when a second passivation layer is applied in a separate operation prior to metallisation disposition, or for bond pads located in isolation tubs.

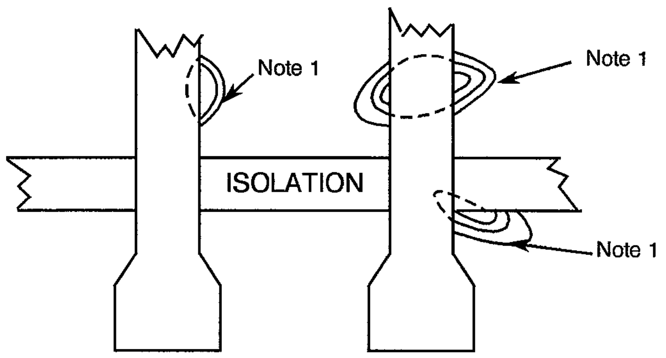
(b) Active junction not covered by passivation, unless in accordance with the design specification.

(c) Contact window that extends across a junction line, unless in accordance with the design specification.

(d) A passivation defect which causes unintentional opens or shorts in the active area.

(e) Subsurface scratch, below the passivation, where the passivation remains undamaged.

FIGURE VII - PASSIVATION FAULTS



NOTES

1. REJECT: Passivation defect under metallisation.

4.4 GLASSIVATION DEFECTS, "HIGH MAGNIFICATION"

No device shall be acceptable that exhibits (see Figure VIII):

(a) Glass crazing or glass damage that prohibits detection of the visual criteria contained within this document.

(b) Any lifting or peeling of the glassivation in the active areas, or which extends more than 25μm distance from the designed periphery of the glassivation.

(c) A glassivation void that exposes two, or more, active metallisation paths, unless in accordance with the design specification.

(d) Unglassivated areas greater than 125μm in any dimension, unless in accordance with the design specification.

(e) Unglassivated areas at the edge of the bonding pad exposing bare semiconductor material, unless by design.

(f) Glassivation covering more than 25% of the designed, open contact, bonding pad area.

(g) Crazing over a film resistor.

(h) Scratch(es) in the glassivation that disturbs metal, and bridges metallisation paths.

(i) Cracks (not crazing) in the glassivation that form a closed loop over adjacent metallisation paths.

(j) Glassivation void(s) that expose any portion of a thin film resistor or fusible link except where the glassivation is opened by design.

(k) For GaAs devices, voids in the glassivation that extends over the gate channel of the FET.

(l) For GaAs devices, voids in the glassivation which expose adjacent non-connected metal patterns of the FET.

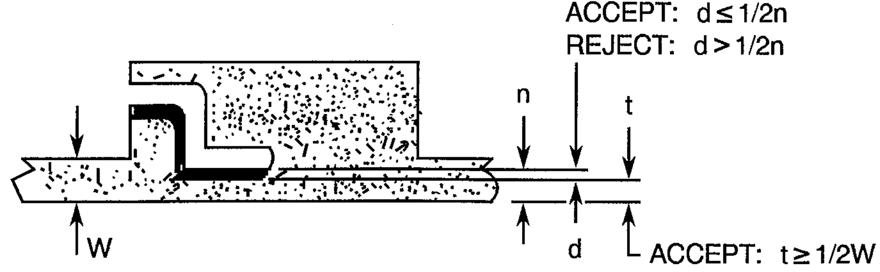
(m) For GaAs devices, scratches in the glassivation over the gate channel of the FET.

(n) For GaAs devices, scratches in the glassivation over the gate insertion of the FET.

(o) For GaAs devices, cracks in the glassivation which are more than 25μm inside the scribe line, or are more than 50% of the distance between the scribe line and any functional or active element (e.g. capacitor, resistor, FET) and which point toward any functional or active element unless the crack terminates at a device feature (e.g. transmission line or d.c. line).

FIGURE VIII - LASER TRIMMED GLASSIVATION DEFECTS

TOP HAT, SERPENTINE OR RECTANGULAR L TRIM



4.5 DIELECTRIC ISOLATION, "HIGH MAGNIFICATION"

No device shall be acceptable that exhibits:

(a) A discontinuous isolation line (typically a black line) around each diffusion well containing functional circuit elements (See Figure IX).

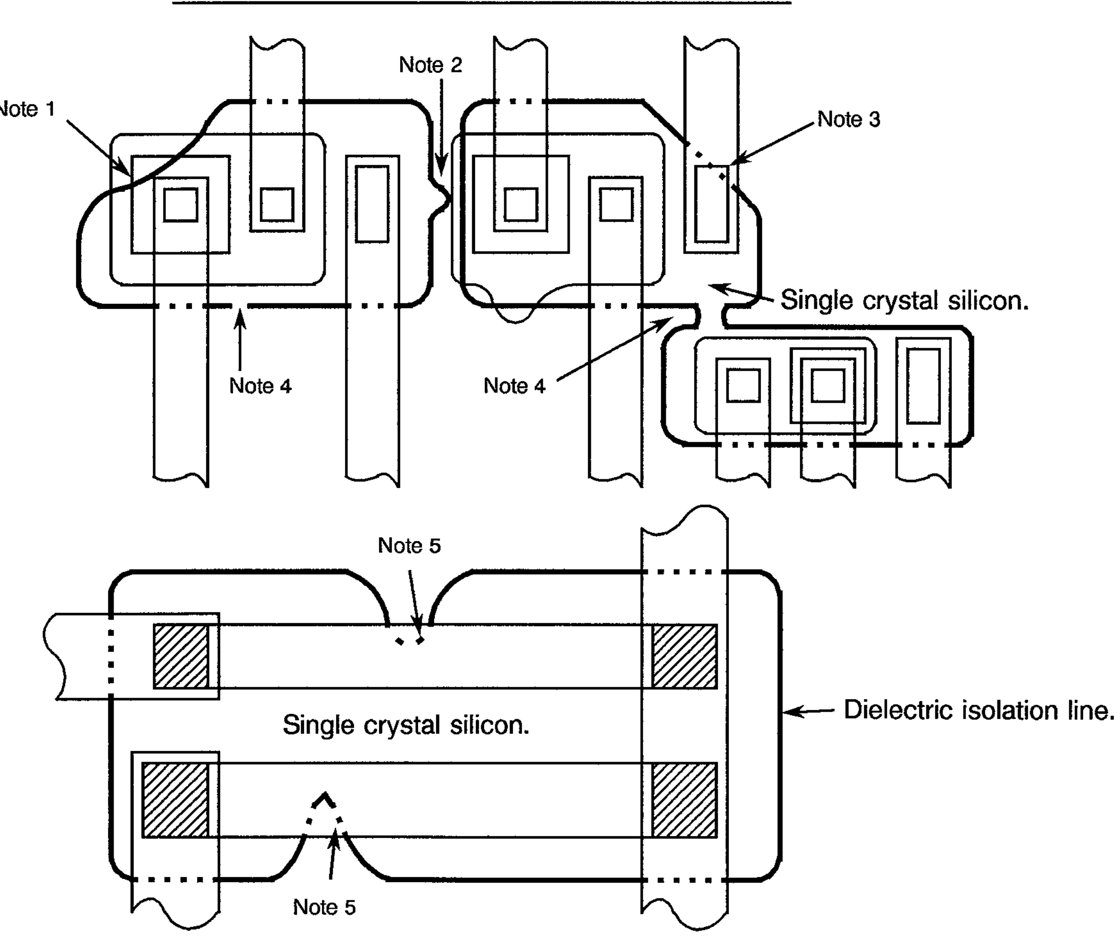
(b) Absence of a continuous isolation line between any adjacent wells, containing functional circuit elements (See Figure IX).

(c) A diffused area which overlaps dielectric isolation material and does not exhibit a line of separation to an adjacent diffusion well; or an overlap of more than one diffusion area into the dielectric isolation material (See Figure IX).

(d) A contact window that touches or overlaps dielectric material, unless in accordance with the design specification.

(e) Metallisation scratch and void defects over a dielectric isolation step shall be in accordance with the requirements of alinea (b) of Para. 4.1.1 and alinea (a) of Para. 4.1.2.

FIGURE IX - DIELECTRIC ISOLATION DEFECTS



NOTES

1. REJECT: Overlap of more than one diffusion.
2. REJECT: Dielectric isolation line without a line of separation to the adjacent tub.
3. REJECT: Contact window overlap.
4. REJECT: Discontinuous isolation line.
5. REJECT: Dielectric material extending under thin film resistor.

4.6 FILM RESISTOR, "HIGH MAGNIFICATION"

Rejection shall be based on defects found within the actively used portions of the film resistor. Metallisation defect criteria of 4.1 shall apply. No device shall be acceptable that exhibits:

(a) Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50% of the original resistor width (See Figure XI).

(b) No visible line of contact overlap between the metallisation and film resistor (See Figure XI).

(c) Increase in resistor width greater than 25% of the original line width.

(d) Void or necking down that leaves less than 75% of the film resistor width undisturbed at a terminal.

(e) Any sharp change in colour of resistor material within 25µm from the resistor/connector termination.

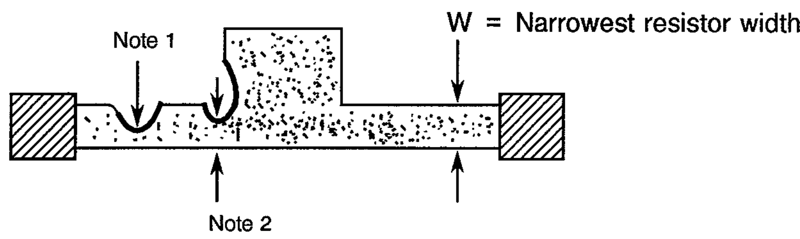
(f) Inactive resistor inadvertently connected to two separate points on an active circuit.

(g) Separation between any two resistors, or a resistor and a metallisation path, that is less than 6.3µm, or 50% of the design specification, whichever is less.

(h) Any thin film resistor that crosses a substrate irregularity (i.e. dielectric isolation line, oxide/diffusion step). This criterion does not apply to square isolated islands of single crystal silicon in the polysilicon area.

(i) Any resistor width reduced to less than half the narrowest resistor width, resulting from voids and/or scratches (see Figure X). The maximum allowable current density requirements shall not be exceeded.

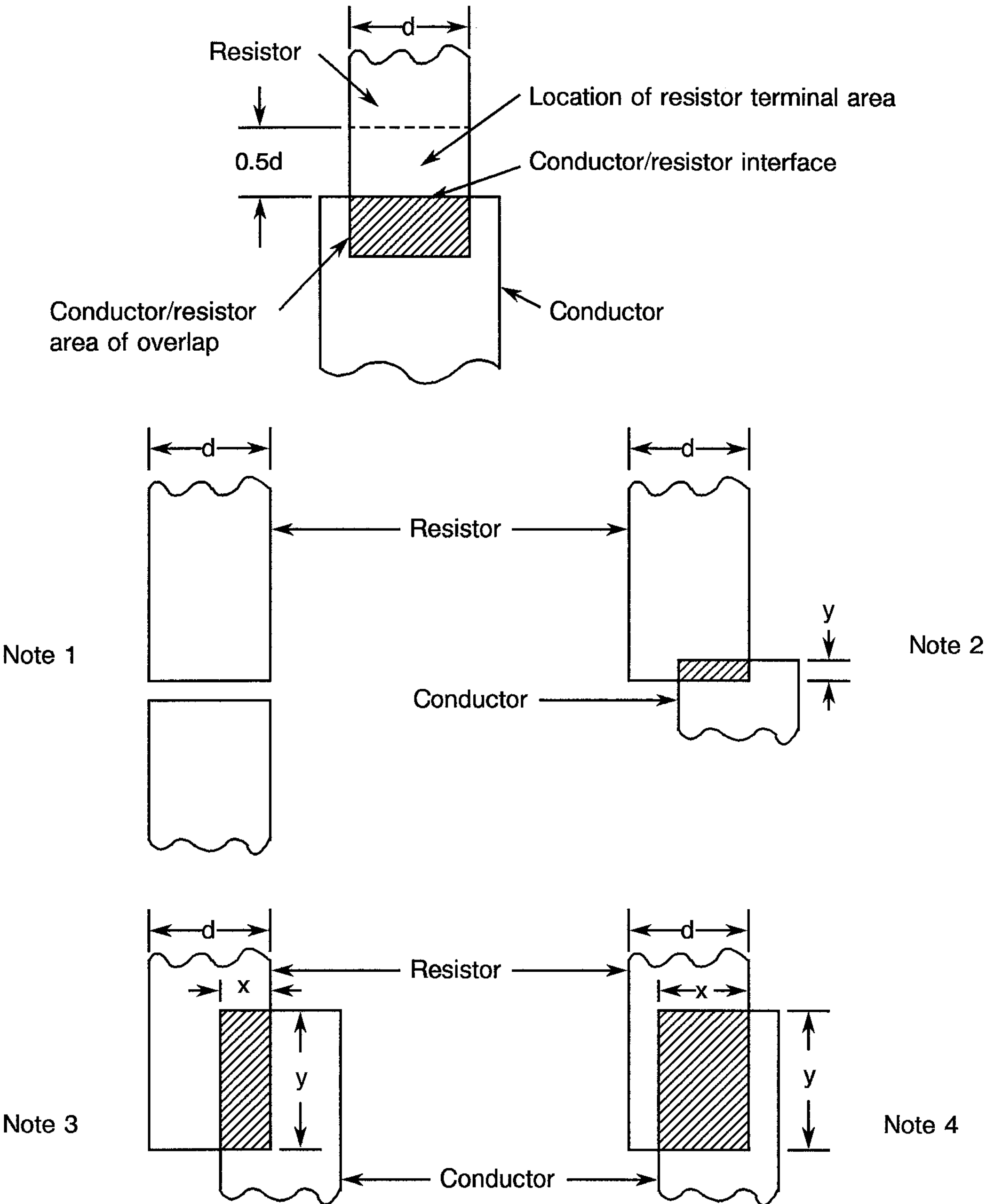
FIGURE X - SCRATCH AND VOID CRITERIA FOR UNTRIMMED RESISTORS



NOTES

1. REJECT: < 1/2W.
2. ACCEPT: ≥ 1/2W.

FIGURE X I - THIN FILM RESISTOR CONTACT AREA



NOTES

1. REJECT: No visible line of contact overlap.
2. ACCEPT: Y equal to or greater than 6.3µm.
3. REJECT: X less than 0.5d.
4. ACCEPT: X equal to or greater than 0.5d.

4.7 LASER TRIMMED THIN FILM RESISTORS, "HIGH MAGNIFICATION"

(a) A kerf less than 2.5μm in width, unless in accordance with the design specification.

(b) A kerf containing particles of detritus.

(c) A kerf containing untrimmed resistor material, unless that material is continuous across the kerf, and is undisturbed for a width greater than 0.5X the narrowest resistor width, unless by design (See Figure XII).

NOTES
1. Maximum allowable current density requirements shall not be exceeded.

(d) Resistor width that has been reduced by trimming to less than 0.5X the narrowest resistor width, including voids, scratches, or a combination thereof, in the trim area (See Figure XIII).

NOTES
1. Trimming of more than 50% of a given resistor shunt link is acceptable by design providing that the last shunt link of the resistor adder network is not trimmed greater than 50%. All trimmable resistor shunt links shall be defined on the design layout drawing.

(e) Trim path into the metallisation except block resistors.

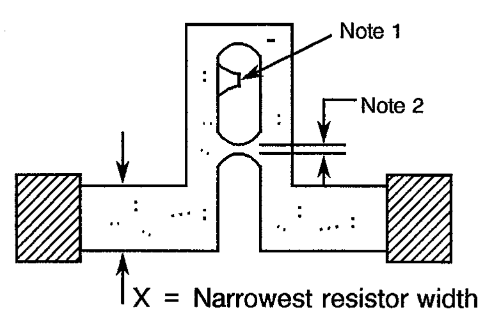
NOTES
1. This criteria can be excluded for trim paths into terminator ends of metallisation runs. Conductors or resistors may be trimmed open for link trims of by design.

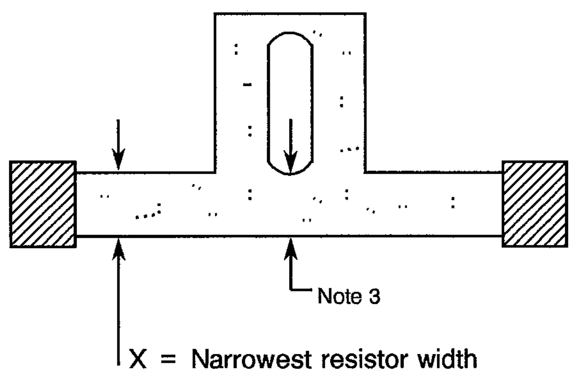
(f) Trim for block resistors which extends into the metallisation (excluding bonding pads) more than 25% of the original metal width (See Figure XIV).

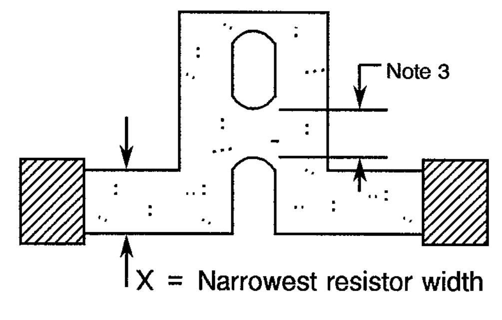
(g) Pits into the silicon dioxide in the kerf which do not exhibit a line of separation between the pit and the resistor material.

FIGURE X II - LASER TRIMMED THIN FILM RESISTORS

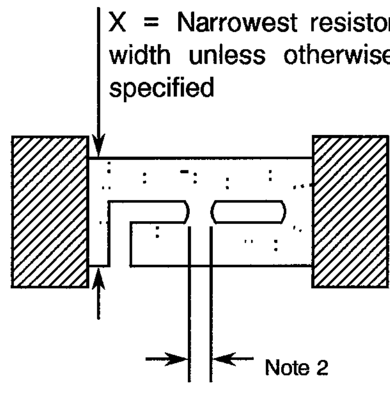
TOP HAT TRIM

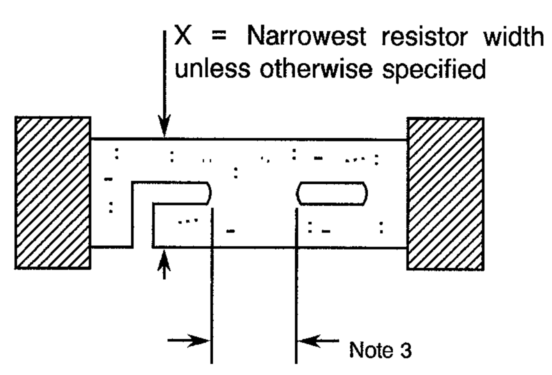






RECTANGULAR L TRIM



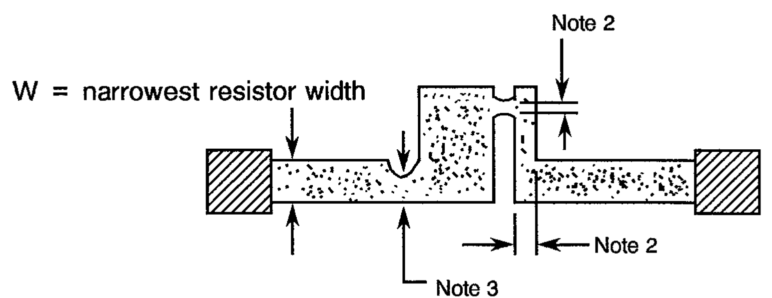


NOTES

1. REJECT: Untrimmed resistor material.
2. REJECT: <1/2X.
3. ACCEPT: >1/2X.

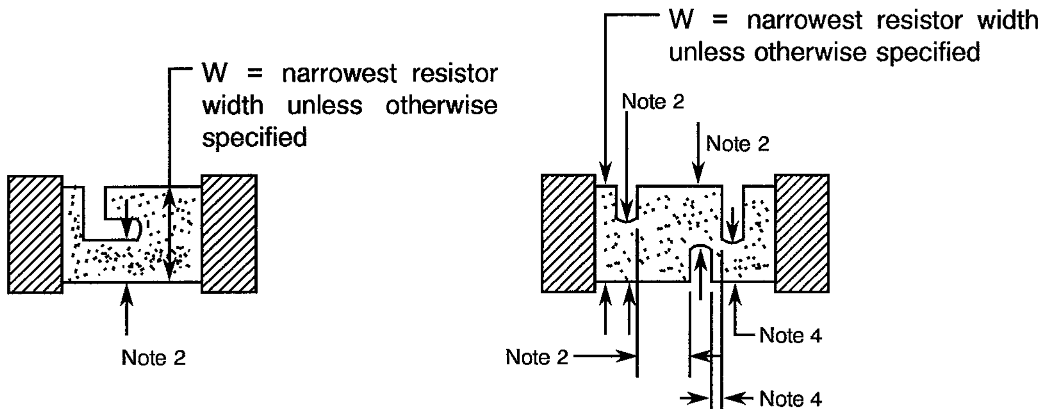
FIGURE XIII - SCRATCH AND VOID CRITERIA FOR TRIMMED RESISTORS

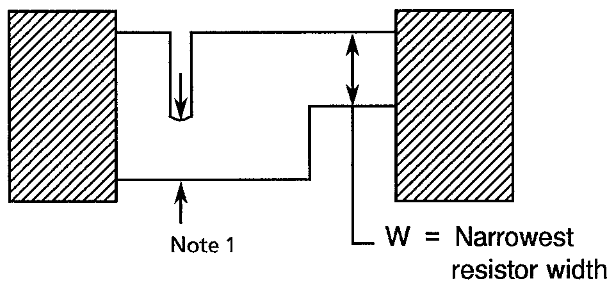
TOP HAT TRIM

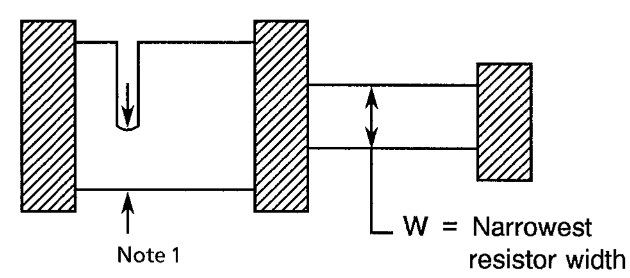


RECTANGULAR L TRIM

SERPENTINE TRIM





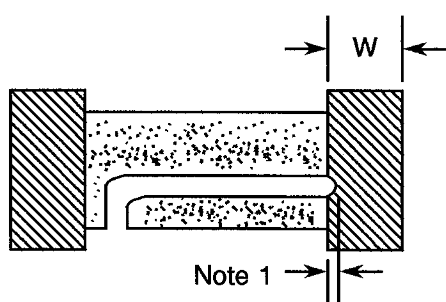


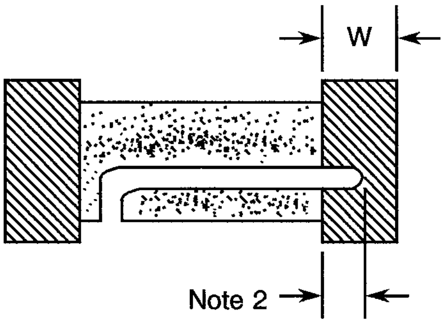
NOTES:

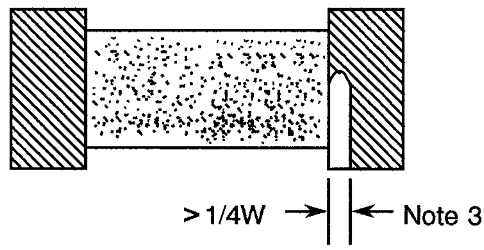
1. ACCEPT: $\geq 1/2W$.
2. ACCEPT: $\geq 1/2W$.
3. ACCEPT: Void or scratch $\geq 1/2W$.
4. REJECT: $< 1/2W$.

FIGURE XIV - BLOCK RESISTOR CRITERIA

TRIM INTO METAL







NOTES

1. ACCEPT: < 1/4W.
2. REJECT: > 1/4W.
3. REJECT: No laser trim into resistor film.

4.8 SCRIBING AND DIE DEFECTS "HIGH MAGNIFICATION"

No device shall be acceptable that exhibits:

(a) Less than 6.3µm of passivation visible between operating metallisation or bond periphery and bare semiconductor material.

NOTES
1. These criteria can be excluded for beam leads and peripheral metallisation including bonding pads where the metallisation is at the same potential as the die.
2. For GaAs devices, less than 2.5µm of substrate visible between operating metallisation or bond periphery and edge of the die.

(b) A chipout or crack in the active circuit area (See Figures XV and XVI). For GaAs devices, a chipout into, or underneath, the functional metallisation, i.e. bond pads, capacitors, peripheral metallisation, but excluding test structures of the device.

NOTES
1. This criterion can be excluded for peripheral metallisation that is at the same potential as the substrate. At least 50% of the metallisation width at the chipout shall remain undisturbed.

(c) Chipout or offset scribe lines/breaks into the non-active circuit area where the distance remaining between the active area and the edge of the fault is greater than 5µm.

(d) A crack whose length exceeds 75µm or comes closer than 6.25µm to any operating metallisation (except for substrate potential peripheral metal), or functional circuit element (See Figure XV).

(e) Semicircular crack(s) terminating at the die edge, long enough to bridge the narrowest spacing between unglassivated operating material (i.e. metallisation, bare semiconductor material, mounting material, bonding wire).

(f) Exposed semiconductor material extending over the passivation edge at the point of the beam lead exit from the die (See Figure XVI), applicable to beam lead structures.

(g) Die having attached portions of the active circuit area of another die.

(h) A crack whose length exceeds 6.25µm inside the scribe line or semiconductor material edge for beam lead devices that points toward operating metallisation or functional circuit elements (See Figure XVI).

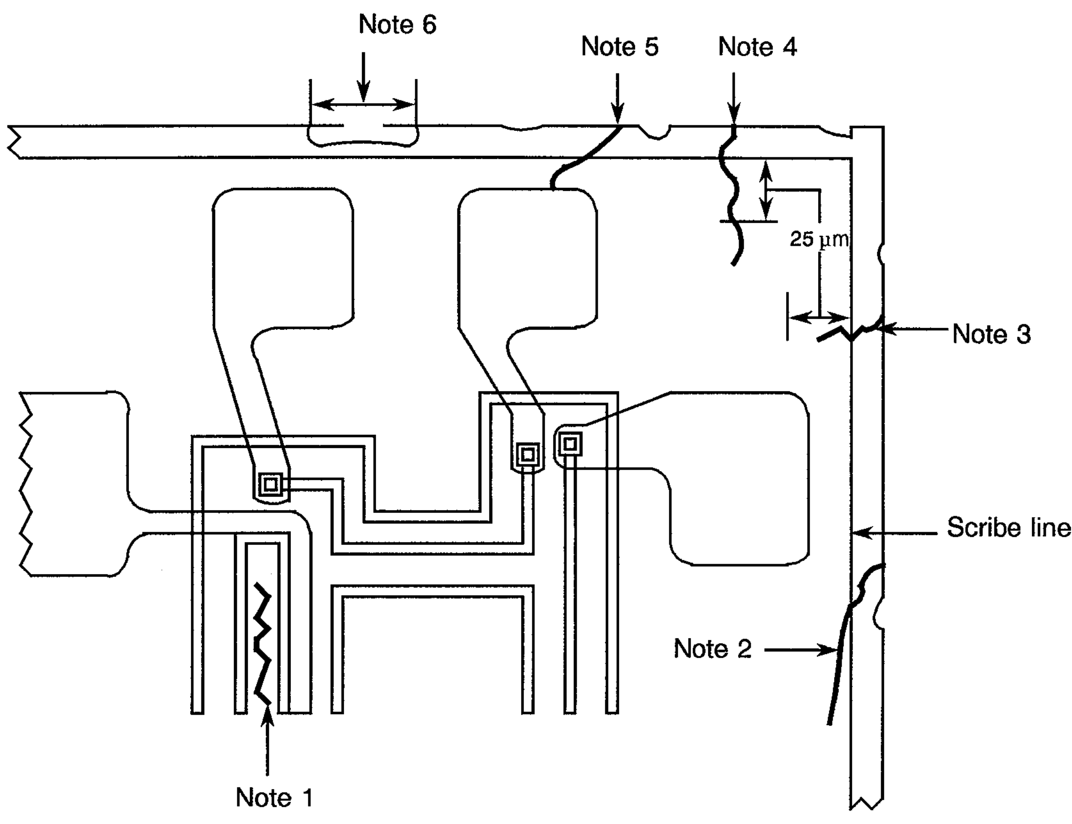
(i) A crack that comes closer than 12.5µm to operating beam lead metallisation (See Figure XVI).

NOTES
1. The criteria of alinea (d) and (i) can be excluded for beam lead devices where the chipout or crack does not extend into the semiconductor material.
2. The criteria of alinea (f), (h) and (i) do not apply to GaAs devices.

(j) Slivers of metallisation on the die after die scribe, due to the practice of printing test patterns onto the scribing line, that are large enough to bridge the spacing between unglassivated operating material.

(h) For GaAs devices, any cracks in the GaAs material which propagate through, or underneath, metallisation patterns of the device.

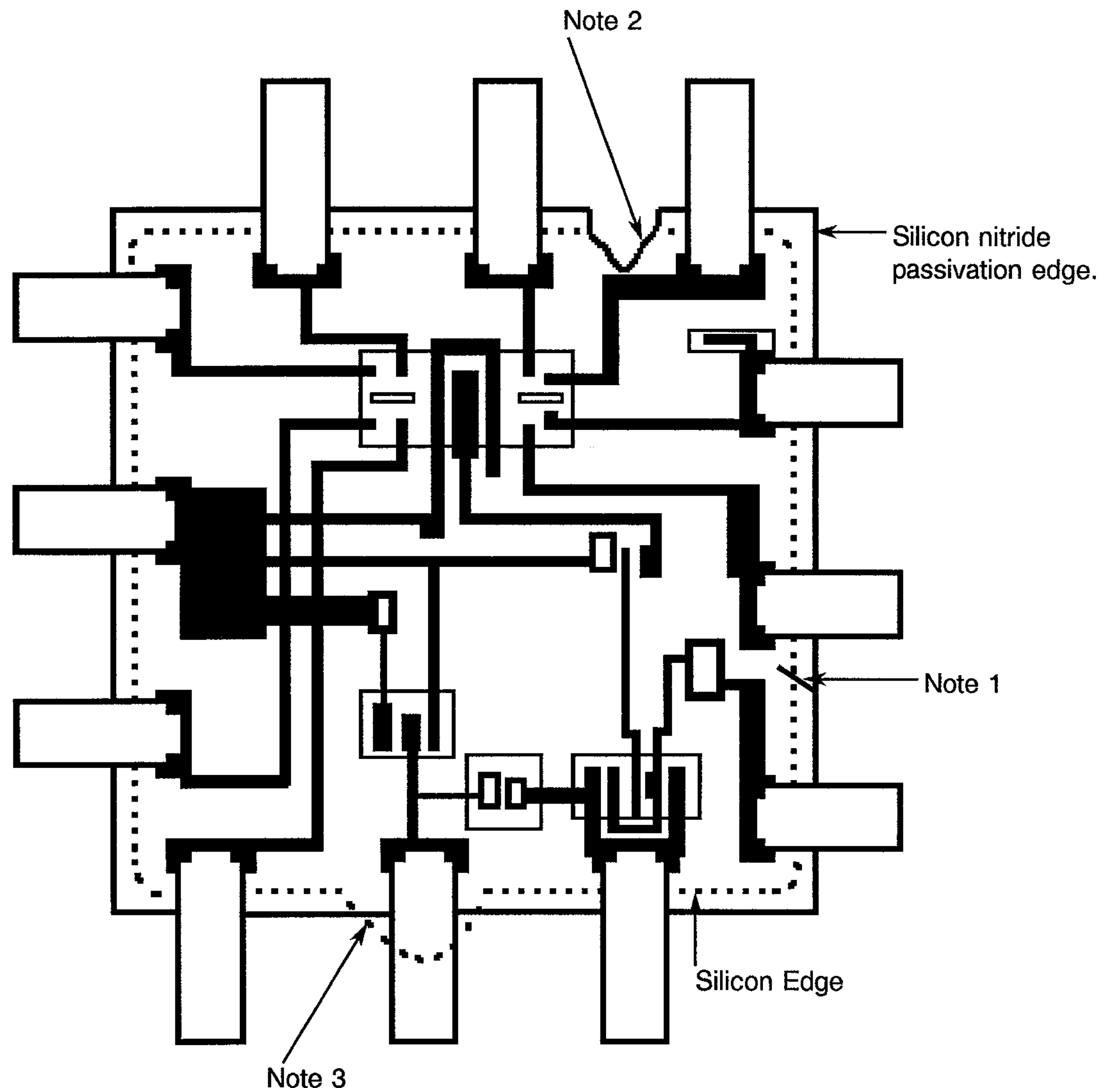
FIGURE X V - SCRIBING AND DIE DEFECTS



NOTES

1. REJECT: Substrate crack in active circuit area.
2. REJECT: Crack >75µm in length.
3. ACCEPT: Crack <25µm inside scribe line.
4. REJECT: Crack >25µm inside scribe line.
5. REJECT: Crack <25µm separation from operating metallisation.
6. REJECT: Semicircular crack having chord long enough to bridge the narrowest separation between unglassivated operating material.

FIGURE X VI - BEAM LEAD DIE FAULTS



NOTES

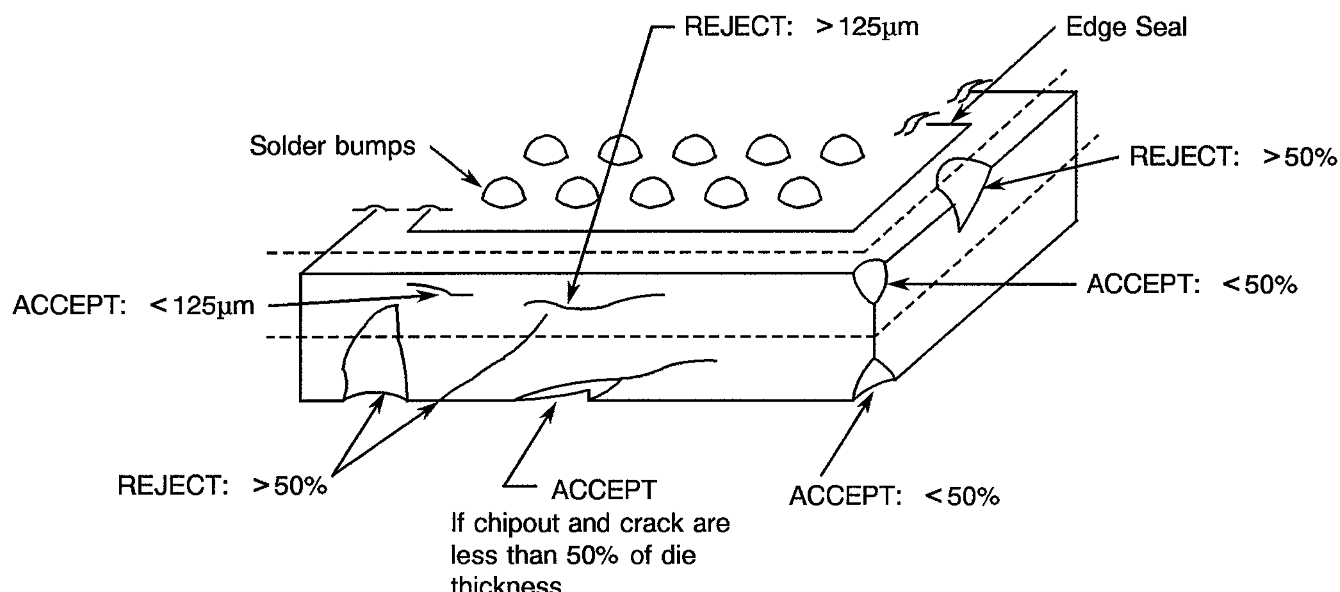
1. REJECT: Crack less than 12.5µm from operating beam lead metallisation.
2. REJECT: Chipout in active circuit area.
3. REJECT: Silicon extending beyond passivation edge at beam exit point.

(l) For GaAs devices, any cracks in the GaAs material outside of, but pointing toward, the metallisation patterns of the device.

(m) For flip chip, cracks or chipouts in the substrate material that extends beyond 50% of the substrate thickness, or a crack greater than 125µm in length in the substrate material (See Figure XVII).

(n) Any blistering, peeling, delamination, corrosion or other gross defects in the glassivation, metal, interlevel dielectrics or other layers.

FIGURE XVII - SCRIBING AND DIE DEFECTS (FLIP CHIPS)



4.9 BOND INSPECTION "LOW MAGNIFICATION"

This inspection and criteria shall be mandatory for the bond type(s) and location(s) to which they are applicable when viewed from above.

NOTES

1. The criteria applicable for bonds (called "wedge bonds" or "bonds") in Paras. 4.9.1 and 4.9.2 refers to the fully or partially deformed area including the tool impression shown as "L" in Figure XVIII. The criteria applicable for "bond tails" or "tails" refers to the resulting length of bonding wire extending beyond the bond shown as "T" in Figure XVIII. The tail is not part of the bond.

4.9.1 General (Gold Ball, Aluminium, Wedge, and Tailless)

As viewed from above, no device shall be acceptable that exhibits:-

(a) Bonds on the die where less than 75% of the bond is within the unglassivated bonding pad area.

(b) Bond tails where no visible line of separation is evident between the tail and the unglassivated metallisation, another bonding wire, wire bond, or wire bond tail; excluding common conductors and pads.

(c) Bond tails, at the die or package post/lead, that exceed two wire diameters in length.

(d) Bond tails extending over glassivated metallisation where the glass exhibits evidence of crazing or cracking that extends under the tail, excluding common conductors.

(e) Bonds that are not completely within the boundaries of the package post. For glass sealed packages, bonds not within 0.5mm of the end of the post.

(f) Rebonding (See Para. 4.9.5 applicable to microwave devices).

(g) Bonds, excluding tails, placed so that the horizontal separation between bond and glassivated or unglassivated, non-common metallisation, scribe lines, another bonding wire or bond is less than 6μm.

NOTES

1. When, by design, there are multiple bonds on a common bonding pad or post, they may not reduce the width of an adjacent bond by more than 25%.

(h) Bonds, excluding tails, placed such that less than 50μm of the bond periphery (on glassivated or unglassivated areas) is exposed to an undisturbed die metallisation connecting path to, or from, the entering or exiting metallisation stripe (See Figure XIX).

NOTES:

1. When bond tails prevent visibility of the connecting path, and the metallisation immediately adjacent to the bond tail is disturbed, the device shall be unacceptable.
2. When a fillet area exists, it is considered as part of the entering/exiting metallisation stripe.

(i) Bonds where more than 25% of the bond is located on die mounting material.

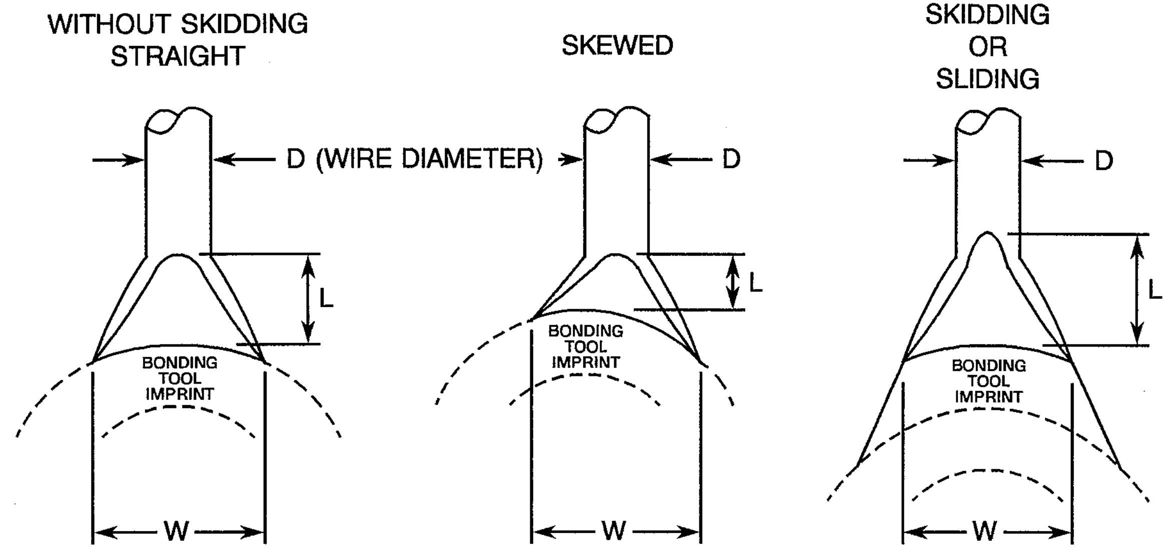
(j) Bonds placed so that the wire exiting from the bond crosses over another bond.

(k) Any evidence of repair of conductors by bridging with additional material.

(l) A bond overlapping another bond, bond wire or residual segment of lead wire, except for compound bonding of microwave devices.

FIGURE XVIII - BOND DIMENSIONS

CRESCENT BOND



WEDGE BOND

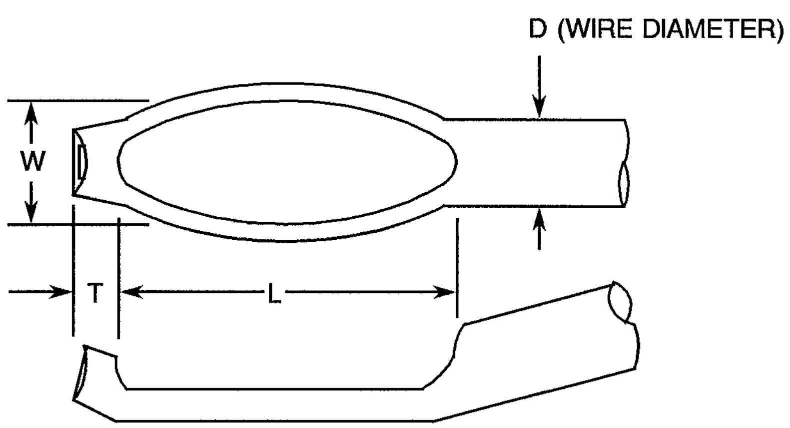
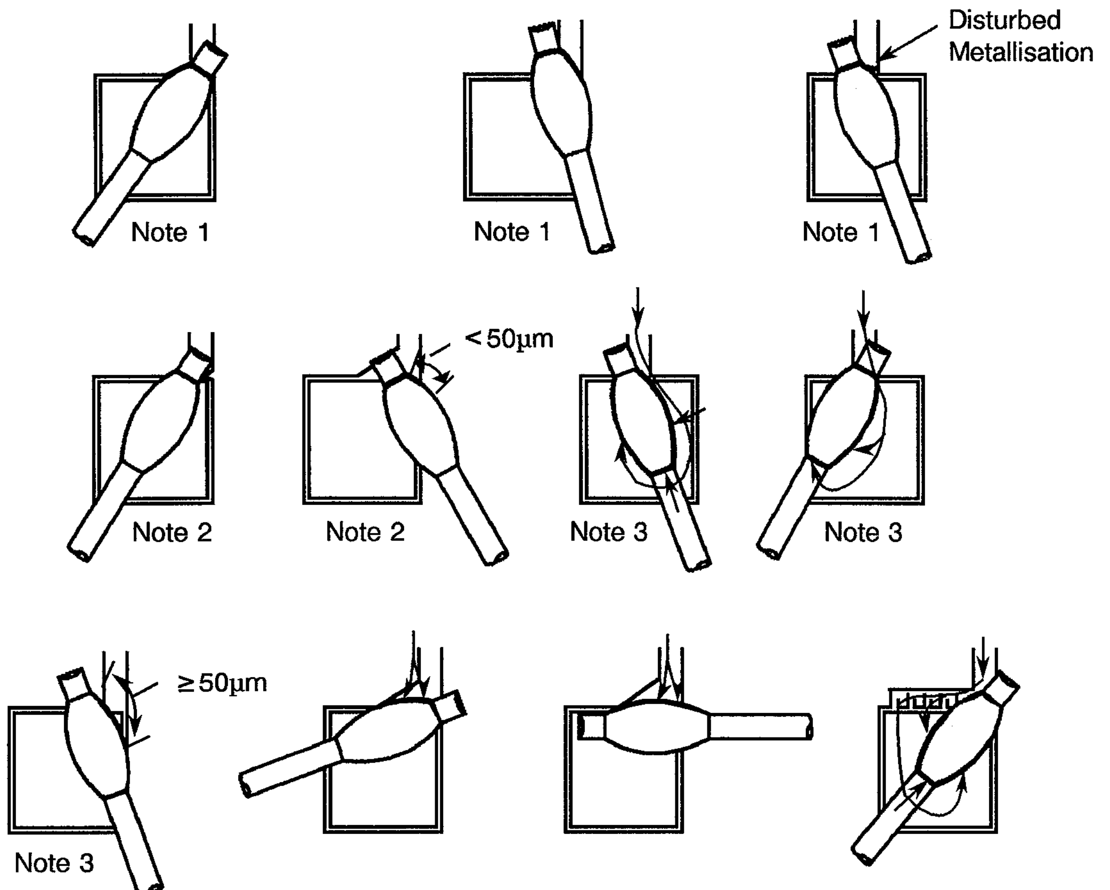


FIGURE XIX - BONDS AT METALLISATION EXIT



Arrows indicate the connecting path to the bond periphery

NOTES

1. REJECT: Bond (excluding tails) placed such that less than 50μm of bond periphery (on glassivated or unglassivated areas) is exposed by an undisturbed die metallisation connecting path to/from the entering/exiting metallisation stripe.
2. REJECT: When bond tails prevent visibility of the connecting path to 50μm of the bond periphery and the metallisation immediately adjacent to the bond tail is disturbed.
3. ACCEPT: Bonds (excluding tails) placed such that there is 50μm or greater of bond periphery (on glassivated or unglassivated areas) exposed by an undisturbed die metallisation connecting path to/from the entering/exiting metallisation stripe.

(m) Intermetallic formation extending radially in excess of 2.5μm completely around the periphery of that portion of the gold bond located on metal.

(n) Bonds on foreign material.

(o) Bond touching metallisation other than bond pad metallisation.

(p) Metallic protrusions around wire bonds in the form of scuffed bonding pad material for wire bond whiskers. This does not include lateral metal disturbances up to 5μm around the side of the wire bond or 1 wire diameter in front of the wire bond.

(q) Side welds having less than an estimated 50% of the package-post weld situated on the specified bonding area.

(r) Where multiple bonding is employed, there is no visible gap between the bonds.

(s) Bond lifting or tearing at the interface of the pad and wire. This criteria is applicable to single bonds and any part of a double bond.

(t) Bond wire fragments or bond pad metal detached from the bond or pad.

(u) One aluminium whisker greater than half a wire diameter.

(v) More than 50% of the pads show aluminium whiskers greater than half the smallest width of the metallised strip.

(w) Multicoloured stains in the bonding pad area. Multicoloured stains appearing along the periphery of the etch line are acceptable, provided that the unstained metallisation is not reduced to less than 75% of the bonding pad area.

4.9.2 Wedge Bonds

No device shall be acceptable that exhibits:-

(a) Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or more than 3.0 times the wire diameter in width, or are less than 1.5 times or more than 6.0 times the wire diameter in length.

(b) Thermocompression wedge bonds on the die or package post that are less than 1.5 times or more than 3.0 times the wire diameter in width, or are less than 1.5 times or more than 6.0 times the wire diameter in length.

(c) Wedge bonds where the tool impression does not cover the entire width of the wire.

(d) Bond width less than 1.0 times the wire diameter. For aluminium wires, 50μm or greater in diameter.

(e) Pad bond torn in the bond area or behind the bond. (See Figure XX).

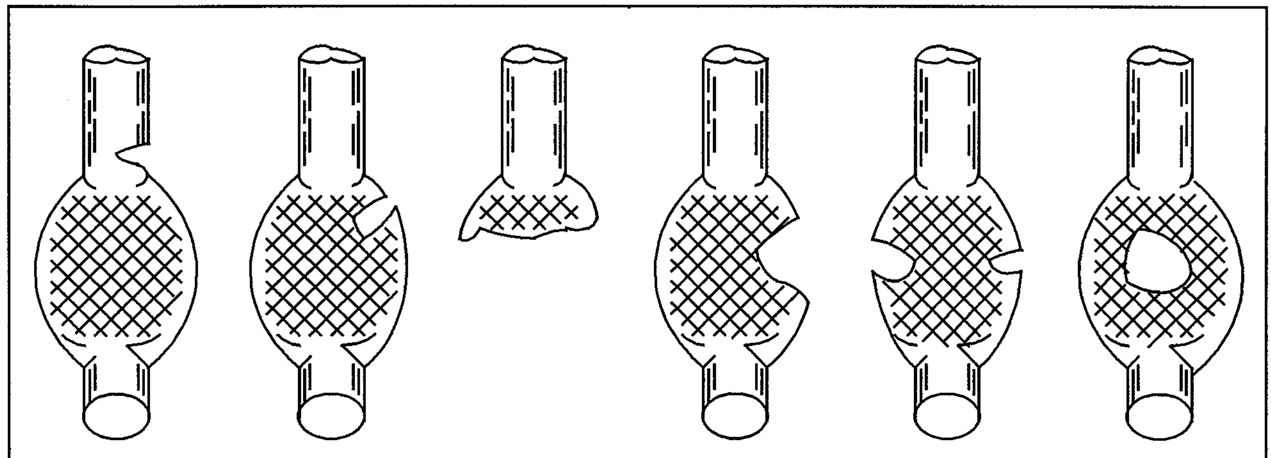
(f) Nicks in the side of the bond or holes in the centre of the bond. (See Figure XX).

(g) If the bond is smaller than the pad area, at least 75% of the tool impression of the pad bond must be bonded to the metallisation.

(h) If the bond is larger than the pad area, less than 50% of the tool impression of the pad bond appearing on the area of the pad.

FIGURE XX - TORN AND INCOMPLETE BONDS

REJECT



4.9.3 Tailless Bonds (Crescent, Terminating Capillary Bond)

No device shall be acceptable that exhibits:-

(a) Tailless bonds on the die or package post that are less than 1.2 times or more than 5.0 times the wire diameter in width, or are less than 0.5 times or more than 3.0 times the wire diameter in length.

(b) Tailless bonds where bond impression does not cover the entire width of the wire.

4.9.4 Gold Ball Bonds

No device shall be acceptable that exhibits:-

(a) Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter. (See Figure XXI).

(b) Gold ball bonds where the wire exit is not completely within the periphery of the ball. (See Figure XXI).

(c) Gold ball bonds where the wire centre exit is not within the boundaries of the unglassivated bonding pad area.

(d) Intermetallic formation extending radially more than 2.5µm completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.

(e) A wire from the ball bond which does not leave the die vertically without kinking or otherwise departing from a smooth line and does not begin to curve towards the post before reaching two thirds of the post height.

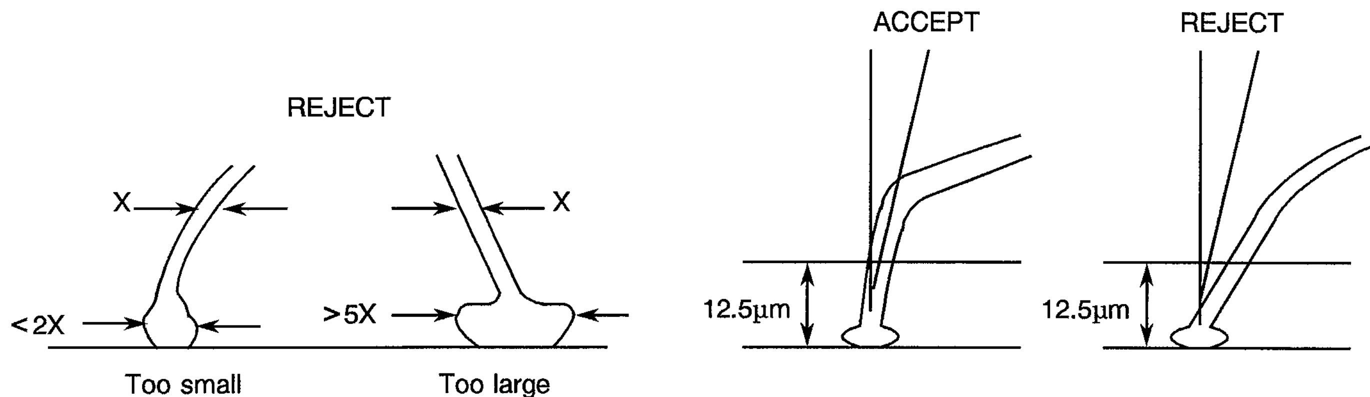
(f) The wire from the ball bond on the die rising to more than 4/3 of the post height. The requirement of the excessive loop sag must still be met.

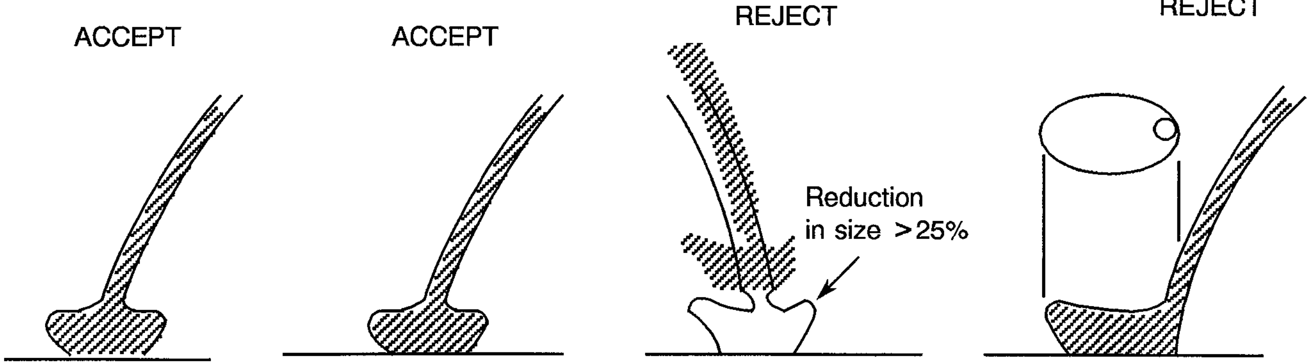
(g) A reduction in the diameter of the wire of >25% where the wire contacts the ball. (See Figure X X I).

(h) Less than 2/3 of the ball in contact with the pad.

(i) Wire not within 10° of the perpendicular to the surface of the chip for a distance of greater than 12.5µm before bending towards the package post or other terminating point. (See Figure X X I).

FIGURE X X I - BALL BONDS





Wire exits from edge of ball

4.9.5 Rebonds (applicable to microwave devices)

A rebond may be a requirement for microwave devices where tuning, via the bond, is necessary. A rebond is permitted only if the original bond has not removed bond pad material. The following criteria apply to rebonds:-

(a) Rebonding on the die shall only be permitted where the bond pad area has been designed to accommodate a rebond. The second bond shall be at a point near to the metallisation exit. There shall be no residual bond material between the rebond and the existing material.

(b) At least 50% of the attachment area of the rebond shall be placed on undisturbed metal, excluding probe marks which do not expose underlying material.

(c) Only one rebond shall be permitted at any one bonding pad or bonding terminal location.

(d) The total number of rebonds, as defined above, shall be limited to a maximum of 10% to the nearest whole number of the total number of bonds on the device (1 rebond can always be allowed).

(e) A bond-off is defined as a bond made in the process of clearing the bonding tool following an unsuccessful bond attempt. Extra lead wires, other than bond-offs, anywhere on the package as a result of clearing the bonding tool are cause for rejection.

4.9.6 Beam Lead

This inspection and requirements shall apply to the completed bond area made using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:-

(a) Bonds where the tool impression does not completely cross the entire beam width.

(b) Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15% (10% for compliant bonds) or greater than 75% of the undeformed beam width.

(c) Bonds where the tool impression length is less than 25μm (See Figure XXII).

(d) Bonding tool impression less than 25μm from the die edge (See Figure XXII).

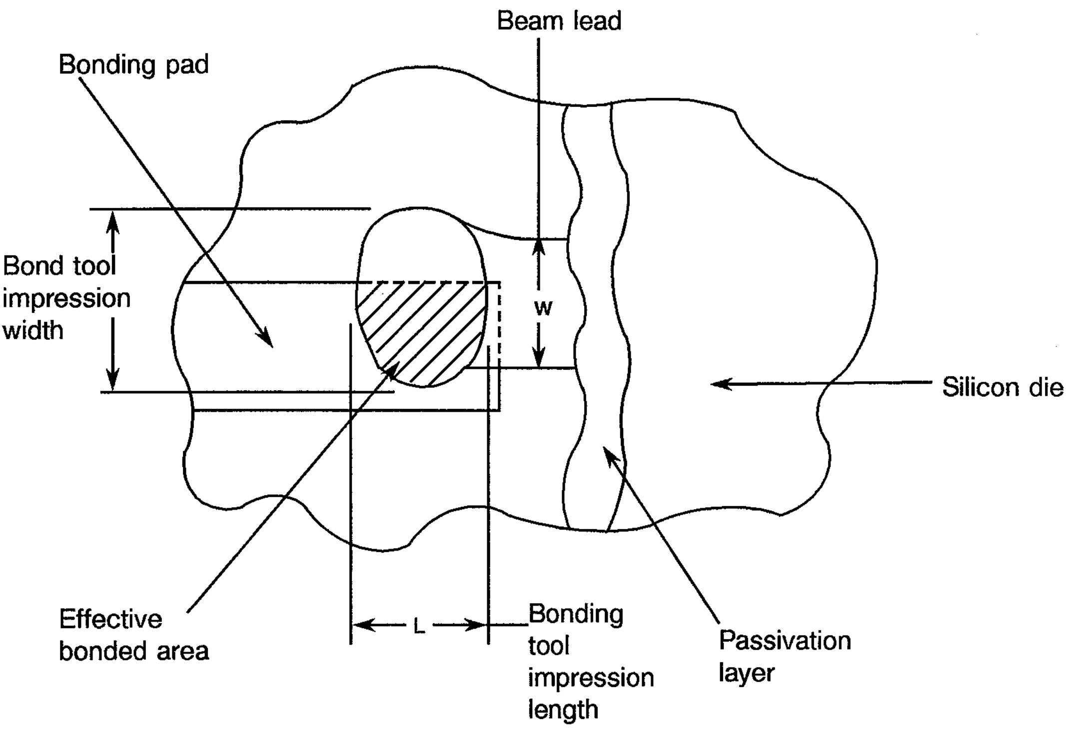
(e) Effective bonded area less than 50% of that which would be possible for an exactly aligned beam (See Figure XXII).

(f) Cracks or tears in the effective bonded area of the beam greater than 50% of the original beam width.

(g) Bonds placed so that the separation between bonds, and between bonds and operating metallisation not connected to them, is less than 2.5μm.

(h) Bonds lifting or peeling.

FIGURE X X II - BEAM LEAD BOND AREA AND LOCATION



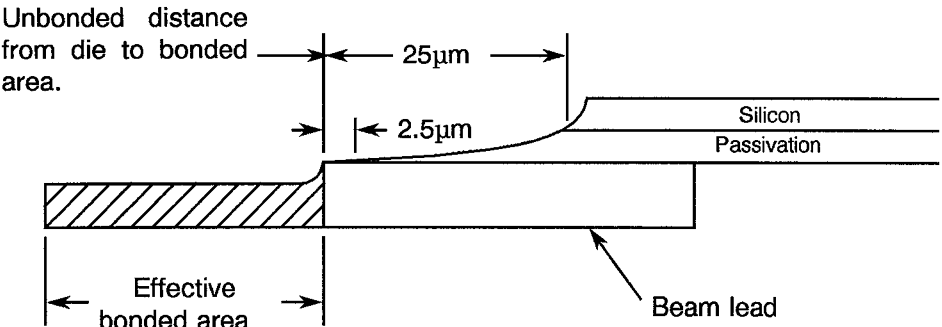
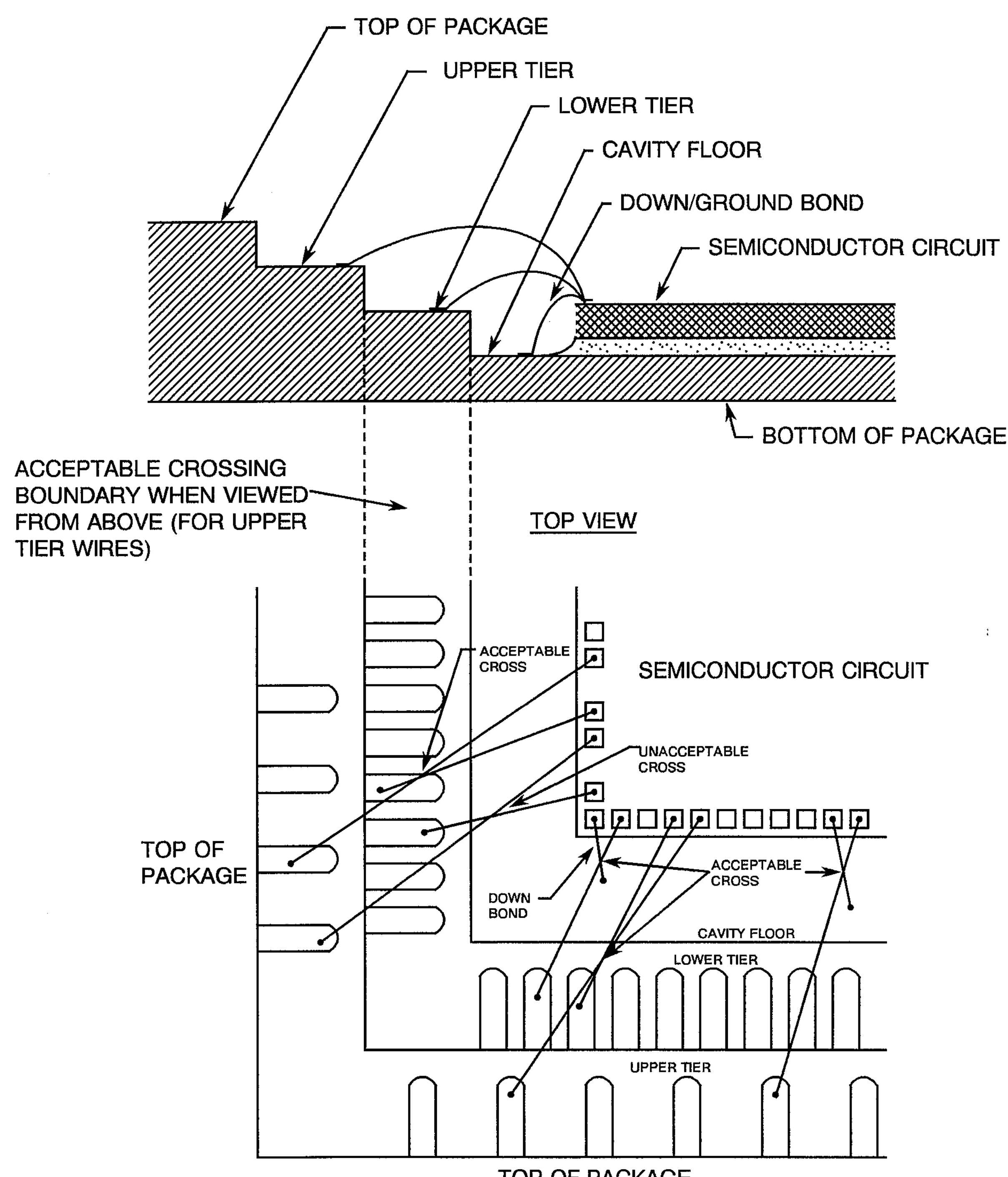


FIGURE XXIII - CRITERIA FOR WIRE(S) CROSSING WIRE(S)

SIDE CROSS-SECTION VIEW



4.10 INTERNAL LEADS, "LOW MAGNIFICATION"

The inspection and criteria shall be mandatory for the lead type(s) and location(s) to which they are applicable when viewed from above. When the requirement of Para. 4.10.1 is not easily determined vertically, the device may be rotated about the X and Y axis to allow an alternate view of the wires such that the vertical separation is verified.

4.10.1 Wires

No device shall be acceptable that exhibits:-

(a) Any wire with a separation of less than two wire diameters to unglassivated operating metallisation, other bonds, another wire (common wires excluded), package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any portion of the package, including the plane of the lid to be attached.

Within a 120µm radial distance from the perimeter of the bond on the die, the separation shall be 25µm minimum.

(b) Nicks, bends, cuts, crimps, scoring or neckdown in any wire that reduces the wire diameter by more than 25%.

(c) Missing or extra lead wires.

(d) Tearing at the junction of the wire and bond or lifted bonds.

(e) Any wire making a straight line run from die bonding pad to package post that has no arc.

(f) Wire less than 125µm diameter bowed more than 7 wire diameters or greater than 125µm diameter bowed more than 3 wire diameters.

(g) Excessive loops, bows or sags in any wires such that they could short to another wire, pad package post, die or touch any portion of the package.

(h) Wire(s) crossing wire(s), except common conductors, when viewed from above, except in multi-tiered packages, where the crossing occurs within the boundary of the lower wire bond tier(s) being crossed or packages with down bond(s). In these situations, the wires that cross are acceptable if they maintain a minimum clearance of 2 wire diameters (See Figure XXIII).

NOTES

1. No bond wire shall cross more than one other bond wire and there shall be no more than 4 crossovers, or crossovers involving more than 10% of the total number of wires, whichever is greater for any single package cavity.

(i) Wire(s) not in accordance with bonding diagram.

(j) Wire has an unintentioned sharp bend with an interior angle of less than 90°, or twisted to such an extent that stress marks appear.

(k) For ball bonded devices, wire not within 10° of the perpendicular to the surface of the chip for the distance of greater than 12.5µm.

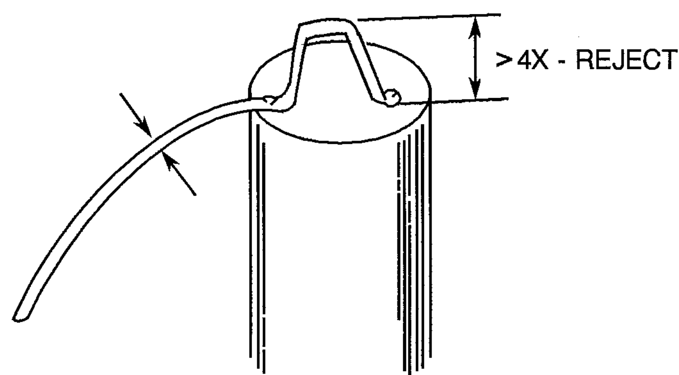
(l) Excessive lead burn at lead post weld.

(m) A bow or loop between double bonds at post greater than 4 x wire diameter. (See Figure XXIV).

(n) Wire twisted more than 360° from the pad post to the pillar bond.

(o) Bond wires which do not clear the die edge by at least 25µm.

FIGURE X X IV - LOOP BETWEEN DOUBLE BOND



4.10.2 Beam Lead Construction

4.10.2.1 Bonds

This inspection criteria shall apply to the completed bond area made, using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:-

(a) Bonds where the tool impression does not completely cross the entire beam width.

(b) Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15% (10% for compliant bonds) or greater than 75% of the undeformed beam width.

(c) Bonds where the tool impression length is less than 25µm (See Figure X X II).

(d) Bonding tool impression less than 25µm from the die edge (See Figure X X II).

(e) Effective bonded area less than 50% of that which would be possible for an exactly aligned beam (See Figure X X II).

(f) Cracks or tears in the effective bonded area of the beam greater than 50% of the original beam width.

(g) Bonds placed so that the separation between bonds and between bonds and operating metallisation not connected to them is less than 2.5µm.

(h) Bonds lifting or peeling.

4.10.2.2 Beam Leads

No device shall be acceptable that exhibits the following:-

(a) Voids, nicks, depressions, or scratches that leave less than 50% of the beam width undisturbed.

(b) Beam separation from the die.

(c) Missing or partially fabricated beam leads unless in accordance with the design specification.

(d) Beam leads that are not bonded.

(e) Bonded area closer than 2.5µm to the edge of the passivation layer.

(f) Passivation layer less than 2.5µm between the die and the beam visible at both edges of the beam (See Figure X X II).

4.10.3 Up-Bonding

(a) Wire not travelling in a smooth upward arc from the pad bond to the edge of the die and clearing the edge by 75µm (See Figure XXV).

(b) Wire rising more than 7 wire diameters above the top of the pillar (See Figure XXV).

(c) Wire sagging below a line parallel to the top of the header and 75µm above the top of the die (See Figure XXV).

4.10.4 Down-Bonding

(a) Wire not travelling in smooth arc from the bond to the edge of the die and clearing the edge by 25µm for an upward arc, 75µm for a downward arc.

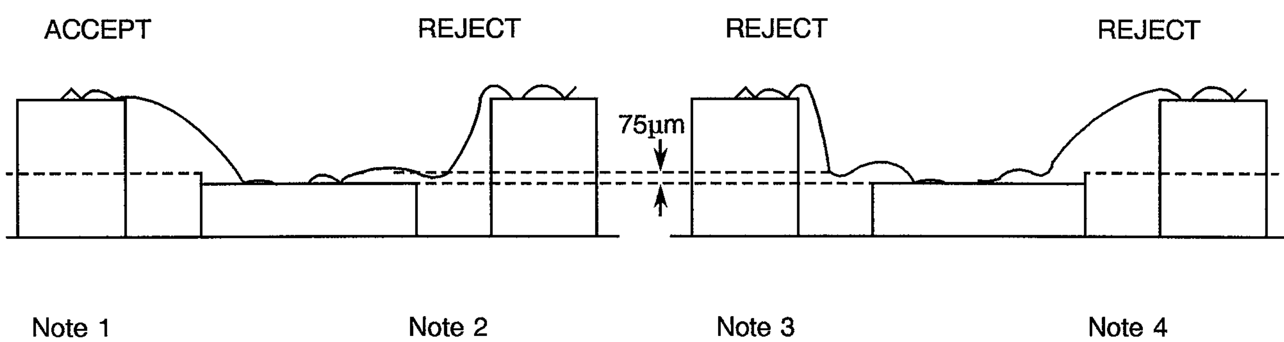
(b) Wire sagging below a line parallel to the top of the header and 75µm above the top of the header and 75µm above the top of the die (See Figure XXVI).

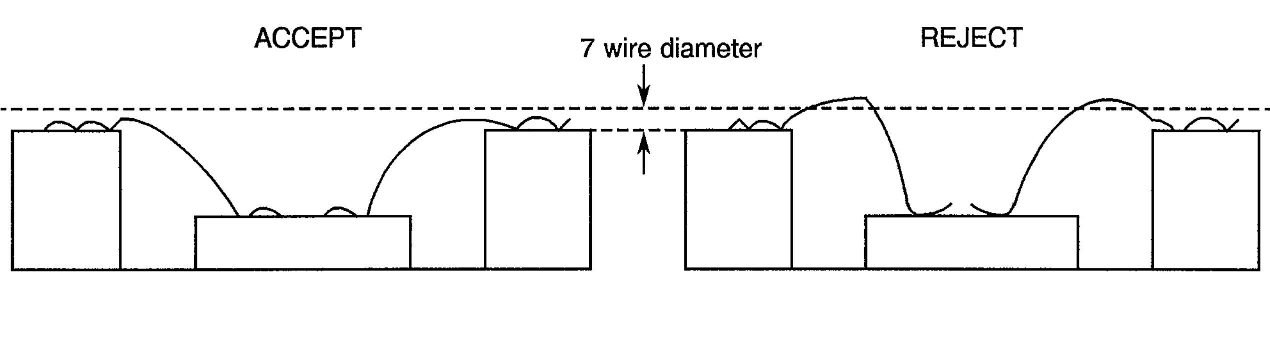
(c) For ultrasonic bonding: Wire equal to or less than 75µm in diameter, rising more than 250µm or 7 wire diameters, whichever is the less, above the top of the die: Wire greater than 75µm in diameter, rising more than 3 wire diameters above the top of the die (See Figure XXVI).

(d) For gold ball bonding: Gold wire rising more than 10 wire diameters above the top of the die (See Figure XXVI).

FIGURE X X V - UP-BONDING

UP BONDING

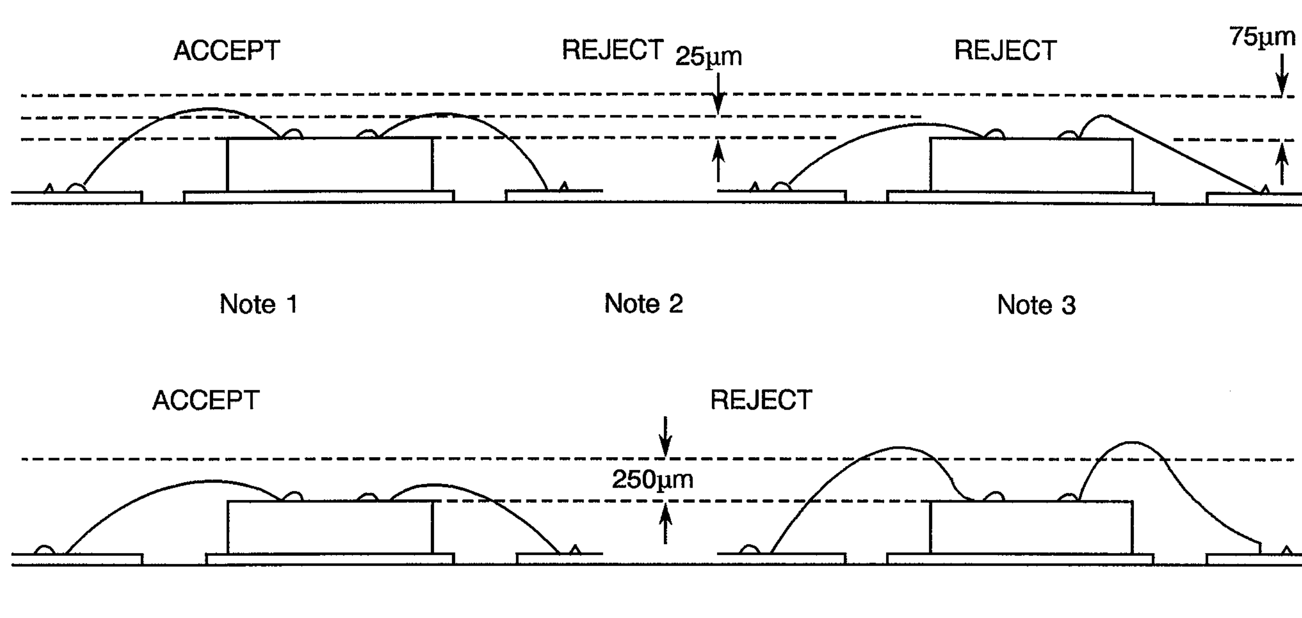


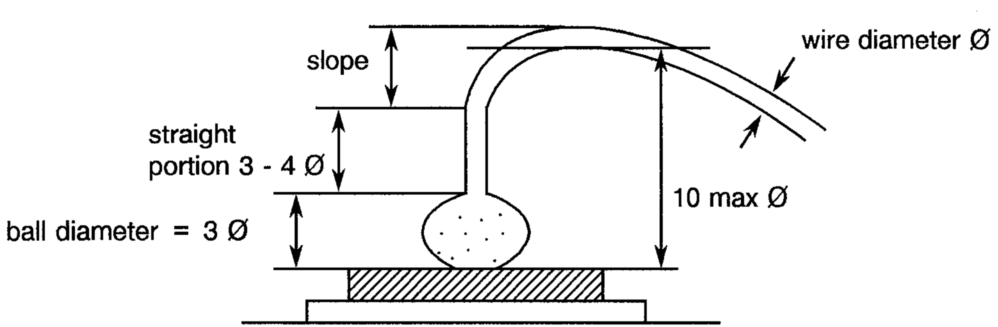


NOTES

1. ACCEPT: Proper arc and clearance.
2. REJECT: Clearance <75µm.
3. REJECT: Sags below 75µm line.
4. REJECT: Not rising in smooth upward arc.
5. ACCEPT: Rises <7 X wire diameter.
6. REJECT: Rises >7 X wire diameter.

FIGURE X X VI - DOWN-BONDING





NOTES

1. ACCEPT: Proper arc and clearance.
2. REJECT: Clearance <25µm in upward arc.
3. REJECT: Clearance <75µm in downward arc.
4. ACCEPT: Proper arc and clearance.
5. REJECT: >250µm above top of die.
6. ACCEPT: <10 wire diameters above top of die.

4.11 DIE MOUNTING

4.11.1 Die Mounting "Low Magnification", Eutectic

(a) Die mounting material build-up that extends on to, or vertically above, the top surface of the die.

(b) Die mounting material (eutectic wetting) not visible around at least two complete sides, or 75%, of the die perimeter, except for transparent die.

(c) Transparent die with less than 50% of the area bonded.

(d) Flaking of the die mounting material.

(e) Balling or build-up of the die mounting material that does not exhibit a minimum of a 50% peripheral fillet, when viewed from above, or the accumulation of bonding material is such that the height of the accumulation is greater than the longest base dimension or the accumulation necks down at any point. (See Figure XXVIII).

(f) Any eutectic material on the glass to metal seal which reduces the exposed glass surface distance from header to post by more than 25%.

(g) Where top metallisation of the die extends to the die edge the maximum height of conductive material allowable is 50% up the side of the die.

4.11.2 Die Mounting "Low Magnification", Non-eutectic, Inorganic

(a) Adhesive material immediately adjacent to the die that extends on to, or vertically above, the top surface of the die.

(b) Adhesive fillet not visible along 75% of each side of the die.

(c) Any flaking, peeling, or lifting of the adhesive material.

(d) Separation, cracks or fissures whose width is ≥50μm in the adhesive at the cavity wall or cavity floor.

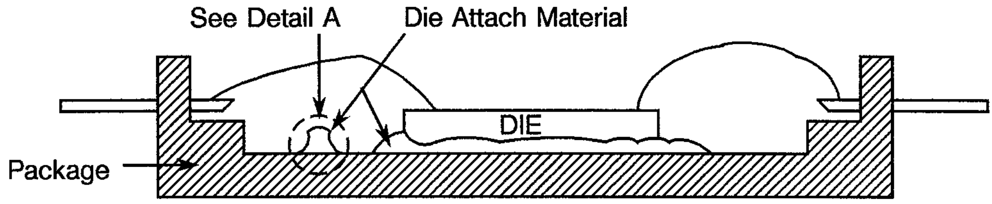
(e) Crazing in the adhesive. Cracks are fractures in the adhesive that have sharp broken edges. Crazing is the presence of numerous minute interconnected surface cracks.

(f) Adhesive material on the top surface of the die.

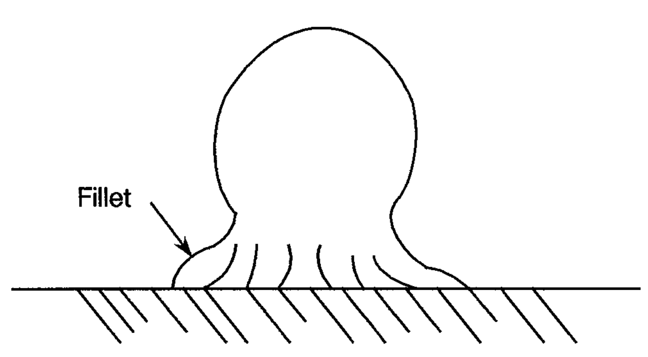
(g) Any adhesive material that is connected to the fillet or conductive cavity (e.g. metal package base or metallised floor of ceramic package) and extends up the cavity wall to within 25μm of the package post.

(h) Transparent die with less than 50% of the area bonded.

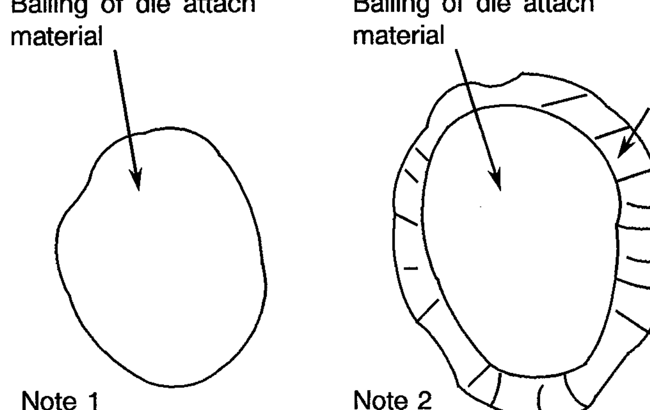
FIGURE XXVII - BALLING OF DIE ATTACH MATERIAL

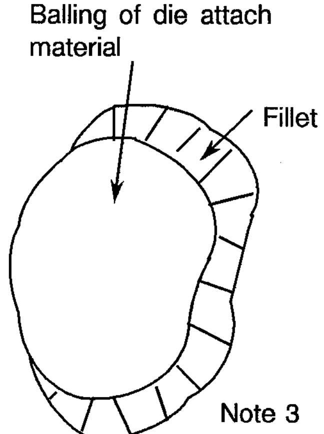


DETAIL A - FRONT VIEW



DETAIL A - TOP VIEW





NOTES

1. REJECT: No fillet visible.
2. ACCEPT: Fillet visible.
3. ACCEPT: Fillet 50% or greater.

4.11.3 Die Orientation

(a) Die not located or orientated in accordance with the applicable assembly drawing of the device.

(b) Die not level within 10° with respect to the die bonding area (package cavity).

(c) Die which overlaps on to any insulating materials, unless in accordance with the design specification.

(d) Die geometry or dimensions not in accordance with the device assembly drawings.

(e) Where mounted on top of a post, the die extends outside the area of the post, except for microwave devices.

(f) When die preform mounting material is used, die which overlaps preform.

(g) Preforms that are not firmly attached to the package.

(h) Preforms which overlap on to any insulating material.

(i) Preform not properly melted.

4.11.4 Insulating Island (Stand-off) Mounting Defects (Multi-chip Devices)

(a) Die mounting material (other than conductive glasses) build up that touches the conductive top surface of the insulating island.

(b) Die mounting material (other than non-conductive glasses) that extends vertically above the top surface of the insulating island.

(c) Die mounting material around the perimeter of the base of the insulating island where there is less than 75% of the perimeter with mounting material attachment visible.

(d) Insulating island which does not meet the applicable orientation criteria of Para. 4.11.3.

4.12 FOREIGN MATERIAL

Die inspection shall be at high magnifications while package and lid inspection may be at low magnifications.-

(a) Foreign particle(s) on the surface of the die or within the package or on the lid or cap that is/are large enough to bridge the narrowest spacing between unglassivated operating material (metallisation, bare semiconductor material, mounting material, bonding wire, etc.).

NOTES

1. Chips of semiconductor material shall be considered as foreign particles.

(b) Foreign particle(s) other than on the surface of the die within the package or on the lid or cap that is/are large enough to bridge the narrowest spacing between unglassivated operating materials and are not semiconductor material, glass splatter, gold imperfections in the die attach area, gold eutectic material or package ceramic material.

NOTES

1. As an alternative to 100% visual inspection of lids or caps, the lids or caps may be subjected to a suitable cleaning process and quality verification approved by the qualifying activity. The lids or caps shall subsequently be held in a controlled environment until capping or preparation for seal.

(c) Foreign material attached to, or embedded in, the die surface that appears to bridge the active circuit elements including metallisation. Suspect particles shall cause rejection unless verified as only attached, but not embedded, by high power dark field illumination.

(d) Liquid droplets, chemical stains, ink or photoresist on the die surface that appears to bridge any combination of unglassivated metallisation or bare areas of semiconductor material.

(e) A particle of gold eutectic material, package ceramic material or semiconductor material, not attached to the die, large enough to bridge the narrowest spacing between unglassivated operating materials, that does not exhibit a minimum of 50% cumulative peripheral fillet or whose height is greater than the longest base dimension.

NOTES

1. Gold imperfections in the die attach area that do not interfere with proper die attachment, sealing glass splatter (provided it does not suggest inadequately controlled process and does not interfere with the die attach area) or internal glass runout from frit seal (provided it is confined to package walls and does not interfere with the die attach area) are not rejectable.

4.13 PACKAGE, HEADER OR CAN DEFECTS

(a) Blistering or flaking of the plating or package or leads.

(b) Contamination, such as grease, varnish, ink, resin, on the insulation (ceramic, glass etc).

(c) Excess metallisation which reduces the insulation separation by more than 50%.

(d) Metal shavings on the flange, rim or other cap sealing area with any dimension greater than the width of the sealing/welding area.

(e) Corrosion of the package, header or can.

(f) Cracks in the ceramic body.

(g) Mechanical damage.

(h) Radial cracks that extend in excess of a third of the distance from the pin to the outer member of the seal.

(i) Cracks in the circumference, except the meniscus, that extend more than 90° about the seal centre.

(j) Contamination on the flange, rim or other cap sealing area with any dimension greater than half the width of the sealing/welding area.

(k) Bubbles in the glass to metal seal with dimensions greater than 0.8mm or any cluster of bubbles with a combined dimension greater than the adjacent pin.

(l) Bubbles, or an area of adjacent or interconnecting bubbles, in the seal area larger than 12.5% of the seal area or which are more than half of the distance between the pin and body or pin and pin.

(m) Foreign particles enclosed in the glass seal.

(n) Plating or die attach material overlapping the seals.

(o) Cracked or chipped glass seals. Meniscus chip outs must not exceed 0.2mm in any dimension.