



Pages 1 to 29

**INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS DUAL  
64-STAGE STATIC SHIFT REGISTER WITH 3-STATE  
OUTPUTS**

**BASED ON TYPE 4517B**

**ESCC Detail Specification No. 9306/049**

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DCR No.	CHANGE DESCRIPTION
90	Specification up issued to incorporate editorial and technical changes per DCR.

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## 1. GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

### 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics

### 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

### 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

#### 1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930604901

- Detail Specification Reference: 9306049
- Component Type Variant Number: 01 (as required)

#### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g
01	4517B	FP	G2	0.7
02	4517B	FP	G4	0.7
07	4517B	CCP	2	0.6
08	4517B	DIP	G2	2.2
09	4517B	DIP	G4	2.2
10	4517B	SO	G2	0.7
11	4517B	SO	G4	0.7

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	$V_{DD}$	-0.5 to 18	V	Note 1
Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$	V	Note 1 Power on
Input Current	$I_{IN}$	$\pm 10$	mA	-
Device Power Dissipation (Continuous)	$P_D$	200	mW	-
Power Dissipation per Output	$P_{DSO}$	100	mW	-
Operating Temperature Range	$T_{op}$	-55 to +125	$^{\circ}C$	$T_{amb}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}C$	-
Soldering Temperature For FP, DIP and SO For CCP	$T_{sol}$	+265 +245	$^{\circ}C$	Note 2 Note 3

**NOTES:**

1. Device is functional for  $3V \leq V_{DD} \leq 15V$ .
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

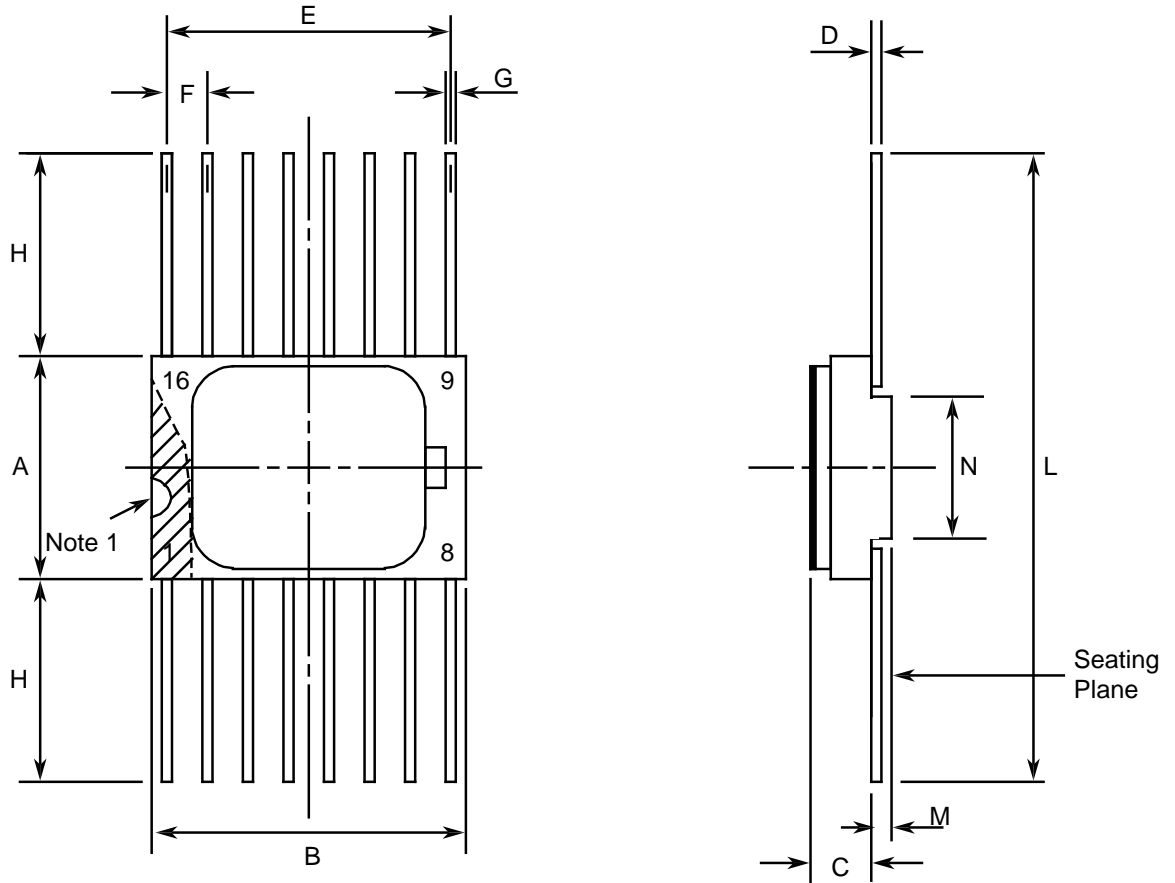
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

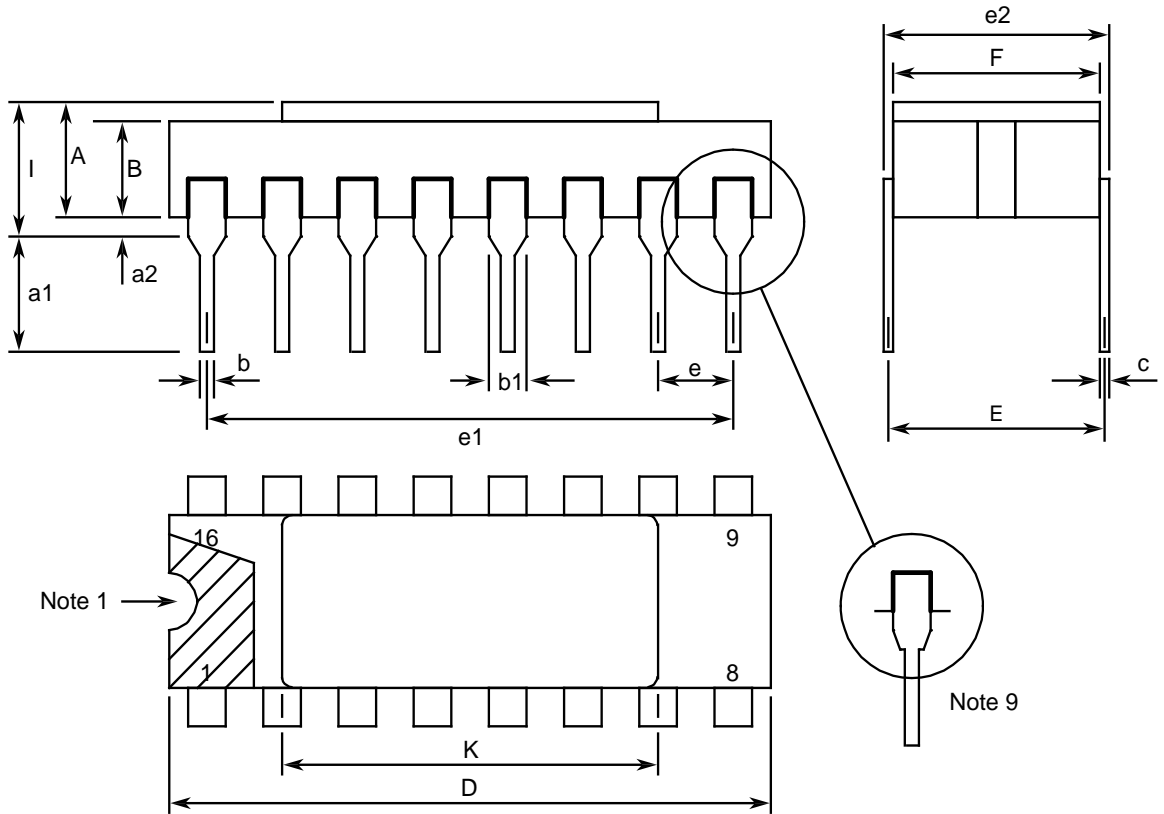
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 TYPICAL		3, 6
G	0.38	0.48	5
H	6	-	5
L	18.75	22	
M	0.33	0.43	
N	4.32 TYPICAL		

1.7.2 Dual-in-line Package (DIP) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.1	2.71	
a1	3	3.7	
a2	0.63	1.14	2
B	1.82	2.39	
b	0.4	0.5	5
b1	1.14	1.5	5
c	0.2	0.3	5
D	20.06	20.58	
E	7.36	7.87	
e	2.54 TYPICAL		4, 6
e1	17.65	17.9	
e2	7.62	8.12	
F	7.29	7.7	
l	-	3.83	



Symbols	Dimensions mm		Notes
	Min	Max	
K	10.9	12.1	

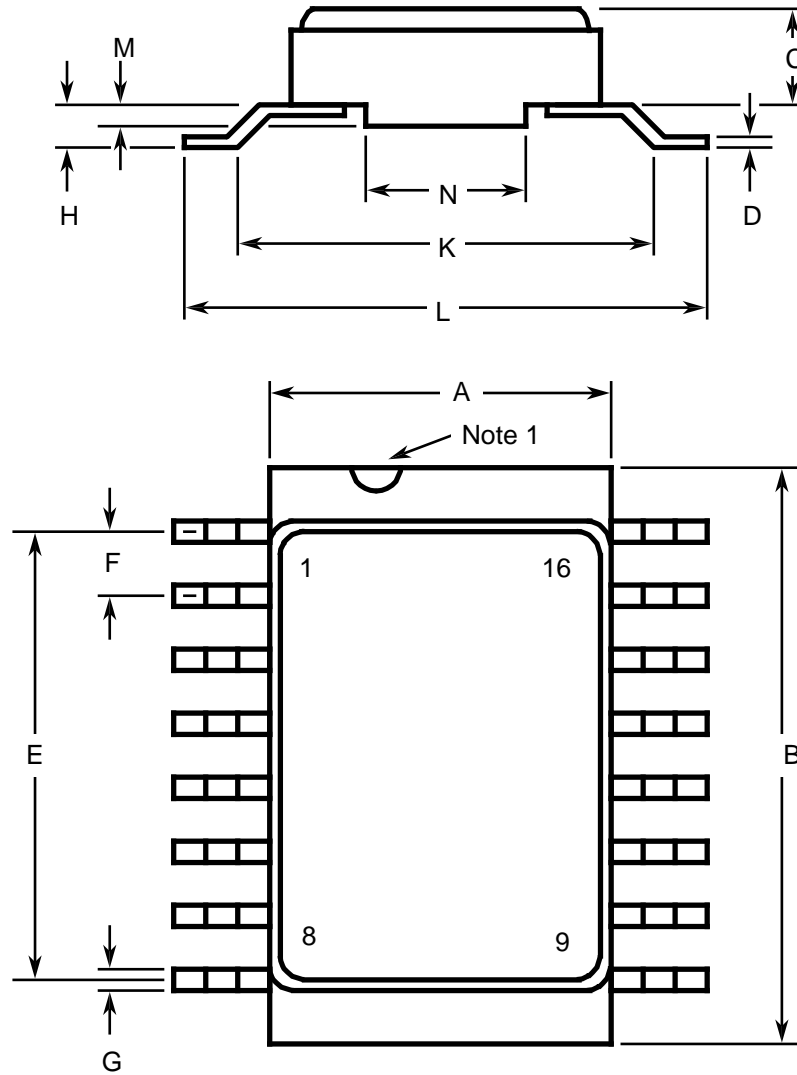
1.7.3 Chip Carrier Package (CCP) - 20 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5
C	1.06	1.47	5
C1	1.91	2.41	

Symbols	Dimensions mm		Notes
	Min	Max	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27 TYPICAL		3, 6
d2	7.62 TYPICAL		
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27 TYPICAL		3, 6
e2	7.62 TYPICAL		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 TYPICAL		3, 6
G	0.38	0.48	5
H	0.6	0.9	5

Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

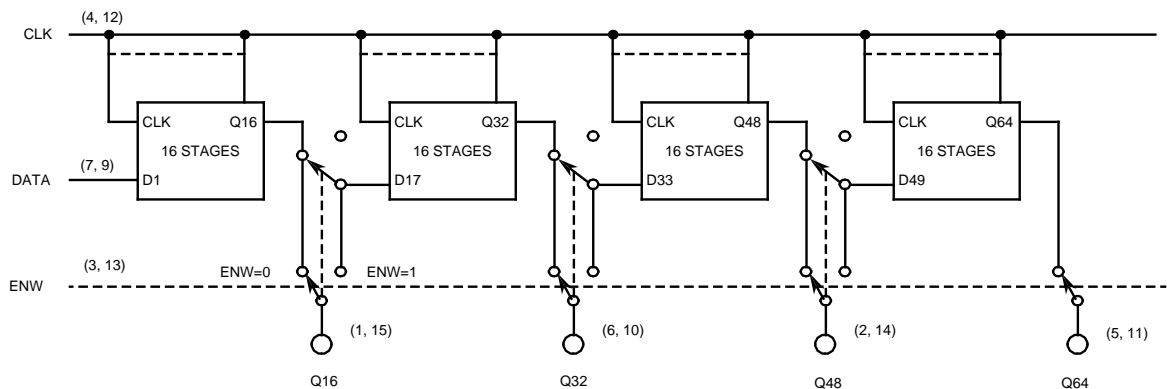
1.7.5 Consolidated Notes

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within  $\pm 0.13\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within  $\pm 0.25\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces for flat, dual-in-line and small outline packages.  
16 spaces for chip carrier packages.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only

EACH REGISTER



1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	1Q16 Output/Input	1Q16 Output/Input	11	2Q64 Output/Input	2DATA Input
2	1Q48 Output/Input	1Q48 Output/Input	12	2CLK Input (Clock)	2Q32 Output/Input
3	1ENW Input (Write Enable)	-	13	2ENW Input (Write Enable)	-
4	1CLK Input (Clock)	1ENW Input (Write Enable)	14	2Q48 Output/Input	2Q64 Output/Input
5	1Q64 Output/Input	1CLK Input (Clock)	15	2Q16 Output/Input	2CLK Input (Clock)
6	1Q32 Output/Input	1Q64 Output/Input	16	V <sub>DD</sub>	2ENW Input (Write Enable)
7	1DATA Input	1Q32 Output/Input	17	-	2Q48 Output/Input
8	V <sub>SS</sub>	-	18	-	-
9	2DATA Input	1DATA Input	19	-	2Q16 Output/Input
10	2Q32 Output/Input	V <sub>SS</sub>	20	-	V <sub>DD</sub>

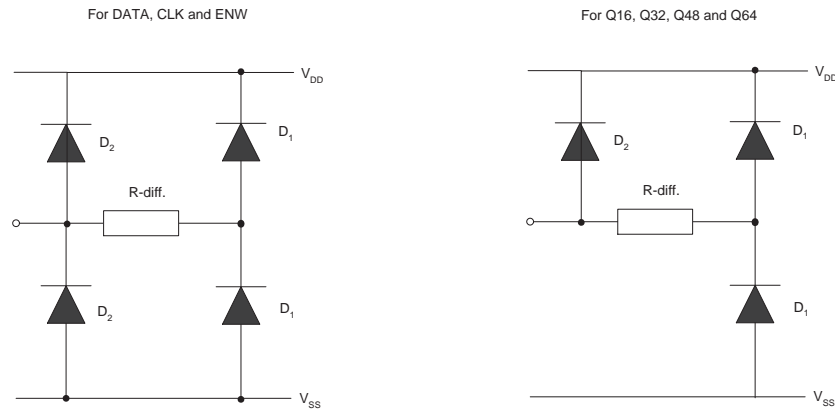
1.10 TRUTH TABLE

- Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance
- ↑ = Transition, Low to High ; ↓ = Transition High to Low

EACH REGISTER

INPUTS			OUTPUTS/INPUTS			
CLK	ENW	DATA	Q16	Q32	Q48	Q64
L	L	X	Q16	Q32	Q48	Q64
L	H	X	Z	Z	Z	Z
H	L	X	Q16	Q32	Q48	Q64
H	H	X	Z	Z	Z	Z
↑	L	D1 In	Q16	Q32	Q48	Q64
↑	H	D1 In	D17 In	D33 In	D49 In	Z
↓	L	X	Q16	Q32	Q48	Q64
↓	H	X	Z	Z	Z	Z

1.11 INPUT PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at  $T_{amb}=+22 \pm 3^{\circ}C$ .

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load $V_{IL}=0V, V_{IH}=3V$ $V_{DD}=3V, V_{SS}=0V$ Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 2	-	-	-
Quiescent Current	$I_{DD}$	3005	$V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 3	-	1	$\mu A$
Low Level Input Current	$I_{IL}$	3009	$V_{IN}$ (Under Test)=0V $V_{DD}=15V, V_{SS}=0V$	-	-50	nA
High Level Input Current	$I_{IH}$	3010	$V_{IN}$ (Under Test)=15V $V_{DD}=15V, V_{SS}=0V$	-	50	nA
Low Level Output Voltage 1	$V_{OL1}$	3007	$V_{IL}=0V, V_{IH}=15V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	$V_{OL2}$	3007	$V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OL}=0A$ $V_{DD}=5V, V_{SS}=0V$	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	$V_{OL3}$	3007	$V_{IL}=4V, V_{IH}=11V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$	-	1.5	V
High Level Output Voltage 1	$V_{OH1}$	3006	$V_{IL}=0V, V_{IH}=15V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	$V_{OH2}$	3006	$V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OH}=0A$ $V_{DD}=5V, V_{SS}=0V$	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	$V_{OH3}$	3006	$V_{IL}=4V, V_{IH}=11V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$	13.5	-	V
Low Level Output Current 1	$I_{OL1}$	-	$V_{IL}=0V, V_{IH}=5V,$ $V_{OL}=0.4V$ $V_{DD}=5V, V_{SS}=0V$ Note 4	510	-	$\mu A$

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Current 2	$I_{OL2}$	-	$V_{IL}=0V, V_{IH}=15V,$ $V_{OL}=1.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4	3.4	-	mA
High Level Output Current 1	$I_{OH1}$	-	$V_{IL}=0V, V_{IH}=5V,$ $V_{OH}=4.6V$ $V_{DD}=5V, V_{SS}=0V$ Note 4	-510	-	$\mu A$
High Level Output Current 2	$I_{OH2}$	-	$V_{IL}=0V, V_{IH}=15V,$ $V_{OH}=13.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4	-3.4	-	mA
Output Leakage Current Third State, Low Level Applied	$I_{OZL}$	3020	$V_{IL}=0V, V_{IH}=15V$ $V_{OL}=0V$ $V_{DD}=15V, V_{SS}=0V$	-	-400	nA
Output Leakage Current Third State, High Level Applied	$I_{OZH}$	3021	$V_{IL}=0V, V_{IH}=15V$ $V_{OH}=15V$ $V_{DD}=15V, V_{SS}=0V$	-	400	nA
Threshold Voltage N-Channel	$V_{THN}$	-	1ENW, 2ENW Inputs at Ground All Other Inputs: $V_{IN}=5V$ $V_{DD}=5V, I_{SS}=-10\mu A$	-0.7	-3	V
Threshold Voltage P-Channel	$V_{THP}$	-	1CLK, Input at Ground All Other Inputs: $V_{IN}=-5V$ $V_{SS}=-5V, I_{DD}=10\mu A$	0.7	3	V
Input Clamp Voltage 1, to $V_{SS}$	$V_{IC1}$	-	$I_{IN}$ (Under Test) = -100 $\mu A$ $V_{DD}$ =Open, $V_{SS}=0V$ All Other Pins Open	-	-2	V
Input Clamp Voltage 2, to $V_{DD}$	$V_{IC2}$	-	$V_{IN}$ (Under Test)=6V $R=30k\Omega, V_{SS}$ =Open All Other Pins Open Note 5	3	-	V
Input Capacitance 1ENW, 2ENW, 1CLK, 2CLK, 1DATA, 2DATA	$C_{IN1}$	3012	$V_{IN}$ (Not Under Test)=0V $V_{DD}=V_{SS}=0V$ $f = 100$ kHz to 1 MHz Note 6	-	7.5	pF



Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Input Capacitance 1Qn, 2Qn	C <sub>IN2</sub>	3012	V <sub>IN</sub> (ENW)=5V V <sub>IN</sub> (Remaining Inputs Not Under Test)=0V V <sub>DD</sub> =V <sub>SS</sub> =0V f = 100 kHz to 1 MHz Note 6	-	7.5	pF
Propagation Delay Low to High, 1CLK to 1Q16, 2CLK to 2Q16	t <sub>PLH</sub>	3003	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	400	ns
Propagation Delay High to Low, 1CLK to 1Q16, 2CLK to 2Q16	t <sub>PHL</sub>	3003	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	400	ns
Output Disable Time Low Output to High Impedance, 1ENW to 1Q32, 2ENW to 2Q32	t <sub>PLZ</sub>	3003	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	150	ns
Output Enable Time High Impedance to Low Output, 1ENW to 1Q32, 2ENW to 2Q32	t <sub>PZL</sub>	3003	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	150	ns
Output Disable Time High Output to High Impedance, 1ENW to 1Q32, 2ENW to 2Q32	t <sub>PHZ</sub>	3003	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	150	ns
Output Enable Time High Impedance to High Output, 1ENW to 1Q32, 2ENW to 2Q32	t <sub>PZH</sub>	3003	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	150	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Transition Time Low to High, 1Q16, 2Q16	t <sub>TLH</sub>	3004	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	200	ns
Transition Time High to Low, 1Q16, 2Q16	t <sub>THL</sub>	3004	V <sub>IN</sub> (Under Test)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Note 7	-	200	ns
Maximum Clock Frequency	f <sub>CLK</sub>	-	V <sub>IN</sub> (CLK)=Pulse Generator V <sub>IN</sub> (Remaining Inputs)=Truth Table V <sub>IL</sub> =0V, V <sub>IH</sub> =5V, V <sub>DD</sub> =5V, V <sub>SS</sub> =0V Notes 8, 9	3	-	MHz

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T<sub>amb</sub>=+125 (+0 -5) °C and T<sub>amb</sub>=- 55(+5-0)°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V <sub>IL</sub> =0V, V <sub>IH</sub> =3V V <sub>DD</sub> =3V, V <sub>SS</sub> =0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V <sub>IL</sub> =0V, V <sub>IH</sub> =15V V <sub>DD</sub> =15V, V <sub>SS</sub> =0V Note 2	-	-	-
Quiescent Current	I <sub>DD</sub>	3005	V <sub>IL</sub> =0V, V <sub>IH</sub> =15V V <sub>DD</sub> =15V, V <sub>SS</sub> =0V Note 3 T <sub>amb</sub> =+125°C T <sub>amb</sub> =- 55°C	- -	30 1	µA
Low Level Input Current	I <sub>IL</sub>	3009	V <sub>IN</sub> (Under Test)=0V V <sub>DD</sub> =15V, V <sub>SS</sub> =0V T <sub>amb</sub> =+125°C T <sub>amb</sub> =- 55°C	- -	-100 -50	nA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Input Current	$I_{IH}$	3010	$V_{IN}$ (Under Test)=15V $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	- -	100 50	nA
Low Level Output Voltage 1	$V_{OL1}$	3007	$V_{IL}=0V, V_{IH}=15V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	$V_{OL2}$	3007	$V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OL}=0A$ $V_{DD}=5V, V_{SS}=0V$	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	$V_{OL3}$	3007	$V_{IL}=4V, V_{IH}=11V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$	-	1.5	V
High Level Output Voltage 1	$V_{OH1}$	3006	$V_{IL}=0V, V_{IH}=15V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	$V_{OH2}$	3006	$V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OH}=0A$ $V_{DD}=5V, V_{SS}=0V$	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	$V_{OH3}$	3006	$V_{IL}=4V, V_{IH}=11V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$	13.5	-	V
Low Level Output Current 1	$I_{OL1}$	-	$V_{IL}=0V, V_{IH}=5V,$ $V_{OL}=0.4V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	360 640	- -	$\mu A$
Low Level Output Current 2	$I_{OL2}$	-	$V_{IL}=0V, V_{IH}=15V,$ $V_{OL}=1.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	2.4 4.2	- -	mA
High Level Output Current 1	$I_{OH1}$	-	$V_{IL}=0V, V_{IH}=5V,$ $V_{OH}=4.6V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	-360 -640	- -	$\mu A$
High Level Output Current 2	$I_{OH2}$	-	$V_{IL}=0V, V_{IH}=15V,$ $V_{OH}=13.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	-2.4 -4.2	- -	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Leakage Current Third State, Low Level Applied	$I_{OZL}$	3020	$V_{IL}=0V, V_{IH}=15V$ $V_{OL}=0V$ $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	- - -	-12 -0.4	$\mu A$
Output Leakage Current Third State, High Level Applied	$I_{OZH}$	3021	$V_{IL}=0V, V_{IH}=15V$ $V_{OH}=15V$ $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	- - -	12 0.4	$\mu A$
Threshold Voltage N-Channel	$V_{THN}$	-	1ENW, 2ENW Inputs at Ground All Other Inputs: $V_{IN}=-5V$ $V_{DD}=-5V, I_{SS}=-10\mu A$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	-0.3 -0.7	-3.5 -3.5	V
Threshold Voltage P-Channel	$V_{THP}$	-	1CLK Input at Ground All Other Inputs: $V_{IN}=-5V$ $V_{SS}=-5V, I_{DD}=10\mu A$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$	0.3 0.7	3.5 3.5	V

2.3.3 Notes to Electrical Measurement Tables

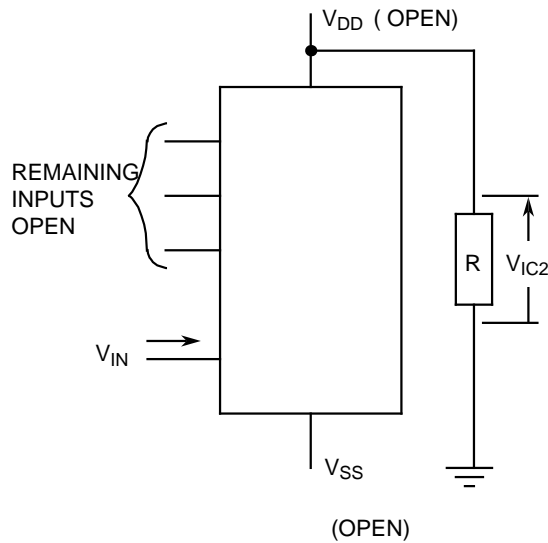
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be  $V_{IN} = V_{SS}$  or  $V_{DD}$  and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with  $V_{OH} \geq V_{DD} - 0.5V$ ,  $V_{OL} \leq 0.5V$ . The Maximum time to output comparator strobe = 300 $\mu s$ .
3. Quiescent Current shall be tested using the following input conditions where 1 =  $V_{IH}$  and 0 =  $V_{IL}$ :

IDD Test No.	Input Pattern No.	Input Conditions													
		1Q16	1Q32	1Q48	1Q64	1ENW	1CLK	1DATA	2Q16	2Q32	2Q48	2Q64	2ENW	2CLK	2DATA
	1					0	0	0					0	0	0
	2					0	1	0					0	1	0
	3					0	0	1					0	0	1
	4					0	1	1					0	1	1
	5					0	0	0					0	0	0
	Repeat 1 to 5, 31 times														
	156					0	1	0					0	1	0
	157					0	0	1					0	0	1
	158					0	1	1					0	1	1

IDD Test No.	Input Pattern No.	Input Conditions													
		1Q16	1Q32	1Q48	1Q64	1ENW	1CLK	1DATA	2Q16	2Q32	2Q48	2Q64	2ENW	2CLK	2DATA
(a)	159					0	0	1					0	0	1
(b)	160					0	0	0					0	0	0
(c)	161					0	1	1					0	1	1
(d)	162					0	1	0					0	1	0
	163	0	0	0	0	1	1	0	0	0	0	0	1	1	0
(e)	164	0	0	0	0	1	0	0	0	0	0	0	1	0	0
(f)	165	1	1	1	1	1	0	1	1	1	1	1	1	0	1
(g)	166	0	0	0	0	1	1	0	0	0	0	0	1	1	0
(h)	167	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	168					0	0	0					0	0	0
	169					0	1	0					0	1	0
	170					0	0	0					0	0	0
Repeat 168 to 170, 31 times															
(i)	260					0	0	0					0	0	0
(j)	261					0	1	0					0	1	0
(k)	262					0	0	1					0	0	1
(l)	263					0	1	1					0	1	1
	264					0	0	0					0	0	0
	265					0	1	0					0	1	0
	266					0	0	1					0	0	0
	267					0	1	1					0	1	0
	268					0	0	0					0	0	0
Repeat 264 to 268, 30 times															
(m)	413					0	0	0					0	0	0
(n)	414					0	1	0					0	1	0
(o)	415					0	0	0					0	0	1
(p)	416					0	1	0					0	1	1
	417					0	0	0					0	0	0
	418					0	1	0					0	1	0
	419					0	0	0					0	0	1
	420					0	1	0					0	1	1
	421					0	0	0					0	0	0
Repeat 417 to 421, 60 times															
(q)	716					0	0	0					0	0	0

IDD Test No.	Input Pattern No.	Input Conditions													
		1Q16	1Q32	1Q48	1Q64	1ENW	1CLK	1DATA	2Q16	2Q32	2Q48	2Q64	2ENW	2CLK	2DATA
(r)	717					0	1	0					0	1	0
(s)	718					0	0	1					0	0	1
(t)	719					0	1	1					0	1	1
	720					0	0	0					0	0	0
	721					0	1	0					0	1	0
	722					0	0	1					0	0	1
	723					0	1	1					0	1	1
	724					0	0	1					0	0	1
Repeat 720 to 724, 30 times															
(u)	869					0	0	1					0	0	1
(v)	870					0	1	1					0	1	1

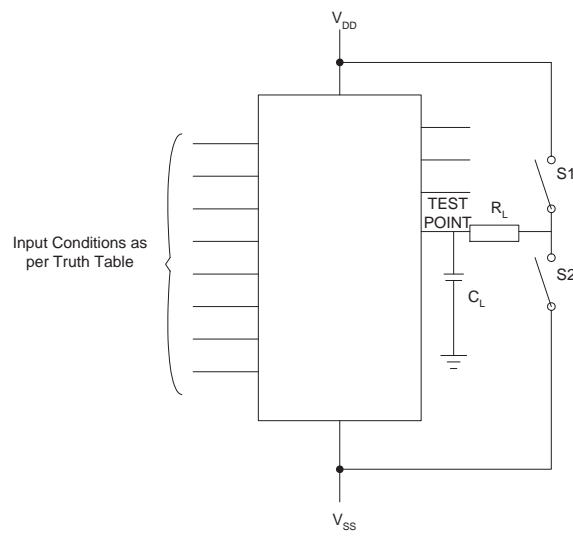
4. Interchange of forcing and measuring parameters is permitted.
5. Input Clamp Voltage 2 to  $V_{DD}$ ,  $V_{IC2}$ , shall be tested on each input as follows:-



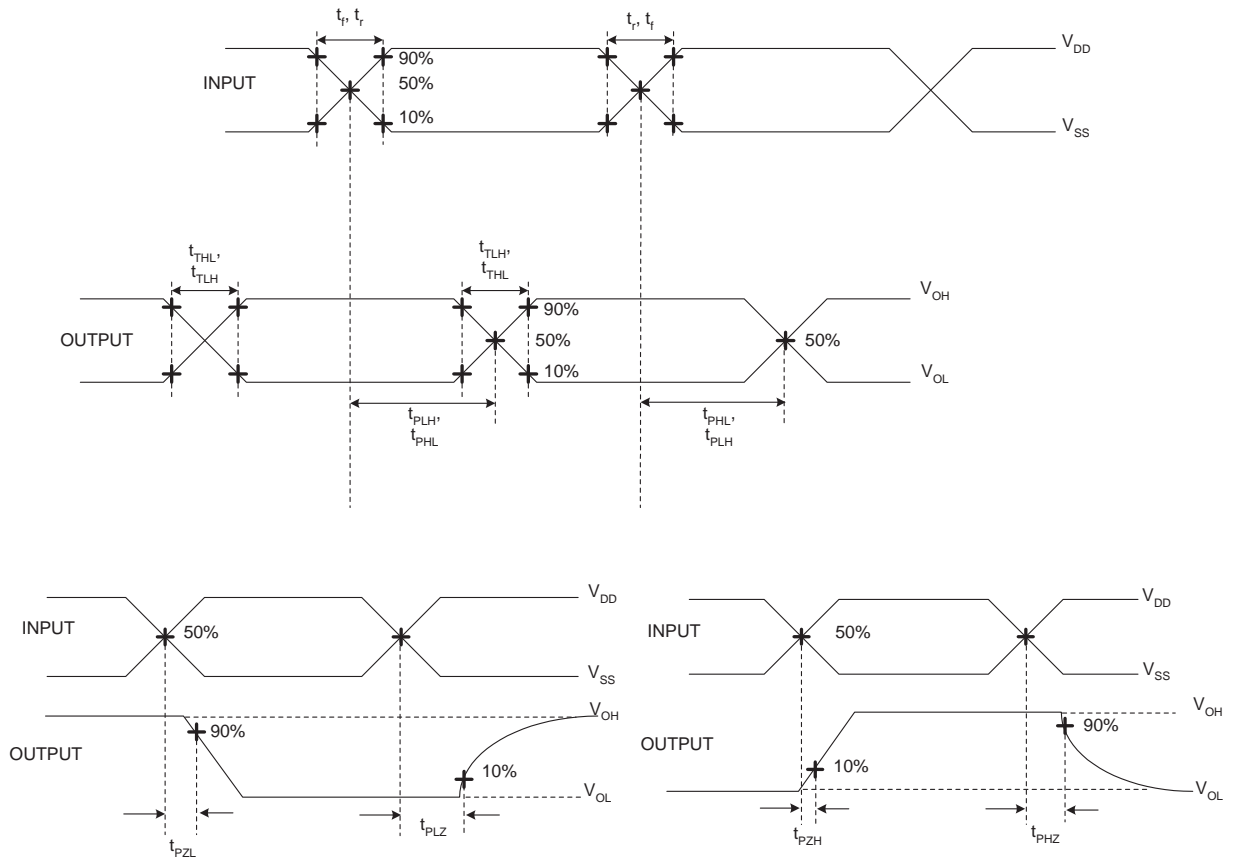
6. Guaranteed but not tested.
7. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.  
The pulse generator shall have the following characteristics:

$V_{GEN} = 0$  to  $V_{DD}$ ;  $f = 500\text{kHz}$ ;  $t_r$  and  $t_f \leq 15 \text{ ns}$  (10% to 90%); duty cycle = 50%. Output load capacitance  $C_L = 50\text{pF} \pm 5\%$  including scope probe, wiring and stray capacitance without component in the test fixture.

Propagation delay and transition times shall be measured as follows:



Parameter	RL	S1	S2
$t_{pZH}$	1k $\Omega$	Open	Closed
$t_{pZL}$		Closed	Open
$t_{pHZ}$		Open	Closed
$t_{pLZ}$		Closed	Open
$t_{pHL}, t_{pLH}, t_{pTHL}, t_{pTLH}$	200k $\Omega$	Open	Closed



8. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
9. A pulse, having the following conditions, shall be applied to the CLK inputs:  $V_P = 0V$  to  $V_{DD}$ . Maximum clock frequency  $f_{CLK}$  requirement shall be considered as met if proper output state changes occur with the pulse repetition rate set to that given in the Limits column.

## 2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^\circ C$ .

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.



Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Quiescent Current	$I_{DD}$	$\pm 0.15$	-	1	$\mu A$
Low Level Output Current 1	$I_{OL1}$	$\pm 15\% (2)$	510	-	$\mu A$
High Level Output Current 1	$I_{OH1}$	$\pm 15\% (2)$	-510	-	$\mu A$
Output Leakage Current Third State, Low Level Applied	$I_{OZL}$	$\pm 60$	-	-400	nA
Output Leakage Current Third State, High Level Applied	$I_{OZH}$	$\pm 60$	-	400	nA
Threshold Voltage N-Channel	$V_{THN}$	$\pm 0.3$	-0.7	-3	V
Threshold Voltage P-Channel	$V_{THP}$	$\pm 0.3$	0.7	3	V

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Percentage of limit value if voltage is the measuring parameter.

2.5

**INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS**

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements .

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Quiescent Current	$I_{DD}$	$\pm 0.15$	-	1	$\mu A$
Low Level Input Current	$I_{IL}$	-	-	-50	nA
High Level Input Current	$I_{IH}$	-	-	50	nA
Low Level Output Voltage 1	$V_{OL1}$	-	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	$V_{OL2}$	-	-	500	mV
High Level Output Voltage 1	$V_{OH1}$	-	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	$V_{OH2}$	-	4.5	-	V
Low Level Output Current 1	$I_{OL1}$	$\pm 15\%$ (3)	510	-	$\mu A$
Low Level Output Current 2	$I_{OL2}$	$\pm 15\%$ (3)	3.4	-	mA
High Level Output Current 1	$I_{OH1}$	$\pm 15\%$ (3)	-510	-	$\mu A$
High Level Output Current 2	$I_{OH2}$	$\pm 15\%$ (3)	-3.4	-	mA
Output Leakage Current Third State, Low Level Applied	$I_{OZL}$	$\pm 60$	-	-400	nA
Output Leakage Current Third State, High Level Applied	$I_{OZH}$	$\pm 60$	-	400	nA
Threshold Voltage N-Channel	$V_{THN}$	$\pm 0.3$	-0.7	-3	V
Threshold Voltage P-Channel	$V_{THP}$	$\pm 0.3$	0.7	3	V

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values ( $\Delta$ ) are applicable to the Operating Life test only.
3. Percentage of limit value if voltage is the measuring parameter.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	°C
Outputs 1Q64, 2Q64	$V_{OUT}$	Open	V
Inputs 1Q16, 1Q32, 1Q48, 2Q16, 2Q32, 2Q48, 1DATA	$V_{IN}$	$V_{SS}$	V
Inputs 1ENW, 2ENW, 1CLK, 2CLK, 2DATA	$V_{IN}$	$V_{DD}$	V
Positive Supply Voltage	$V_{DD}$	15 (+0 -0.5)	V
Negative Supply Voltage	$V_{SS}$	0	V
Duration	t	72	Hours

**NOTES:**

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	°C
Outputs 1Q64, 2Q64	$V_{OUT}$	Open	V
Inputs 1Q16, 1Q32, 1Q48, 2Q16, 2Q32, 2Q48, 1DATA	$V_{IN}$	$V_{DD}$	V
Inputs 1ENW, 2ENW, 1CLK, 2CLK, 2DATA	$V_{IN}$	$V_{SS}$	V
Positive Supply Voltage	$V_{DD}$	15 (+0 -0.5)	V
Negative Supply Voltage	$V_{SS}$	0	V
Duration	t	72	Hours

**NOTES:**

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	°C
Output 1Qn, 2Qn	$V_{OUT}$	$V_{DD}/2$	V
Inputs 1ENW, 2ENW	$V_{IN}$	$V_{SS}$	V
Inputs 1CLK, 2CLK	$V_{IN}$	$V_{GEN1}$	V
Inputs 1DATA, 2DATA	$V_{IN}$	$V_{GEN2}$	V
Pulse Voltage	$V_{GEN}$	0V to $V_{DD}$	V
Pulse Frequency Square Wave	$f_{GEN1}$ $f_{GEN2}$	50k 25k 50% Duty Cycle	Hz
Positive Supply Voltage	$V_{DD}$	15 (+0 -0.5)	V
Negative Supply Voltage	$V_{SS}$	0	V

**NOTES:**

1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

**APPENDIX 'A'**

**AGREED DEVIATIONS FOR STMICROELECTRONICS (F)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
<p>Deviations from Screening Tests - Chart F3</p>	<p>External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p> <p>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.</p>
<p>Deviations from Qualification and Periodic Tests - Chart F4</p>	<p>External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p>
<p>Deviations from High and Low Temperatures Electrical Measurements</p>	<p>High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>
<p>Deviations from Room Temperature Electrical Measurements</p>	<p>All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>