TRANSISTORS, FIELD-EFFECT, N-CHANNEL,

BASED ON TYPES 2N4091/4092/4093

ESCC Detail Specification No. 5205/007

ISSUE 1

October 2002

Document Custodian: European Space Agency - see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

european space agency
agence spatiale européenne

Pages 1 to 19

TRANSISTORS, FIELD-EFFECT, N-CHANNEL,

BASED ON TYPES 2N4091/4092/4093

ESA/SCC Detail Specification No. 5205/007

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 2	March 1979	-	-
Revision 'A'	February 1992		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference / Item	Approved DCR No.
'A'	Feb. '92	This Issue incorporates all modifications agreed on the basis of Policy DCR 21016 for adaptation to new qualification requirements	
		P1. Cover page	None
		P2. DCN	None
		P4. Table of Contents : "Appendices" Title added	21019
		P5. Para. 1.2 : Paragraph amended	21021
		P6. Table 1(a) : "Lead Material and/or Finish" column added	21025
		P9. Para. 2 : MIL-STD-1276 deleted, "ESA/SCC Basic Spec. No. 23500" added	21025
		Para. 4.1 : Additional text added	21019
		Para. 4.2.2 : PIND deviation deleted	21043
		P10. Para. 4.4.2 : Paragraph amended	21025
		P16. Table 3 : Note deleted	21047
		This document has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.	

TABLE OF CONTENTS

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for Transistors, Field-Effect, N-Channel based on Types 2N4091, 2N4092 and 2N4093.

It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

See Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The applicable derating information for the transistors specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification of the transistors specified herein, is shown in Figure 3.

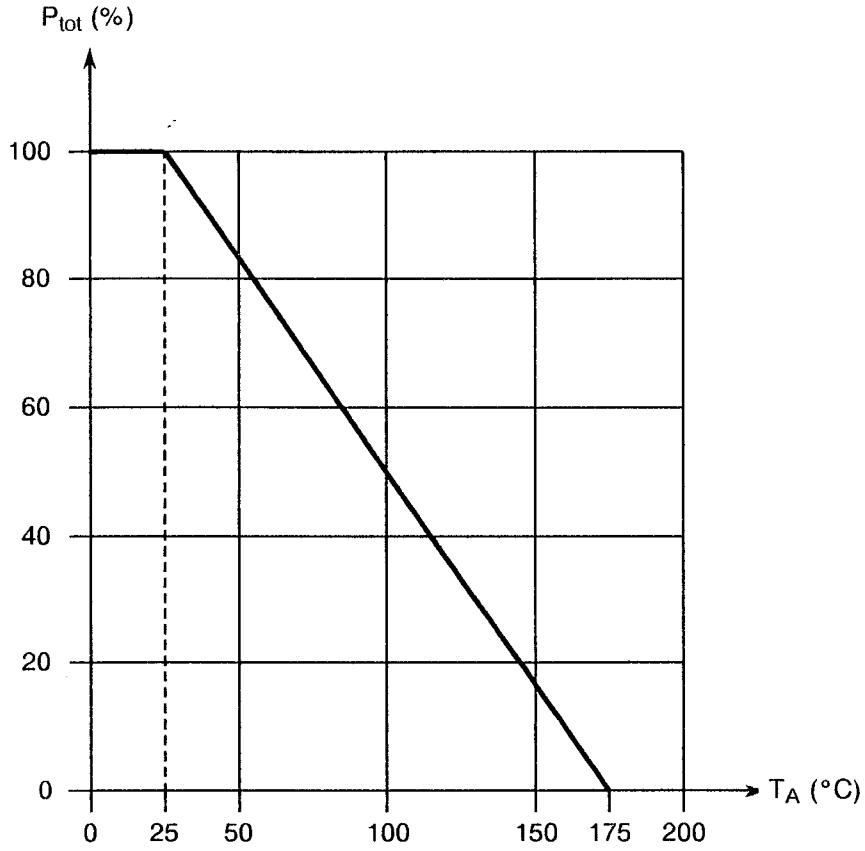
TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CHARACTERISTICS	LEAD MATERIAL AND FINISH
01	2N4091	See Table 2	D2
02	2N4092		
03	2N4093		

TABLE 1(b) - MAXIMUM RATINGS

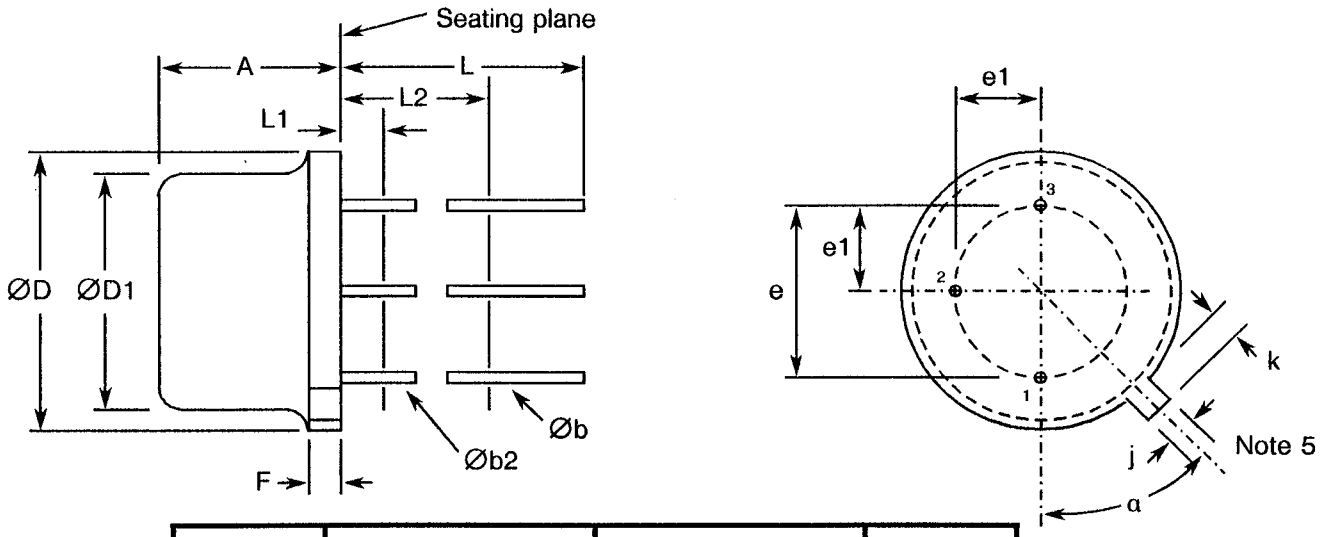
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain Source Voltage	V_{DS}	40	V	
2	Gate Source Voltage	V_{GS}	−40	V	
3	Gate Drain Voltage	V_{GD}	−40	V	
4	Gate Current	I_G	10	mA	
5	Total Power Dissipation (see Figure 1)	P_{tot}	300	mW	T_{amb} = +25°C
6	Operating Temperature Range	T_{op}	−55 to +175	°C	T_{amb}
7	Storage Temperature Range	T_{stg}	−65 to +200	°C	
8	Soldering Temperature	T_{sol}	+235	°C	Time ≤ 10 sec. Distance to case: ≥ 1.5mm

FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

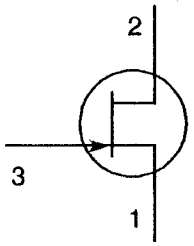


SYMBOL	INCHES		MILLIMETRES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
Øb	0.016	0.021	0.406	0.533	1
Øb2	0.016	0.019	0.406	0.483	1
ØD	0.209	0.230	5.31	5.84	
ØD1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		2, 4
e1	0.050 T.P.		1.27 T.P.		2, 4
F	-	0.030	-	0.762	
j	0.036	0.046	0.914	1.17	4
k	0.028	0.048	0.711	1.22	3
L	0.500	-	12.70	-	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
α	45° T.P.		45° T.P.		5

NOTES

1. (3 leads) Øb2 applies between L1 and L2. Øb applies between L2 and 0.5 inch (12.70mm) from seating plane. Diameter is uncontrolled in L1 and beyond 0.5 inch (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019 inch (0.483mm) measured in gauging plane 0.054 inch (1.37mm) + 0.001 inch (0.025mm) − 0.000 inch (0.000mm) below the seating plane of the device shall be within 0.007 inch (0.178mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. The device may be measured by direct methods or by the gauge and gauging procedure described on gauge drawing GS-2.
5. Tab centreline.

FIGURE 3 - FUNCTIONAL DIAGRAM



1. Source.
2. Drain.
3. Gate (connected to case).

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

(c) ESA/SCC Basic Specification No. 23500, Requirements for Lead Materials and Finishes for Components for Space Application.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductors. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

High Temperature Reverse Bias Test (H.T.R.B.) is not required.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 0.9 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition: 'A', Tension.
Applied Force: 5.0 Newtons.
Duration: 10 seconds.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

Metal case, hermetically sealed, similar to JEDEC TO-18.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

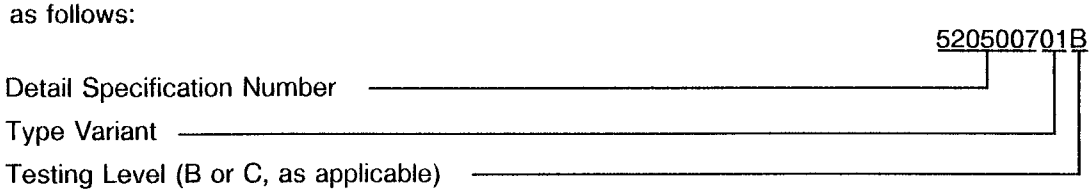
(c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Burn-in

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Total Gate Leakage Current	I_{GSS}	MIL-STD-750 Method 3411	V_{DS} = 0V V_{GS} = −20V	-	−0.2	nA
2	Gate Source Breakdown Voltage	$V_{(BR)GSS}$	MIL-STD-750 Method 3401	V_{DS} = 0V I_G = −1.0µA	−40	-	V
3	Drain Cut-off Current - Variant 01 - Variant 02 - Variant 03	I_{DSX}	MIL-STD-750 Method 3413	V_{DS} = 20V V_{GS} = −12V V_{GS} = −8.0V V_{GS} = −6.0V	-	−0.2	nA
4	Drain Current - Variant 01 - Variant 02 - Variant 03	I_{DSS}	MIL-STD-750 Method 3413	V_{DS} = 20V V_{GS} = 0V Note 1	 30 15 8.0	 - - -	mA
5	Gate Source Cut-off Voltage - Variant 01 - Variant 02 - Variant 03	V_{GSoff}	MIL-STD-750 Method 3403	V_{DS} = 20V I_D = 1.0nA	 −5.0 −2.0 −1.0	 −10 −7.0 −5.0	V
6	Drain Source Saturation Voltage - Variant 01 - Variant 02 - Variant 03	V_{Dsat}	MIL-STD-750 Method 3405	V_{GS} = 0V I_D = 6.6mA I_D = 4.0mA I_D = 2.5mA	-	0.2	V
7	On-State Drain Source Resistance - Variant 01 - Variant 02 - Variant 03	r_{DSon}	MIL-STD-750 Method 3421	V_{GS} = 0V I_D = 1.0mA	 - - -	 30 50 80	Ω

NOTES

1. Pulse measurement: Pulse length ≤300µs, Duty Cycle ≤2%.

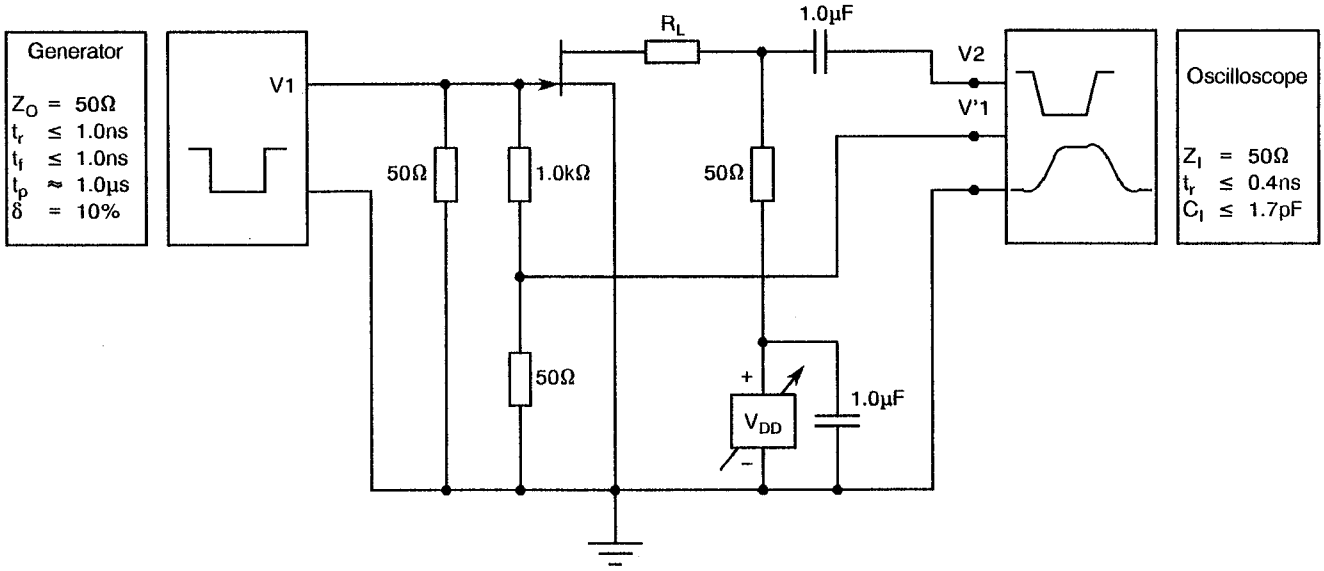
TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	On-State Drain Source Resistance - Variant 01 - Variant 02 - Variant 03	$r_{DS(on)}$	MIL-STD-750 Method 3423	V_{GS} = 0V I_D = 0A f = 1.0kHz	 - - -	 30 50 80	Ω
2	Input Capacitance	C_{iss}	MIL-STD-750 Method 3431	V_{GS} = 0V V_{DS} = 0V f = 1.0MHz	-	28	pF
3	Reverse Transfer Capacitance	C_{rss}	MIL-STD-750 Method 3433	V_{DS} = 0V V_{GS} = −20V f = 1.0MHz	-	5.0	pF
4	Rise Time - Variant 01 - Variant 02 - Variant 03	t_r	See Figure 4	V_{GS} = 0V V_{GSX} = −12V I_D = 6.6mA V_{GSX} = −8.0V I_D = 4.0mA V_{GSX} = −6.0V I_D = 2.5mA	 - - -	 10 20 40	ns
5	Turn-on Delay Time - Variant 01 - Variant 02 - Variant 03	$t_{d(on)}$	See Figure 4	V_{GS} = 0V V_{GSX} = −12V I_D = 6.6mA V_{GSX} = −8.0V I_D = 4.0mA V_{GSX} = −6.0V I_D = 2.5mA	 - - -	 15 15 20	ns
6	Turn-off Time - Variant 01 - Variant 02 - Variant 03	$t_{(off)}$	See Figure 4	V_{GS} = 0V V_{GSX} = −12V I_D = 6.6mA V_{GSX} = −8.0V I_D = 4.0mA V_{GSX} = −6.0V I_D = 2.5mA	 - - -	 40 60 80	ns

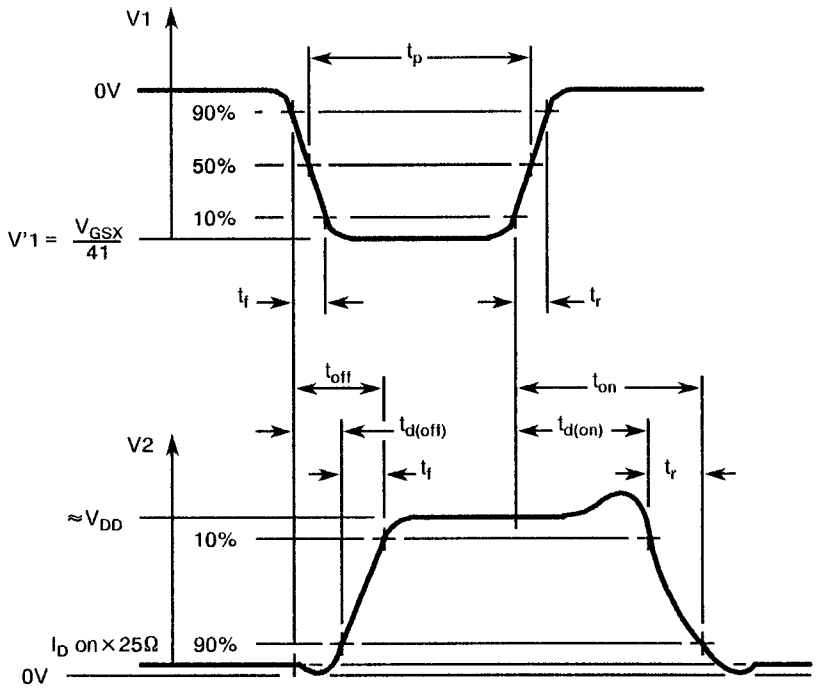
NOTES

1. If more than 20 units have to be measured, the measurements shall be made on a sample basis in accordance with Para. 7.4.2 of ESA/SCC Generic Specification No. 5000. Inspection Level II with an AQL = 2.5%.

FIGURE 4 - SWITCHING TIMES TEST CIRCUIT



V_{GSX} = −12V (2N4091); −8.0V (2N4092); −6.0V (2N4093)



I_D on ≈ 6.6mA (2N4091); 4.0mA (2N4092); 2.5mA (2N4093)

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Total Gate Leakage Current	I_{GSS}	MIL-STD-750 Method 3411	$V_{DS} = 0V$ $V_{GS} = -20V$ $T_{amb} = +150°C$	-	-0.4	µA
2	Drain Cut-off Current - Variant 01 - Variant 02 - Variant 03	I_{DSX}	MIL-STD-750 Method 3413	$V_{DS} = 20V$ $T_{amb} = +150°C$ $V_{GS} = -12V$ $V_{GS} = -8.0V$ $V_{GS} = -6.0V$	-	0.4	µA

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Total Gate Leakage Current	I_{GSS}	MIL-STD-750 Method 3411	$V_{DS} = 0V$ $V_{GS} = -20V$	±100 or (2) ±100	% pA
2	Gate Source Cut-off Voltage	$V_{GS(off)}$	MIL-STD-750 Method 3403	$V_{DS} = 20V$ $I_D = 1.0nA$	±10	%
3	Drain Current	I_{DSS}	MIL-STD-750 Method 3413	$V_{DS} = 20V$ $V_{GS} = 0V$ Note 1	±15	%

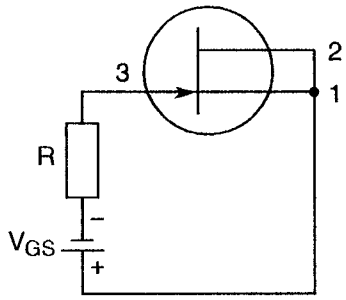
NOTES

1. Pulse measurement: Pulse length ≤300µs, Duty Cycle ≤2%
2. Whichever is greater.

TABLE 5 - CONDITIONS FOR BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	150	°C
2	Drain Source Voltage	V_{DS}	0	V
3	Gate Source Voltage	V_{GS}	−28	V

FIGURE 5 - ELECTRICAL CIRCUITS FOR BURN-IN



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in Table 6.

4.8.3 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be as specified in Table 5 for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be as shown in Figure 5 for burn-in.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Total Gate Leakage Current	I_{GSS}	MIL-STD-750 Method 3411	V_{DS} = 0V V_{GS} = −20V	-	−0.2	nA
2	Gate Source Cut-off Voltage - Variant 01 - Variant 02 - Variant 03	$V_{GS(off)}$	MIL-STD-750 Method 3403	V_{DS} = 20V I_D = 1.0nA	 −5.0 −2.0 −1.0	 −10 −7.0 −5.0	V
3	Drain Current - Variant 01 - Variant 02 - Variant 03	I_{DSS}	MIL-STD-750 Method 3413	V_{DS} = 20V V_{GS} = 0V Note 1	 30 15 8.0	 - - -	mA

NOTES

1. Pulse measurement: Pulse length ≤300μs, Duty Cycle ≤2%