TRANSISTORS, POWER, FET, N-CHANNEL,

BASED ON TYPES 2N6764, 2N6766 AND 2N6768

ESCC Detail Specification No. 5205/013

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ESA/SCC Detail Specification No. 5205/013

space components
coordination group

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		SCCG Chairman	ESA Director General or his Deputy
Issue 2	March 1983	-	-
Revision A	Sept. 1989		
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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This issue supersedes Issue 1 and incorporates all modifications agreed on the basis of Policy DCR 21022, Policy DCR 21019 (Appendices to Detail Specifications), Policy DCR 21025 and the following DCR's:-		
		Cover page		None
		DCN		None
		Table 1(a)	: Column 10, g_{fs} ratings modified	22203
			: Column 11, I_D conditions modified	22203
		Table 1(b)	: Note 3 amended to refer to rating No. 4	22203
		Notes 3 and 5	: "greater than" changed to "less than" signs	22203
		Figure 2	: Note for Variant 03 min. dimension changed to 1.09mm	22203
		Safe Operating Area Test Method: Drain Supply Voltage varied I/O set value		22203
		Table 2	: No. 6; See Fig. 4(a) added	22203
		Table 2 a.c.	: Figure 4 changed to Fig. 4(b)	22203
		New Figure 4(a)	: Added	22203
		Figure 4	: Changed to Fig. 4(b)	22203
'A'	Sept. 89	P1. Cover page		None
		P2. DCN		None
		P10. Para. 4.2.1	: Deleted Method 2077 of MIL-STD-750 and inserted ESA/SCC 21400.	22535
		P12. Para. 4.4.1	: Deleted "and shall be nickel plated"	22737
'B'	Feb. '92	P1. Cover Page		None
		P2. DCN		None
		P5. Para. 1.2	: Paragraph amended	21021
		P6. Table 1(a)	: "Lead Material and/or Finish" column added	21025
		P10. Para. 2	: "ESA/SCC Basic Spec. No. 23500" added	21025
		Para. 4.2.2	: PIND deviation deleted	21043
		P11. Para. 4.2.3	: H.T.R.B. deviation deleted, subsequent deviations renumbered	23499
			: Radiographic Inspection deviation deleted	21049
		Para. 4.2.4	: Bond Strength and Die Shear Test deviations deleted	23499
		P12. Para. 4.4.2	: Paragraph amended	21025
		P18. Table 3	: Note 1 put under this table	21047

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
'C'	March '93	P1. Cover page		None
		P2A. DCN	: New page	None
		P16. Table 2	: Limits for item 8 amended	22972
		P17. Table 2	: Limits for item 13 amended	22972
		This document has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.		

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for N-channel, enhancement-mode, MOSFET, Power Transistors, based on Types 2N6764, 2N6766 and 2N6768. It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

See Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information applicable to the transistors specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification, of the transistors specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling.

TABLE 1(a) - TYPE VARIANTS

(1) VARIANT	(2) TYPE	(3) V_{DS} (MAX.) (V)	(4) V_{DGR} (MAX.) (V)	(5) I_D (MAX.) (A)	(6) I_{LM} (MAX.) (A)	(7) BV_{DSS} (V)	(8) $R_{DS(on)}$ (Ω)	(9) I_D for $R_{DS(on)}$ (A)	(10) g_{fs} (S)	(11) I_D for g_{fs} (A)	(12) $R_{DS(on)}$ at + 125(+ 0-5)°C (Ω)	(13) LEAD MATERIAL AND FINISH
01	2N6764	100	100	28	70	100	0.055	24	9.0	14	0.1	H or I4
02	2N6766	200	200	20	60	200	0.085	19	9.0	19	0.2	H or I4
03	2N6768	400	400	11	25	400	0.300	9.0	8.0	9.0	0.7	F4

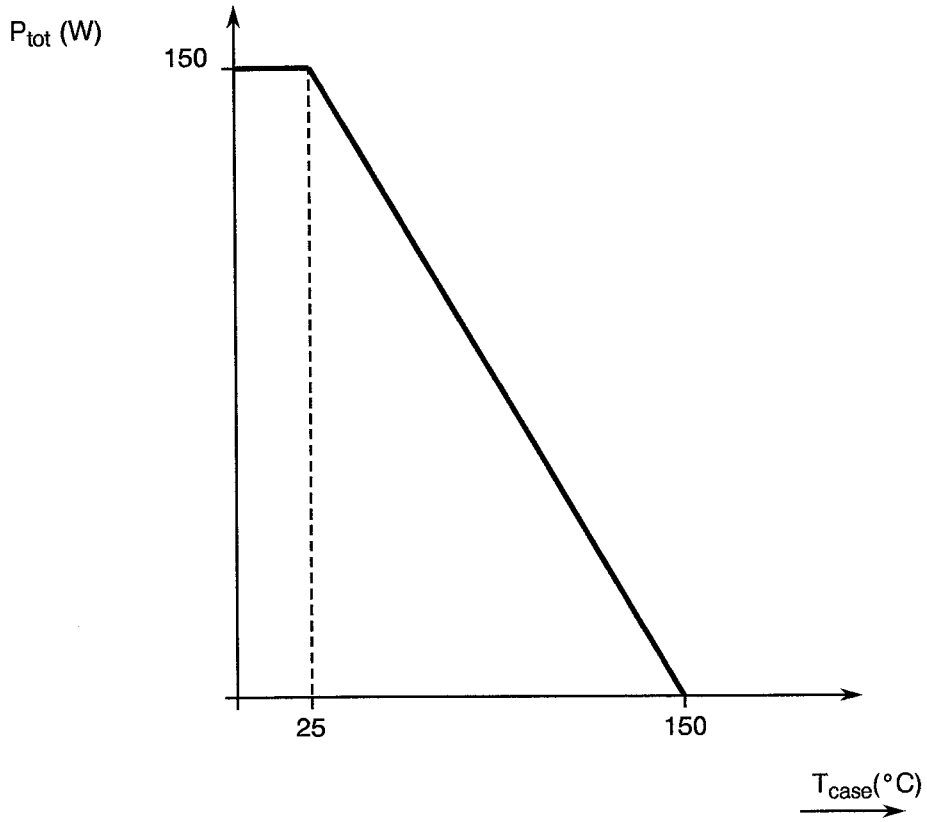
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS (Note 1)	UNIT	NOTES
1	Drain-Source Voltage	V_{DS}	Column 3	V	
2	Drain-GateVoltage	V_{DGR}	Column 4	V	2
3	Gate-Source Voltage	V_{GS}	±20	V	
4	Drain Current (Continuous)	I_D	Column 5	A	3
5	Inductive Current (Clamped)	I_{LM}	Column 6	A	4
6	Total Power Dissipation	P_{tot}	150	W	5
7	Operating Temperature Range	T_{op}	−55 to +150	°C	T_{case}
8	Storage Temperature Range	T_{stg}	−55 to +150	°C	
9	Soldering Temperature	T_{sol}	+260	°C	6

NOTES

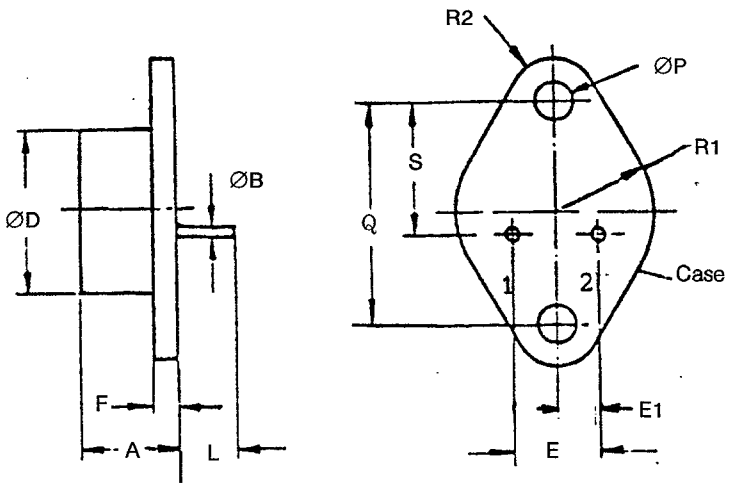
1. All columns refer to Table 1(a).
2. $R_{GS} = 1.0M\Omega$.
3. For $T_{case} \leq +94°C$.
4. $L = 100\mu H$.
5. For $T_{case} \leq +25°C$. For derating with temperature, see Figure 1.
6. Duration: 10 seconds maximum at a distance of not less than 1.5mm from the case, and the same lead shall not be resoldered until three minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION



Rated Power Dissipation versus Case Temperature

FIGURE 2 - PHYSICAL DIMENSIONS



SYMBOL	MILLIMETRES		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	6.86	10.67	0.270	0.420
ØB	See Note 1		See Note 1	
ØD	-	22.23	-	0.875
E	10.67	11.18	0.420	0.440
E1	5.21	5.72	0.205	0.225
F	1.52	3.43	0.060	0.135
L	7.92	12.70	0.312	0.500
ØP	3.84	4.09	0.151	0.161
Q	29.90	30.40	1.177	1.197
R1	12.57	13.34	0.495	0.525
R2	3.33	4.78	0.131	0.188
S	16.64	17.15	0.655	0.675

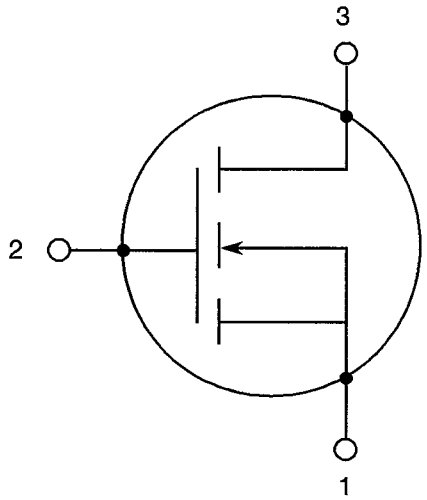
NOTES

1. Pin diameters are as follows:-

   Type Variants 01 and 02: 0.063" (1.60mm) / 0.057" (1.45mm)

   Type Variant 03: 0.043" (1.09mm) / 0.038" (0.97mm)

FIGURE 3 - FUNCTIONAL DIAGRAM



1. Source.
2. Gate.
3. Drain.

NOTES

1. The drain is internally connected to the case.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

(c) ESA/SCC Basic Specification No. 23500, Requirements for Lead Materials and Finishes for Components for Space Application.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein are stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

The following deviations from ESA/SCC Generic Specification No. 5000 shall apply:-

4.2.1 Deviations from Special In-process Controls

(a) For testing levels 'B' and 'C', a Scanning Electron Microscope (SEM) inspection shall be performed on samples from each metallisation lot in accordance with ESA/SCC Basic Specification No. 21400.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Burn-in Test: The duration shall be 240 hours.

(b) The following test shall be added to the Electrical Measurements at Room Temperature; to be performed after the burn-in test only:-

Verification of Safe Operating Area

Test 'A' Conditions

T_{case} = +25 ± 10 °C; duration = 1.0sec.

Type Variant 01: V_{DS} = 80Vdc; I_D = 1.87Adc
Type Variant 02: V_{DS} = 160Vdc; I_D = 0.94Adc
Type Variant 03: V_{DS} = 200Vdc; I_D = 0.75Adc

Test 'B' Conditions

T_{case} = +25 ± 10 °C; duration = 1.0sec.

Type Variant 01: V_{DS} = 3.95Vdc; I_D = 38Adc
Type Variant 02: V_{DS} = 5.0Vdc; I_D = 30Adc
Type Variant 03: V_{DS} = 10.7Vdc; I_D = 14Adc

Test Method for Both Tests

Using a 1.0 second pulse width with a minimum of 1 minute between pulses, increase V_{GS} and the Drain Supply Voltage until the specified value of I_D and V_{DS} are obtained. A load resistor, R_L, shall be used and shall be selected such that $I_D R_L$ = ≈ 10Vdc.

Electrical Measurements

After performing both tests, the electrical measurements Nos. 1 to 5 inclusive of Table 2 shall be repeated.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 18 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition : 'A' (Tension).
Applied Force : 10 Newtons.
Duration : 10 seconds.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be metal, hermetically sealed, similar to JEDEC TO-3.

4.4.2 Lead Material and Finish

Type variants 01 and 02 shall have leads of Type 'H' or Type 'I'. Type variant 03 shall have leads of Type 'F'. The lead finish for all variants shall be Type '4' in accordance with the requirements of ESA/SCC Basic Specification N. 23500.

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

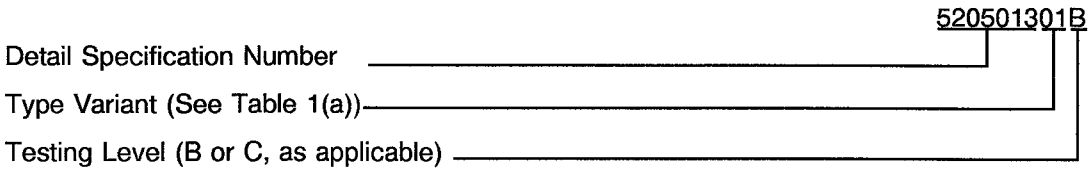
(c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for HTRB and Burn-in

The requirements for HTRB and Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for HTRB and Power Burn-in shall be as specified in Tables 5(a) and (b).

4.7.3 Electrical Circuits for HTRB and Burn-in

Circuits for use in performing the HTRB and Burn-in tests are shown in Figures 5(a) and (b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Drain-Source Breakdown Voltage	BV_{DSS}	3407 Bias Cond. 'C'	V_{GS} = 0V I_D = 1.0mA	Col. 7 of Table 1(a)	-	V
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	V_{DS} = V_{GS} I_D = 1.0mA	2.5	4.5	V
3	Gate-Source Leakage Current	I_{GSS}	3411 Bias Cond. 'C'	V_{GS} = 20V	-	100	nA
4	Off-State Drain Current	I_{DSS}	3415	V_{DS} = Col. 3 of Table 1(a) V_{GS} = 0V	-	1.0	mA
5	Static Drain-Source ON-State Resistance	$R_{DS(ON)}$	3421 Bias Cond. 'A'	V_{GS} = 10V I_D = Col. 9 of Table 1(a) Note 1	-	Col. 8 of Table 1(a)	Ω
6	Forward Transconductance	g_{fs}	See Fig. 4(a)	V_{DS} = 15V I_D = Col. 11 of Table 1(a) Note 1	Col. 10 of Table 1(a)	-	S

NOTES

1. Pulse Measurement: Pulse length = 300μs, Duty Cycle ≤ 2.0%.
2. Measurements to be performed on a sample basis, LTPD = 7.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS (NOTE 2)	LIMITS		UNIT
					MIN	MAX	
7	Input Capacitance	C_{iss}	3431	$V_{GS} = 0$; $V_{DS} = 25V$ $f = 1.0MHz$	-	4000	pF
8	Output Capacitance	C_{oss}	-	$V_{GS} = 0$; $V_{DS} = 25V$ $f = 1.0MHz$ Type Variant 01 Type Variant 02 Type Variant 03	 - - -	 1500 1200 800	pF
9	Rise Time	t_r	See Fig. 4(b)	Type Variant 01: $I_D = 24A$; $V_{DD} \simeq 24V$ Type Variant 02: $I_D = 19A$; $V_{DD} \simeq 95V$ Type Variant 03: $I_D = 9.0A$; $V_{DD} \simeq 180V$	 - - -	 100 10 65	ns
10	Fall Time	t_f	See Fig. 4(b)	Type Variant 01: $I_D = 24A$; $V_{DD} \simeq 24V$ Type Variant 02: $I_D = 19A$; $V_{DD} \simeq 95V$ Type Variant 03: $I_D = 9.0A$; $V_{DD} \simeq 180V$	 - - -	 100 100 75	ns
11	Turn-on Delay Time	$t_{d(ON)}$	See Fig. 4(b)	Type Variant 01: $I_D = 24A$; $V_{DD} \simeq 24V$ Type Variant 02: $I_D = 19A$; $V_{DD} \simeq 95V$ Type Variant 03: $I_D = 9.0A$; $V_{DD} \simeq 180V$	 - - -	 35 35 35	ns
12	Turn-off Delay Time	$t_{d(OFF)}$	See Fig. 4(b)	Type Variant 01: $I_D = 24A$; $V_{DD} \simeq 24V$ Type Variant 02: $I_D = 19A$; $V_{DD} \simeq 95V$ Type Variant 03: $I_D = 9.0A$; $V_{DD} \simeq 180V$	 - - -	 125 125 150	ns

NOTES: See Page 15.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (Cont'd)

No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS (NOTE 2)	LIMITS		UNIT
					MIN	MAX	
13	Common Source Reverse Transfer Capacitance	C_{RSS}	-	$V_{GS} = 0$; $V_{DS} = 25V$ $f = 1.0MHz$ Type Variant 01 Type Variant 02 Type Variant 03	 200 150 50	 500 500 350	pF

NOTES: See Page 15.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

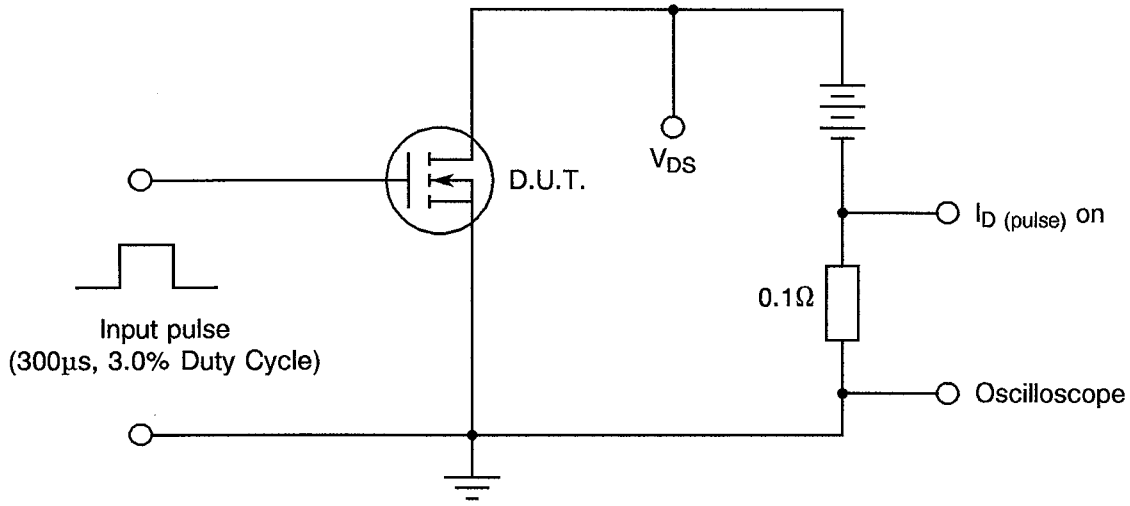
No.	CHARACTERISTICS	SYMBOL	MIL-STD 750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} = V_{GS}$ $I_D = 1.0mA$ $T_{amb} = +125\ (+0\text{-}5)°C$ $T_{amb} = -55\ (+5\text{-}0)\ °C$	 1.0 -	 - 5.0	V
3	Gate-Source Leakage Current	I_{GSS}	3411 Bias Cond. 'D'	$V_{GS} = 10V$ $T_{amb} = -55\ (+5\text{-}0)\ °C$	-	100	nA
4	Off-State Drain Current	I_{DSS}	3415	V_{DS} = Col. 3 of Table 1(a) $V_{GS} = 0V$ $T_{amb} = +125\ (+0\text{-}5)°C$	-	4.0	mA
5	Static Drain-Source ON-State Resistance	$R_{DS(ON)}$	3421 Bias Cond. 'A'	$V_{GS} = 10V$ I_D = Col. 9 of Table 1(a) $T_{amb} = +125\ (+0\text{-}5)°C$ See Note 1	-	Col. 12 of Table 1(a)	Ω

NOTES

1. Pulse Measurement: Pulse length = 300μs, Duty Cycle ≤ 2.0%.

FIGURE 4 - CIRCUIT FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - FORWARD TRANSCONDUCTANCE



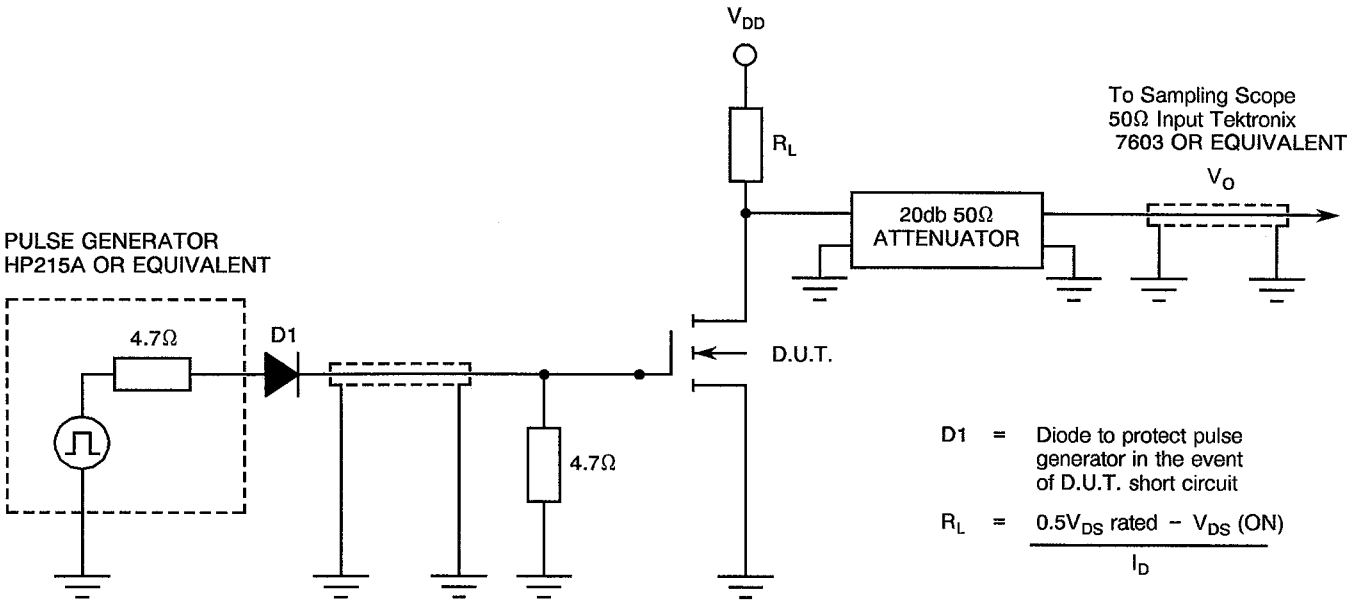
TEST METHOD

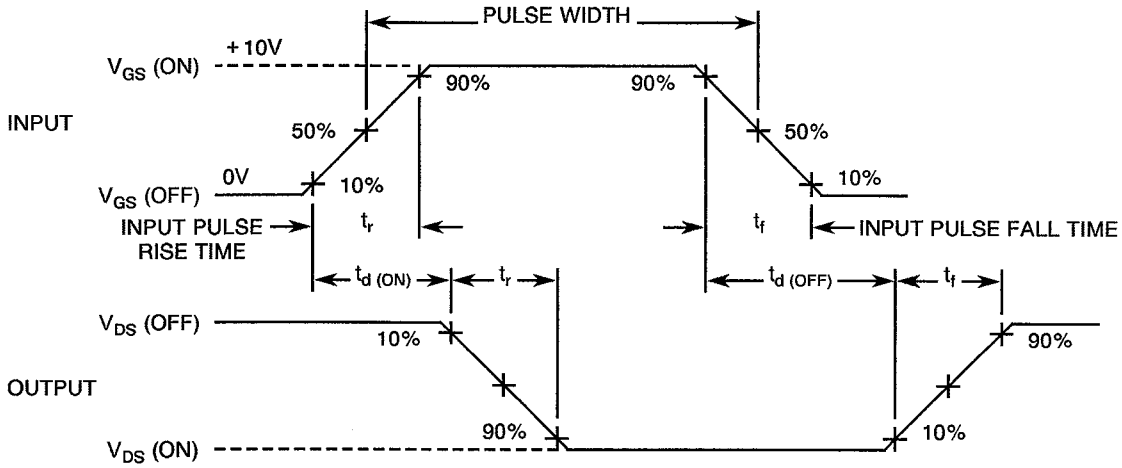
1. V_{DS} and I_D as required for transistor under test (see Table 2).
2. Two measurements are taken at drain current of $I_D + 10\%$ and $I_D - 10\%$, both at the specified V_{DS}.
3. Apply a negative going voltage pulse between gate and source of duration of 300µs and duty cycle ≤3.0%.
4. Adjust the pulse amplitude until the pulsed drain current reaches the $I_D - 10\%$ point. Note the pulse amplitude – $V_{GS(1)}$.
5. Raise the pulse amplitude until the drain current reaches the $I_D + 10\%$ point. Note the pulse amplitude – $V_{GS(2)}$.
6. Forward transconductance is calculated as follows:-

$$g_{21s} = \frac{I_D \times 0.2}{V_{GS(2)} - V_{GS(1)}}$$

FIGURE 4 - CIRCUIT FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - SWITCHING TIMES





NOTES

1. When measuring rise time, V_{GS} (ON) shall be as specified on the input waveform.

   When measuring fall time, V_{GS} (OFF) shall be as specified on the input waveform.

   The input transition and drain voltage response detector shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement. The current shall be sufficiently small so that doubling it does not affect test results greater than the precision of measurement.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	±20	%
3	Gate-Source Leakage Current	I_{GSS}	As per Table 2	As per Table 2	±20 or (1) ±100	nA %
4	Zero Gate Voltage Drain Current	I_{DSS}	As per Table 2	As per Table 2	±20 or (1) ±100	µA %
5	Static Drain-Source ON-State Resistance	$R_{DS(ON)}$	As per Table 2	As per Table 2	±20	%

NOTES

1. Whichever is greater.

TABLE 5(a) - CONDITIONS FOR HTRB (PRE-CONDITIONING STRESS)

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+150(+0-5)	°C
2	Drain-Source Voltage	V_{DS}	Type Variant 01 80 Type Variant 02 160 Type Variant 03 320	V
3	Gate-Source Voltage	V_{GS}	0	V
4	Duration	-	48	Hrs

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS

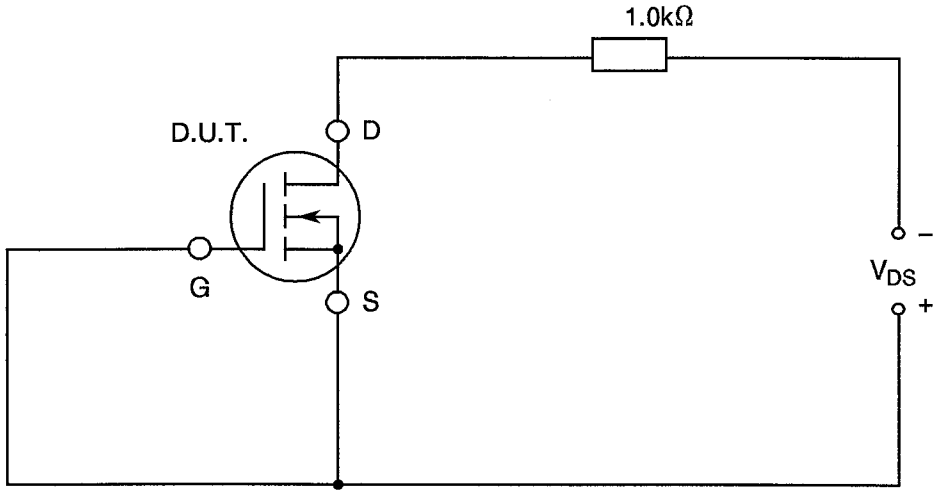
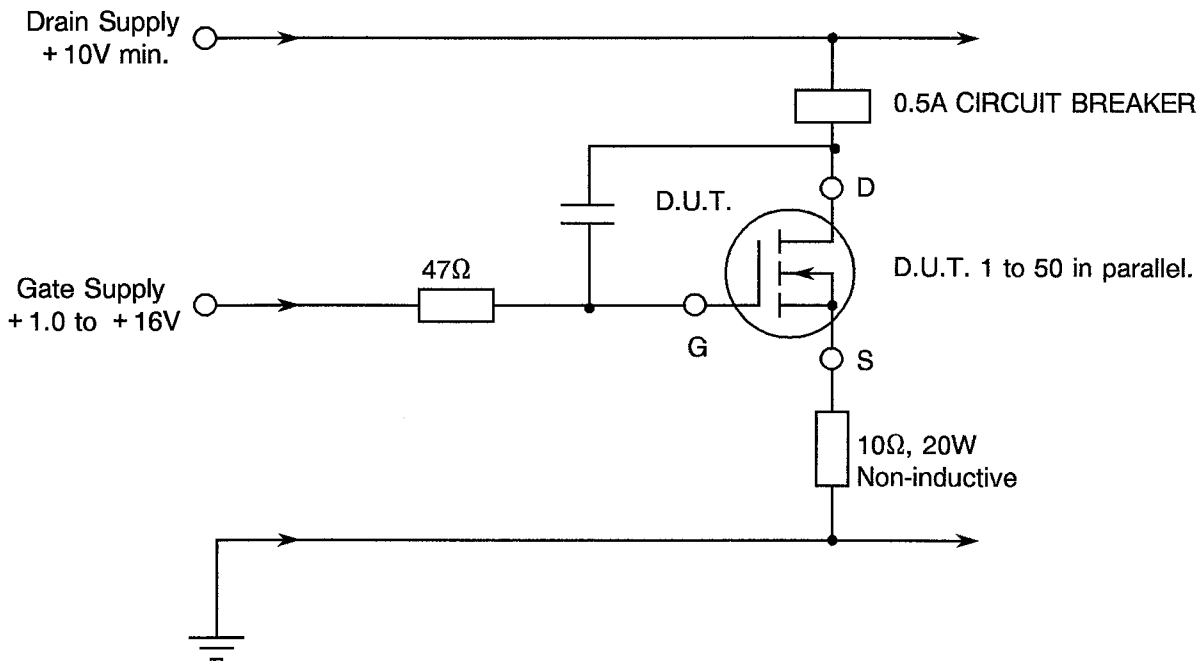


TABLE 5(b) - CONDITIONS FOR BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Case Temperature	T_{case}	+140 ± 10	°C
2	Drain-Source Voltage	V_{DS}	≥10	V
3	Gate-Source Voltage	V_{GS}	1.0 to 16	V
4	Duration	-	240	Hrs

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 6.

4.8.3 Conditions for Steady State Operation Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be the same as specified in Table 5(b) for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be the same as shown in Figure 5(b) for the burn-in test.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	2.5	4.5	V
3	Gate-Source Leakage Current	I_{GSS}	As per Table 2	As per Table 2	-	100	nA
4	OFF-State Drain Current	I_{DSS}	As per Table 2	As per Table 2	-	1.0	mA
5	Static Drain-Source ON-State Resistance	$R_{DS(ON)}$	As per Table 2	As per Table 2	- - -	0.06 0.14 0.3	Ω