QUADRUPLE PNP SILICON TRANSISTOR ARRAY

BASED ON TYPE MQ3467

ESCC Detail Specification No. 5207/006

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space components
coordination group

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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all modifications defined in Revisions 'A', 'B' and 'C' to Issue 1 and the changes agreed in the following DCRs:-		
		Cover page		None
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		Para. 1.7	: Text amended	21083

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FIGURES

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Quadruple PNP Silicon Transistor Array, based on Type MQ3467. It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic transistors specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the transistors specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification of the transistors specified herein, is shown in Figure 3.

1.7 HIGH TEMPERATURE TEST PRECAUTIONS

For tin-lead plated or solder-dipped lead-finish, all tests to be performed at a temperature that exceeds + 125°C shall be carried out in a 100% inert atmosphere.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductors.

(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	FLAT	2(a)	D2
02	FLAT	2(a)	D3 or D4
03	D.I.L.	2(b)	D2
04	D.I.L.	2(b)	D3 or D4

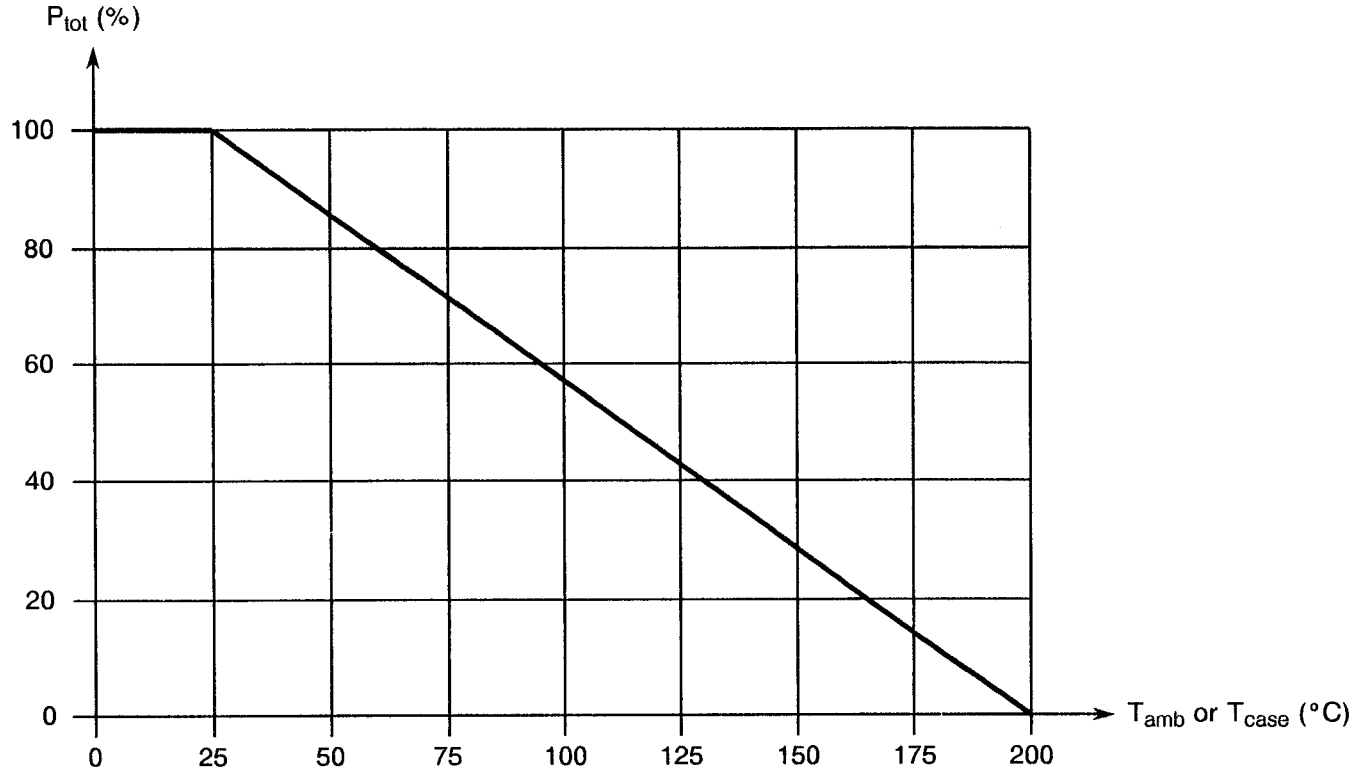
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Collector-Base Breakdown Voltage	V_{CB}	40	V	
2	Collector-Emitter Breakdown Voltage	V_{CE}	40	V	
3	Emitter-Base Breakdown Voltage	V_{EB}	5.0	V	
4	Collector Current	I_C	1.0	A	
5	Power Dissipation T_{amb} = +25°C	P_{tot}	0.4 (Note 1) 0.5 (Note 2)	W	Note 3
6	Power Dissipation T_{case} = +25°C	P_{tot}	1.25 (Note 1) 5.0 (Note 2)	W	Note 4
7	Operating Temperature Range	T_{op}	−55 to +200	°C	T_{amb}
8	Storage Temperature Range	T_{stg}	−65 to +200	°C	
9	Soldering Temperature	T_{sol}	+260	°C	Note 5

NOTES

1. One transistor.
2. Four transistors.
3. For T_{amb} > +25°C derate at 2.8mW/°C up to +200°C.
4. For T_{case} > +25°C derate at 28mW/°C up to +200°C.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

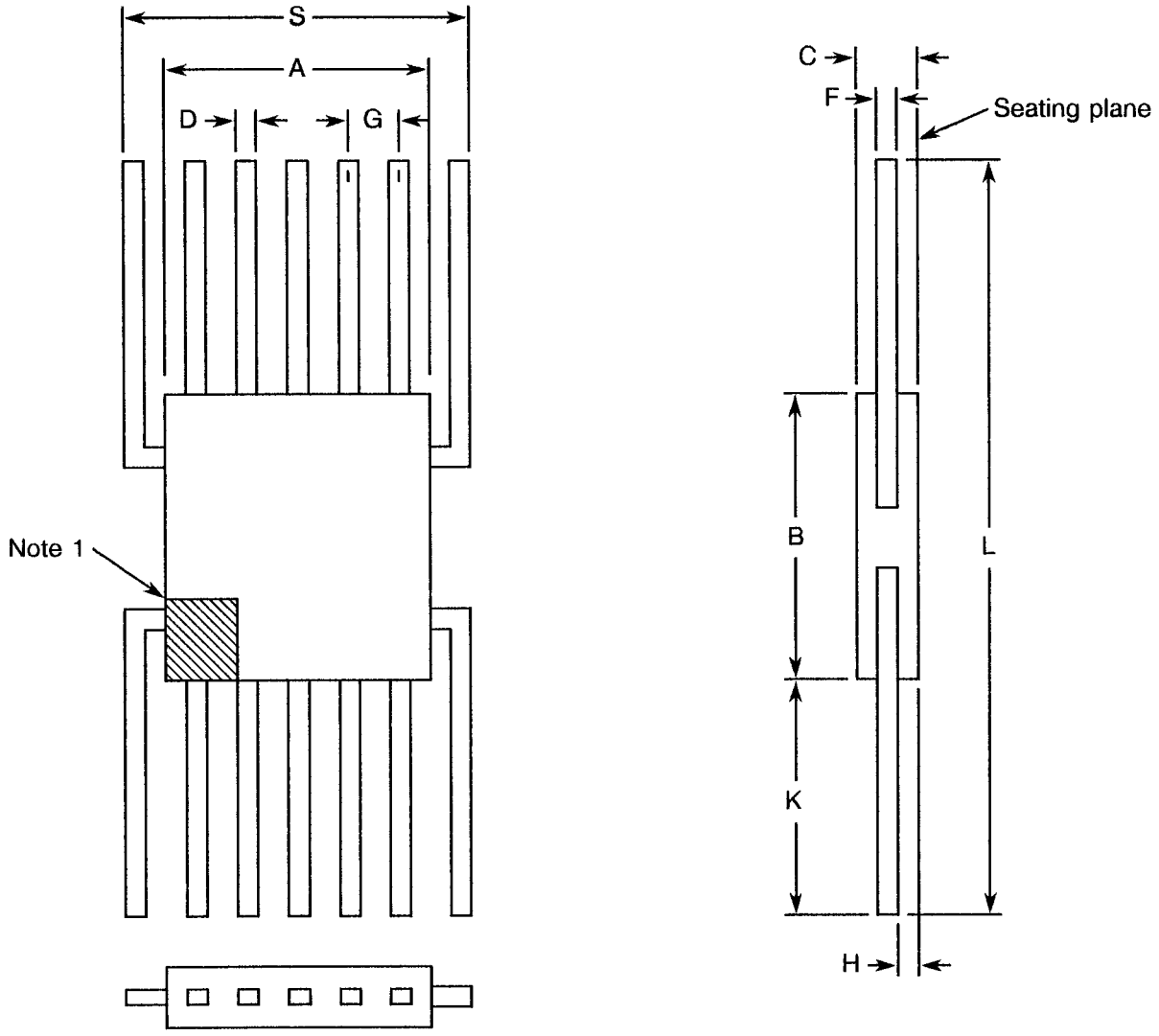
FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 14-PIN

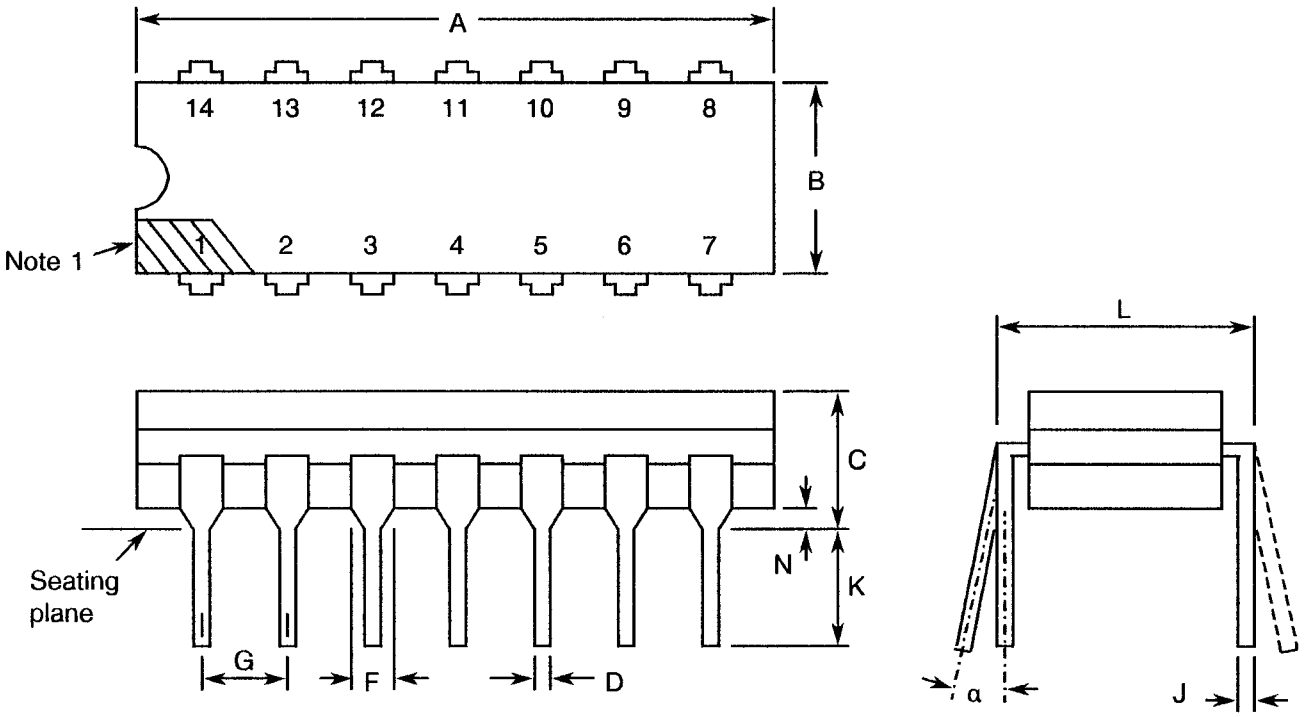


SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	6.1	7.0	-
B	6.1	6.6	2
C	0.76	0.79	-
D	0.3	0.5	4
F	0.08	0.15	4
G	1.1	1.4	3, 5
H	-	0.8	-
K	6.1	-	-
L	18.8	-	-

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 14-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	19.05	19.94	8
B	6.23	7.11	8
C	3.94	5.08	-
D	0.39	0.58	4
F	1.40	1.66	4
G	2.54 BSC		5, 9
J	0.21	0.38	4
K	3.18	4.31	6
L	7.62 BSC		7
α	0°	15°	10
N	0.51	1.01	-

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) AND 2(b)

1. Index area: a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. This dimension allows for off-centre lids, meniscus and glass overrun.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ± 0.13mm of its true longitudinal position relative to Pins 1 and 14.
4. All leads.
5. 12 spaces.
6. Leads within 0.13mm radius of true position at seating plane at maximum material condition.
7. Dimension L to centre of leads when formed parallel.
8. Dimension A and B do not include glass run-out.
9. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25mm of its true longitudinal position relative to Pins 1 and 14, at the seating plane maximum position.
10. Lead centre when α is 0°.

FIGURE 3 - FUNCTIONAL DIAGRAM AND PIN ASSIGNMENT

FIGURE 3(a) - FLAT PACKAGE

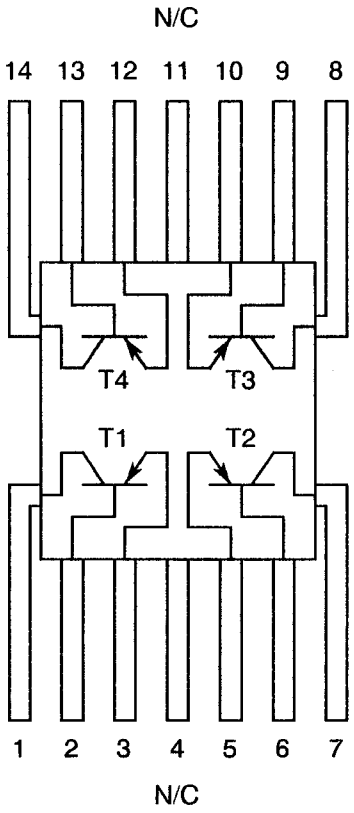
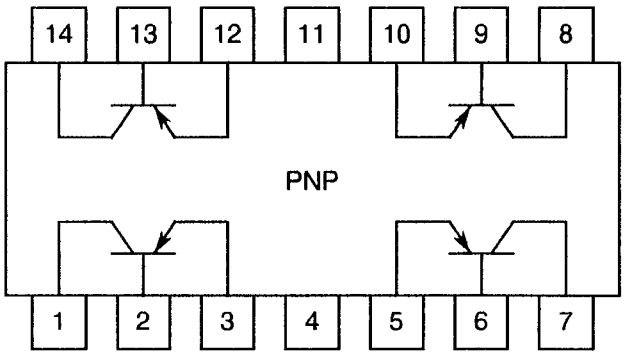


FIGURE 3(b) - DUAL-IN-LINE PACKAGE



4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductors. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

None.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) The electrical measurements specified at the end of Subgroup I and II tests shall be carried out as stated in Table 6 of this specification.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) The electrical measurements referenced 9.9.3 shall be performed as stated in Table 6 of this specification.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 2.0 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body with hard glass seals, and the lid shall be welded, brazed or preform soldered.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' or Type '3 or 4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

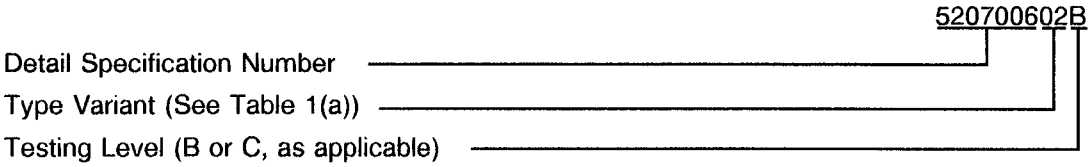
(c) Traceability Information.

4.5.2 Lead Identification

Pin 1 shall be marked with a black dot located within the shaded area shown in Figure 2.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +150$°C and -55°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 are shown, where applicable, in MIL-STD-750 and Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. and Burn-in

The requirements for H.T.R.B. and burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for H.T.R.B. and burn-in shall be as specified in Tables 5(a) and 5(b) of this specification.

4.7.3 Electrical Circuits for Burn-in (Figure 5)

Not applicable.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN.	MAX.	
1 to 4	Collector-Base Breakdown Voltage	BV_{CBO}	3001	$I_C = 10\mu A$ $I_E = 0A$ (Pins 1-2-6-7-8-9-13-14)	−40	-	V
5 to 8	Collector-Emitter Breakdown Voltage	BV_{CEO}	3011	$I_C = 10mA$ $I_B = 0A$ Note 1 (Pins 1-3-5-7-8-10-12-14)	−40	-	V
9 to 12	Emitter-Base Breakdown Voltage	BV_{EBO}	3026	$I_E = 10\mu A$ $I_C = 0A$ (Pins 2-3-5-6-9-10-12-13)	−5.0	-	V
13 to 16	Collector Cut-off Current	I_{CBO}	3036	$V_{CB} = 30V$ $I_E = 0A$ (Pins 1-2-6-7-8-9-13-14)	-	100	nA
17 to 20	Collector Saturation Voltage	$V_{CE(SAT)}$	3071	$I_C = 500mA$ $I_B = 50mA$ Note 1 (Pins 1-3-5-7-8-10-12-14)	-	0.5	V
21 to 24	Base Saturation Voltage	$V_{BE(SAT)}$	3066	$I_C = 500mA$ $I_B = 50mA$ Note 1 (Pins 2-3-5-6-9-10-12-13)	-	1.2	V
25 to 28	D.C. Forward Current Transfer Ratio	h_{FE}	3076	$I_C = 500mA$ $V_{CE} = 1.0V$ Note 1 (Pins 1 to 14)	20	-	-

NOTES

1. Pulse measurements: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
2. Test performed on a sample basis Inspection Level II, Table IIA, AQL = 1.0, of MIL-STD-105.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN.	MAX.	
29 to 32	Output Capacitance	C_{obo}	3236		V_{CB} = 10V I_E = 0A Variants 01, 02 f = 100kHz Variants 03, 04 f = 1.0MHz (Pins 1-2-3, 5-6-7, 8-9-10, 12-13-14) Note 2	 - -	 20 25	pF
33 to 36	Input Capacitance	C_{ibo}	3240		V_{EB} = 0.5V I_C = 0A Variants 01, 02 f = 100kHz Variants 03, 04 f = 1.0MHz (Pins 1-2-3, 5-6-7, 8-9-10, 12-13-14) Note 2	 - -	 80 80	pF
37 to 44	Switching Time	t_{on} t_{off}	-	4	I_C = 500mA I_B = 50mA (Pins 1-2-3, 5-6-7, 8-9-10, 12-13-14) Note 2	- -	40 110	ns
45 to 48	Current Gain Bandwidth Product	f_T	3261	-	I_C = 50mA V_{CE} = 10V f = 100MHz (Pins 1-2-3, 5-6-7, 8-9-10, 12-13-14) Note 2	150	-	MHz

NOTES: See Page 15.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +150°C, −55°C

No.	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN.	MAX.	
13 to 16	Collector-Base Cut-off Current	I_{CBO}	3036	V_{CB} = 30V I_E = 0A T_{amb} = +150°C (Pins 1-2, 6-7, 8-9, 13-14)	-	10	µA
25 to 28	D.C. Forward Current Transfer Ratio	h_{FE}	3076	I_C = 500mA V_{CE} = 1.0V T_{amb} = −55°C (Pins 1-2-3, 5-6-7, 8-9-10, 12-13-14) Note 1	15	-	-

NOTES: See Page 15.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - SWITCHING TIME

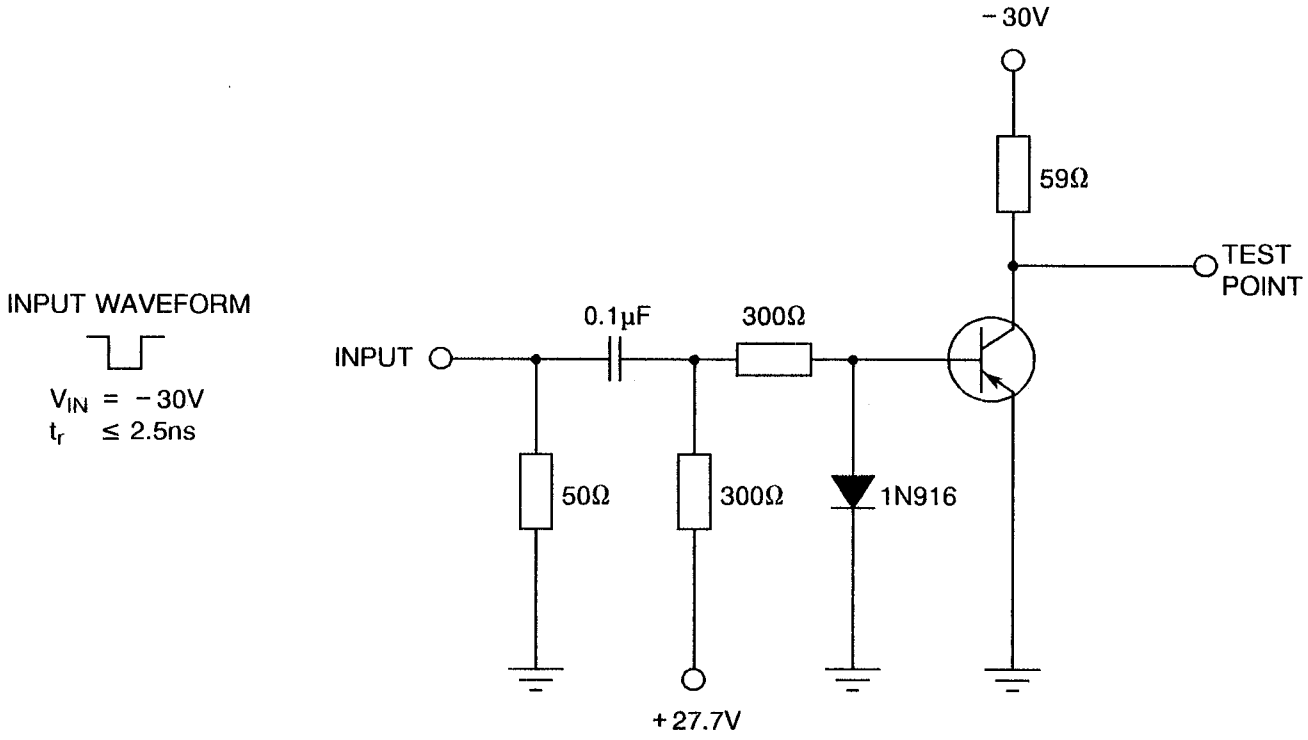


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
13 to 16	Collector-Base Cut-off Current	I_{CBO}	As per Table 2	As per Table 2	±100	%
17 to 20	Collector Saturation Voltage	$V_{CE(SAT)}$	As per Table 2	As per Table 2	±50	mV
25 to 28	D.C. Forward Current Transfer Ratio	h_{FE}	As per Table 2	As per Table 2	±20	%

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+150	°C
2	Collector-Base Voltage	V_{CB}	32	V
3	Test Method 1039 of MIL-STD-750	-	A	-
4	Duration	-	48	Hrs

TABLE 5(b) - CONDITIONS FOR BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+25±3	°C
2	Power Dissipation	P_{tot}	125 (Note 1)	mW
3	Collector-Base Voltage	V_{CB}	20 (Note 1)	V
4	Test Method 1039 of MIL-STD-750	-	B	-

NOTES

1. Each transistor.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are scheduled in Table 6.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance tests are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests (Figure 5)

Not applicable.

4.8.6 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The conditions for high temperature storage shall be $T_{amb} = +200(+0-5)$°C.

TABLE 6 - ELECTRICAL MEASUREMENTS AFTER ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS DURING ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
13 to 16	Collector-to-Base Cut-off Current	I_{CBO}	As per Table 2	As per Table 2	-	100	nA
17 to 20	Collector Saturation Voltage	$V_{CE(SAT)}$	As per Table 2	As per Table 2	-	0.5	V
25 to 28	D.C. Forward Current Transfer Ratio	h_{FE}	As per Table 2	As per Table 2	-	Min. 20	%