



**TRANSISTORS, QUADRUPLE,
NPN SILICON ARRAY,
BASED ON TYPE S502T
ESCC Detail Specification No. 5207/020**

**ISSUE 1
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NPN SILICON ARRAY,

BASED ON TYPE S502T

ESA/SCC Detail Specification No. 5207/020



**space components
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**SCC**ESA/SCC Detail Specification
No. 5207/020

Rev. 'B'

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DOCUMENTATION CHANGE NOTICE

| Rev. Letter | Rev. Date | Reference | CHANGE Item | Approved DCR No. |
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| 'A' | Feb. '92 | P1. Cover page P2. DCN P5. Para. 1.2 P10. Para. 2 Para. 4.2.2 P11. Para. 4.2.4 P18. Table 3 | : Paragraph amended : "ESA/SCC Basic Spec. No. 23500" added : Bond Strength and Die Shear Test deviations deleted : PIND deviation deleted : Bond Strength and Die Shear Test deviations deleted : Note 2 deleted | None None 21021 21025 23499 21043 23499 21047 |
| | | This document has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist. | | |
| 'B' | Aug. '96 | P1. Cover page P2. DCN P5. Para. 1.7 | : Text amended | None None 21083 |

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APPENDICES (Applicable to specific Manufacturers only)

None.

**1. GENERAL****1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Transistor, Quadruple, NPN Silicon Array, based on Type S502T.

It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

See Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistor array specified herein are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the transistor array specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the transistor array specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram showing lead identification, of the transistor array specified herein, is shown in Figure 3.

1.7 HIGH TEMPERATURE TEST PRECAUTIONS

For tin-lead plated or solder-dipped lead finish, all tests to be performed at a temperature that exceeds +125°C shall be carried out in a 100% inert atmosphere.

**TABLE 1(a) - TYPE VARIANTS**

| VARIANT | BASED ON TYPE | CASE | FIGURE | LEAD MATERIAL AND FINISH |
|---------|---------------|-----------|--------|--------------------------|
| 01 | S502T | Flat Pack | 2 | D2 |
| 02 | S502T | Flat Pack | 2 | D3 or D4 |

TABLE 1(b) - MAXIMUM RATINGS

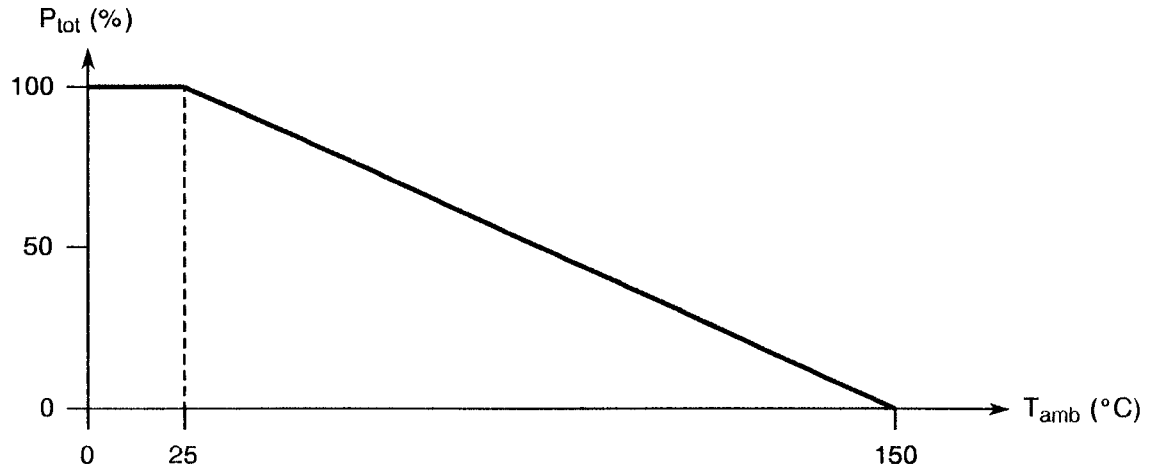
| No. | CHARACTERISTICS | SYMBOL | MAXIMUM RATINGS | UNIT | REMARKS |
|-----|--------------------------------|-----------|------------------------------|------------------|---|
| 1 | Collector-Base Voltage | V_{CBO} | 75 | V | |
| 2 | Collector-Emitter Voltage | V_{CEO} | 40 | V | |
| 3 | Emitter-Base Voltage | V_{EBO} | 6.0 | V | |
| 4 | Collector Current (Continuous) | I_C | 500 | mA | |
| 5 | Power Dissipation | P_{tot} | 0.3 (Note 1) 0.5 (Note 2) | W | $T_{amb} \leq +25^\circ\text{C}$ (see Figure 1 for derating) |
| 6 | Operating Temperature Range | T_{op} | - 65 to + 150 | $^\circ\text{C}$ | T_{amb} |
| 7 | Storage Temperature Range | T_{stg} | - 65 to + 150 | $^\circ\text{C}$ | |
| 8 | Soldering Temperature | T_{sol} | + 260 | $^\circ\text{C}$ | Time: $\leq 10\text{s}$ Distance from case $\geq 1.5\text{mm}$ |

NOTES

1. One Transistor.
2. Four Transistors.



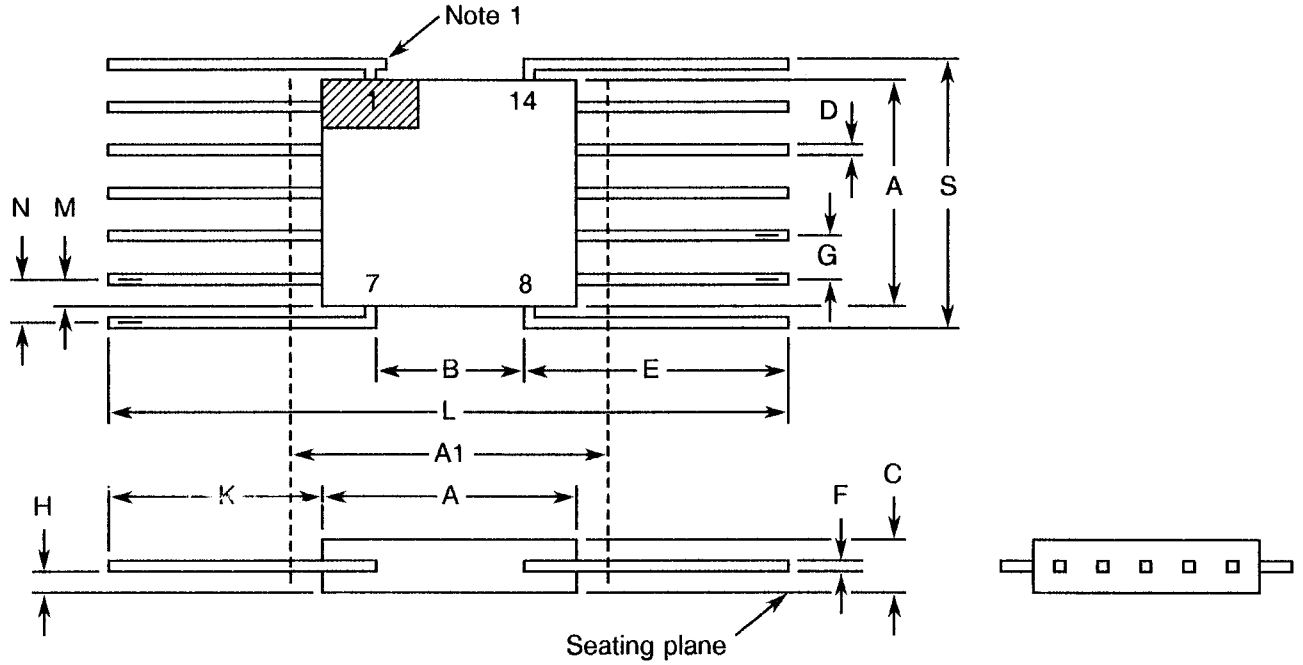
FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature



FIGURE 2 - PHYSICAL DIMENSIONS



| SYMBOL | MILLIMETRES | | INCHES | | NOTES |
|--------|-------------|------|------------|-------|-------|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 6.10 | 7.00 | 0.240 | 0.275 | |
| A1 | - | 7.24 | - | 0.285 | 4 |
| B | 1.22 | 1.32 | 0.048 | 0.052 | |
| C | 0.76 | 2.00 | 0.030 | 0.079 | |
| D | 0.25 | 0.50 | 0.010 | 0.020 | 7 |
| E | 8.79 | - | 0.346 | - | 6 |
| F | 0.08 | 0.15 | 0.003 | 0.006 | 7 |
| G | 1.27 TYP. | | 0.050 TYP. | | 3, 9 |
| H | 0.37 | 0.80 | 0.015 | 0.032 | 2 |
| K | 6.10 | - | 0.240 | - | 8 |
| L | 18.80 | - | 0.740 | - | |
| M | 1.77 | 1.85 | 0.070 | 0.073 | 5 |
| N | 1.27 TYP. | | 0.050 TYP. | | 5 |
| S | - | 7.63 | - | 0.300 | |

NOTES: See Page 9.

**2. APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductor Components.
- (b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.
- (c) ESA/SCC Basic Specification No. 23500, Requirements for Lead Materials and Finishes for Components for Space Application.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

4. REQUIREMENTS**4.1 GENERAL**

The complete requirements for procurement of the transistor array specified herein are stated in this specification and ESA/SCC Generic Specification No. 5000. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION**4.2.1 Deviations from Special In-process Controls**

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.



4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 9.22, "H.T.R.B. Test": Shall not be performed

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) The electrical measurements referenced 9.9.3, shall be performed in accordance with Table 6 of this specification.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistor array specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistor array specified herein shall be 0.4 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition: 'E', Lead Fatigue.

Applied Force: 2.5 ± 0.1 Newtons, 3 bends at 45°.



4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistor array specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal or ceramic body with hard glass seals and the lid shall be welded, brazed, preform soldered or glass frit sealed.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with either Type '2' or Type '3 or 4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

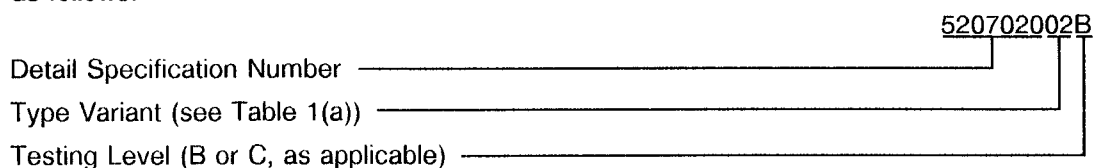
- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:-





4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = -55(+5-0)$ and $+150(+0-5)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Table 2 of this specification are shown in Figure 4.



4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5 of this specification.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS**

| No. | CHARACTERISTICS | SYMBOL | MIL-STD-750 TEST METHOD | TEST CONDITIONS | LIMITS | | UNIT |
|----------------|---|----------------|----------------------------|---|--------|-----|------|
| | | | | | MIN | MAX | |
| 1 to 4 | Collector-Emitter Breakdown Voltage | $V_{(BR)CEO}$ | 3011 | $I_C = 10\text{mA}$ $I_B = 0\text{A}$ Note 1 | 40 | - | V |
| 5 to 8 | Collector-Base Breakdown Voltage | $V_{(BR)CBO}$ | 3001 | $I_C = 10\mu\text{A}$ $I_E = 0\text{A}$ | 75 | - | V |
| 9 to 12 | Emitter-Base Breakdown Voltage | $V_{(BR)EBO}$ | 3026 | $I_E = 10\mu\text{A}$ $I_C = 0\text{A}$ | 6.0 | - | V |
| 13 to 16 | Collector-Base Cut-off Current | I_{CBO} | 3036 | $V_{CB} = 60\text{V}$ $I_E = 0\text{A}$ | - | 10 | nA |
| 17 to 20 | Emitter-Base Cut-off Current | I_{EBO} | 3061 | $V_{EB} = 3.0\text{V}$ $I_C = 0\text{A}$ | - | 10 | nA |
| 21 to 24 | D.C. Forward Current Transfer Ratio 1 | h_{FE1} | 3076 | $I_C = 10\text{mA}$ $V_{CE} = 10\text{V}$ Note 1 | 75 | - | - |
| 25 to 28 | D.C. Forward Current Transfer Ratio 2 | h_{FE2} | 3076 | $I_C = 150\text{mA}$ $V_{CE} = 10\text{V}$ Note 1 | 100 | 300 | - |
| 29 to 32 | D.C. Forward Current Transfer Ratio 3 | h_{FE3} | 3076 | $I_C = 500\text{mA}$ $V_{CE} = 10\text{V}$ Note 1 | 40 | - | - |
| 33 to 36 | Collector-Emitter Saturation Voltage 1 | $V_{CE(sat)1}$ | 3071 | $I_C = 150\text{mA}$ $I_B = 15\text{mA}$ Note 1 | - | 0.3 | V |
| 37 to 40 | Collector-Emitter Saturation Voltage 2 | $V_{CE(sat)2}$ | 3071 | $I_C = 500\text{mA}$ $I_B = 50\text{mA}$ Note 1 | - | 1.0 | V |
| 41 to 44 | Base-Emitter Saturation Voltage | $V_{BE(sat)}$ | 3066 | $I_C = 150\text{mA}$ $I_B = 15\text{mA}$ Note 1 | - | 1.2 | V |

NOTES: See Page 16.

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TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

| No. | CHARACTERISTICS | SYMBOL | MIL-STD-750 TEST METHOD | TEST FIG. | TEST CONDITIONS (NOTE 2) | LIMITS | | UNIT |
|----------------|--------------------|-----------|----------------------------|--------------|---|--------|-----|------|
| | | | | | | MIN | MAX | |
| 45 to 48 | Output Capacitance | C_{obo} | 3236 | - | $V_{CB} = 10V$ $I_E = 0A$ $100kHz < f < 1.0MHz$ | - | 8.0 | pF |
| 49 to 52 | Turn-on Time | t_{on} | - | 4(a) | $I_C = 150mA$ $I_B = 15mA$ $V_{CC} = 30V$ | - | 45 | ns |
| 53 to 56 | Turn-off Time | t_{off} | - | 4(b) | $I_C = 150mA$ $I_{B1} = I_{B2} = 15mA$ $V_{CC} = 30V$ | - | 310 | ns |
| 57 to 60 | Cut-off Frequency | f_t | 3301 | - | $I_C = 20mA$ $V_{CE} = 10V$ $f = 100MHz$ | 250 | - | MHz |

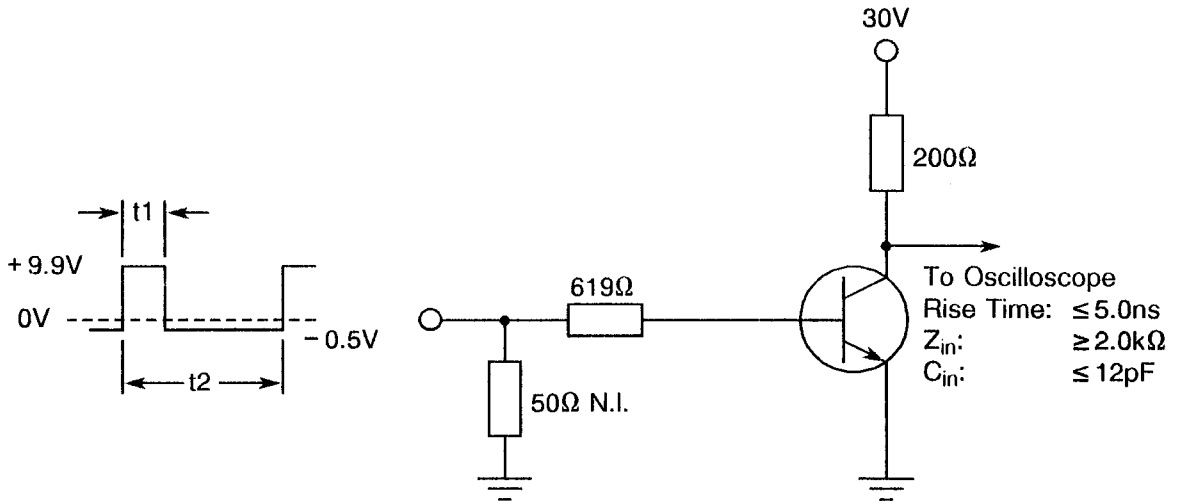
NOTES

1. Pulsed measurement: Pulse Width $\leq 500\mu s$, Duty Cycle $\leq 2.5\%$.
2. Measurements shall be performed on a sample basis, LTPD7 or less.



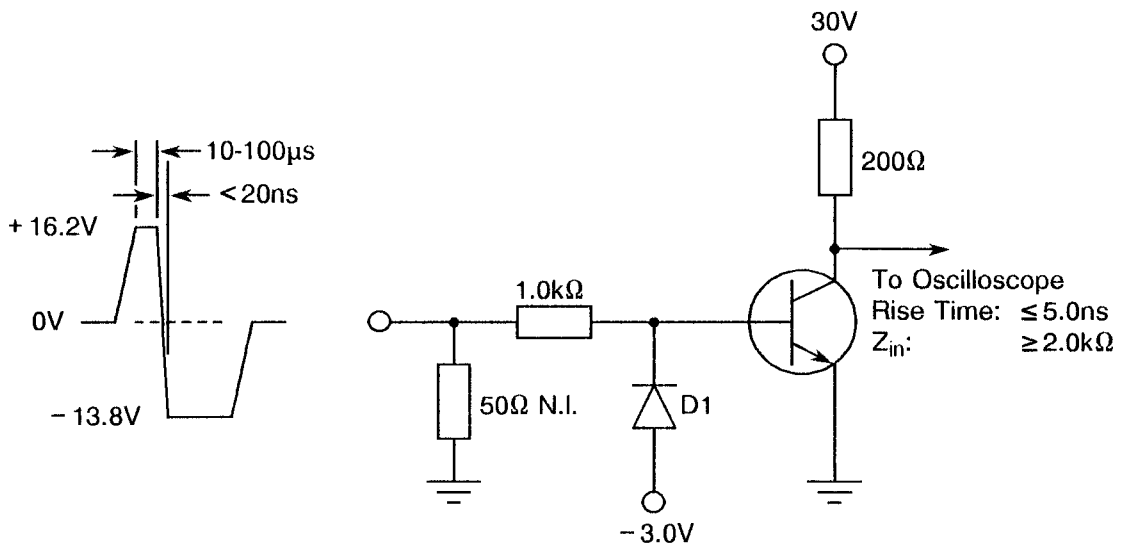
FIGURE 4 - TEST CIRCUIT

FIGURE 4(a) - TURN-ON TIME



Input:
 Rise time $\leq 2.0\text{ns}$
 Duty Cycle $\geq 2.0\% = \frac{t_1}{t_2}$
 $t_1 = 200 \pm 10\text{ns}$.

FIGURE 4(b) - TURN-OFF TIME



Duty Cycle $\leq 2.0\%$

NOTES

1. D1 similar to 1N4148, $t_{rr} \leq 8.0\text{ns}$ max.

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES**

| No. | CHARACTERISTICS | SYMBOL | MIL-STD-750 TEST METHOD | TEST CONDITIONS | LIMITS | | UNIT |
|----------------|--|-----------|----------------------------|--|--------|-----|---------|
| | | | | | MIN | MAX | |
| 13 to 16 | Collector-Base Cut-off Current | I_{CBO} | 3036 | $T_{amb} = +150^{\circ}C$ $V_{CB} = 60V$ $I_E = 0A$ | - | 10 | μA |
| 21 to 24 | D.C. Forward Current Transfer Ratio 1 | h_{FE1} | 3076 | $T_{amb} = -55^{\circ}C$ $I_C = 10mA, V_{CE} = 10V$ Note 1 | 35 | - | - |

NOTES

1. Pulsed measurement: Pulse Width $\leq 500\mu s$, Duty Cycle $\leq 2.5\%$.

TABLE 4 - PARAMETER DRIFT VALUES

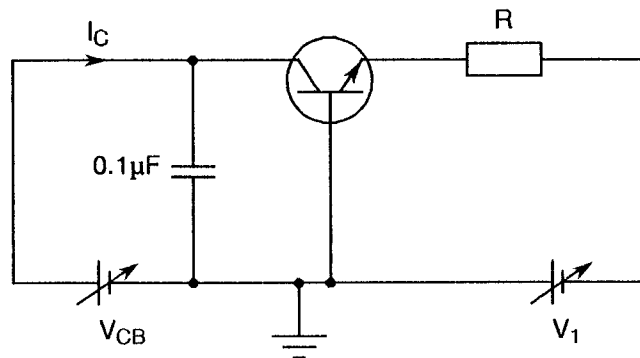
| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | CHANGE LIMITS (Δ) | UNIT |
|----------------|---|----------------|-----------------------------|--------------------|----------------------------------|---------|
| 13 to 16 | Collector-Base Cut-off Current | I_{CBO} | As per Table 2 | As per Table 2 | ± 2.0 or (1) ± 100 | nA % |
| 21 to 24 | D.C. Forward Current Transfer Ratio 2 | h_{FE2} | As per Table 2 | As per Table 2 | ± 15 | % |
| 33 to 36 | Collector-Emitter Saturation Voltage 1 | $V_{CE(sat)1}$ | As per Table 2 | As per Table 2 | ± 30 or (1) ± 15 | mV % |

NOTES

1. Whichever is greater, referred to the initial value.

**TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS**

| No. | CHARACTERISTICS | SYMBOL | CONDITIONS | UNIT |
|-----|---|-----------|----------------|------|
| 1 | Ambient Temperature | T_{amb} | + 20 to + 50 | °C |
| 2 | Collector-Base Voltage | V_{CB} | 10 to 40 | V |
| 3 | Power Dissipation Single Section 4 Sections | P_{tot} | 0.125 0.500 | W |

FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS**NOTES**

1. V_{CB} set for 30V.
2. V_1 adjusted so that $P_{tot} = \text{max. rating at } T_{amb}$ according to derating curve.
3. R chosen according to availability of V_1 , as long as: $V_1 + V_{CB} < V_{CEO}$.
4. Circuit repeated 4 times.



- 4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 5000)
- 4.8.1 Electrical Measurements on Completion of Environmental Tests
The parameters to be measured on completion of environmental tests are scheduled in Table 2. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.
- 4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests
The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 6 of this specification. The measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.
- 4.8.3 Conditions for Operating Life Tests (Part of Endurance Testing)
The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be the same as specified in Table 5 for the power burn-in test.
- 4.8.4 Electrical Circuits for Operating Life Tests
The circuit to be used for performance of the operating life test shall be the same as specified in Figure 5 for power burn-in.
- 4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)
The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

**TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING**

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | LIMITS | | UNIT |
|----------|--|----------------|--------------------------|-----------------|--------|------|------|
| | | | | | MIN. | MAX. | |
| 13 to 16 | Collector-Base Cut-off Current | I_{CBO} | As per Table 2 | As per Table 2 | - | 10 | nA |
| 25 to 28 | D.C. Forward Current Transfer Ratio 2 | h_{FE2} | As per Table 2 | As per Table 2 | 100 | 300 | - |
| 33 to 36 | Collector-Emitter Saturation Voltage 1 | $V_{CE(sat)1}$ | As per Table 2 | As per Table 2 | - | 0.3 | V |