ESCC
European Space Components Coordination

Pages 1 to 27

TRANSISTORS, MICROWAVE, FIELD EFFECT, LOW NOISE, GALLIUM ARSENIDE BASED ON TYPES CFY25 AND CFY27

ESCC Detail Specification No. 5613/008

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DCR No.	CHANGE DESCRIPTION

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Transistor, Microwave, Field Effect, Low Noise and General Purpose, Gallium Arsenide, based on Types CFY25 and CFY27. It shall be read in conjunction with ESCC Generic Specification No. 5010, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type components specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the components specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the components specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the components specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification of the components specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and handling.

These components are catagorised as follows:-

(a) Variants 01 and 02 (CFY27) - Class 1 with a Minimum Critical Path Failure Voltage of 750V.

(b) Variants 03 to 07 (CFY25) - Class 1 with a Minimum Critical Path Failure Voltage of 250V.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components.

(b) MIL-STD-750, Test Methods for Semiconductor Devices.

TABLE 1(a) - TYPE VARIANTS

(1) VARIANT	(2) BASED ON TYPE	(3) CASE	(4) FIGURE	(5) NOISE FIGURE @ 12GHz NF_{min} (dB)	(6) ASSOCIATED GAIN @ 12GHz G_a (dB)	(7) OUTPUT POWER @ 12 GHz P_{-1dB} (dB)	(8) LINEAR GAIN @ 12GHz G_{lp} (dB)	(9) LEAD MATERIAL AND FINISH
01	CFY27-38	Micro-X	2	≤3.8	≥7.5	N/A	N/A	D2
02	CFY27-P	Micro-X	2	N/A	N/A	≥24.5 (Note 1)	≥17.5 (Note 1)	D2
03	CFY25-20P	Micro-X	2	≤2.1	≥8.5	≥14.0	≥8.5	D2
04	CFY25-20	Micro-X	2	≤2.1	≥8.5	N/A	N/A	D2
05	CFY25-23P	Micro-X	2	≤2.4	≥8.0	≥14.0	≥8.0	D2
06	CFY25-23	Micro-X	2	≤2.4	≥8.0	N/A	N/A	D2
07	CFY25-P	Micro-X	2	N/A	N/A	≥14.0	≥8.5	D2

NOTES:

1. P_{-1dB} and G_{lp} for Variant 02 measured at 2.3 GHz.

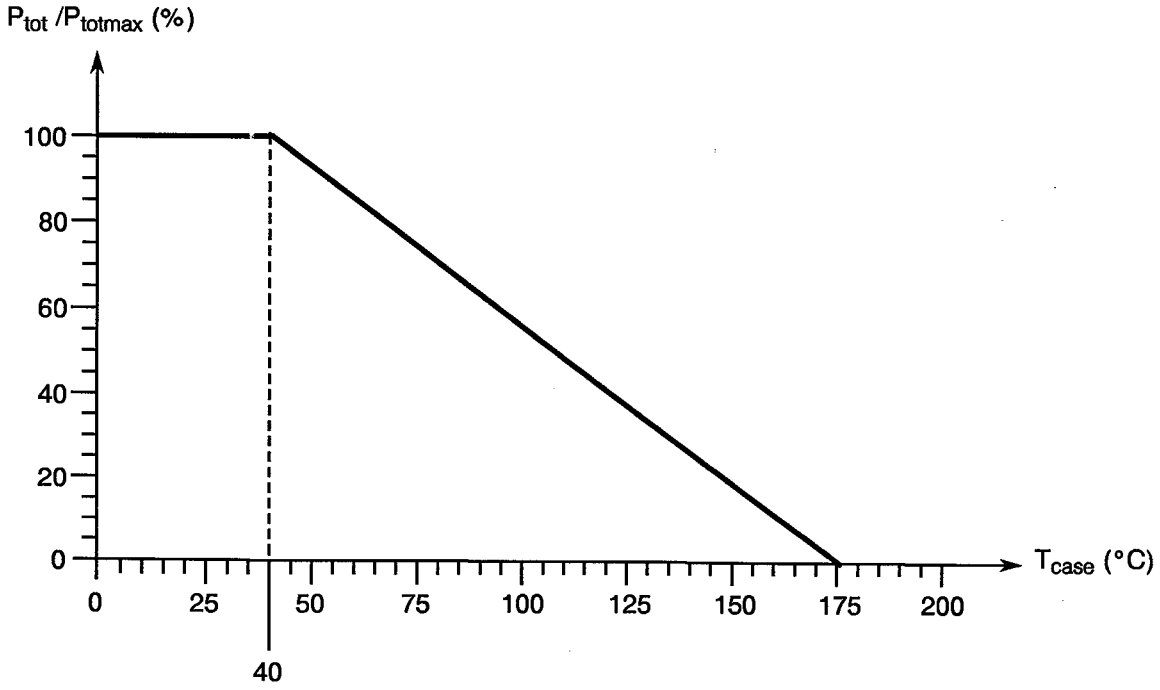
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain-Source Voltage Variants 01 and 02 Variants 03 to 07	V_{DS}	 9 5	V	
2	Drain-Gate Voltage Variants 01 and 02 Variants 03 to 07	V_{DG}	 11 7	V	
3	Gate-Source Voltage Variants 01 and 02 Variants 03 to 07	V_{GS}	 -6 to +0.5 -5 to +0.5	V	
4	Drain Current Variants 01 and 02 Variants 03 to 07	I_D	 385 at V_{DS} <2.0V 80 at V_{DS} <4.1V	mA	Note 1
5	Operational Gate Current Variants 01 and 02 Variants 03 to 07	I_{Go}	 5 1.5	mA	
6	RF Input Power, X-Band Variants 01 and 02 Variants 03 to 07	P_{RFin}	 21 at $V_{DS} \leq 5V$ 17 at $V_{DS} \leq 3.5V$	dBm	Note 2
7	Compression Level Variants 01 and 02 Variants 03 to 07	P_c	 4 at $V_{DS} \leq 5V$, $80mA < I_D < 140mA$ 4 at $V_{DS} \leq 3.5V$, $15mA < I_D < 30mA$	dB	Note 2
8	Power Dissipation Variants 01 and 02 Variants 03 to 07	P_{tot}	 770 330	mW	Note 1
9	Channel Temperature Range	T_{ch}	- 65 to +175	°C	
10	Storage Temperature Range	T_{stg}	−65 to +175	°C	
11	Soldering Temperature	T_{sol}	+230	°C	Note 3

NOTES:

1. At T_{case} = +40°C. For derating at T_{case} > +40°C, see Figure 1.
2. Under continuous wave.
3. Duration 15 seconds maximum for the leads. The same termination shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

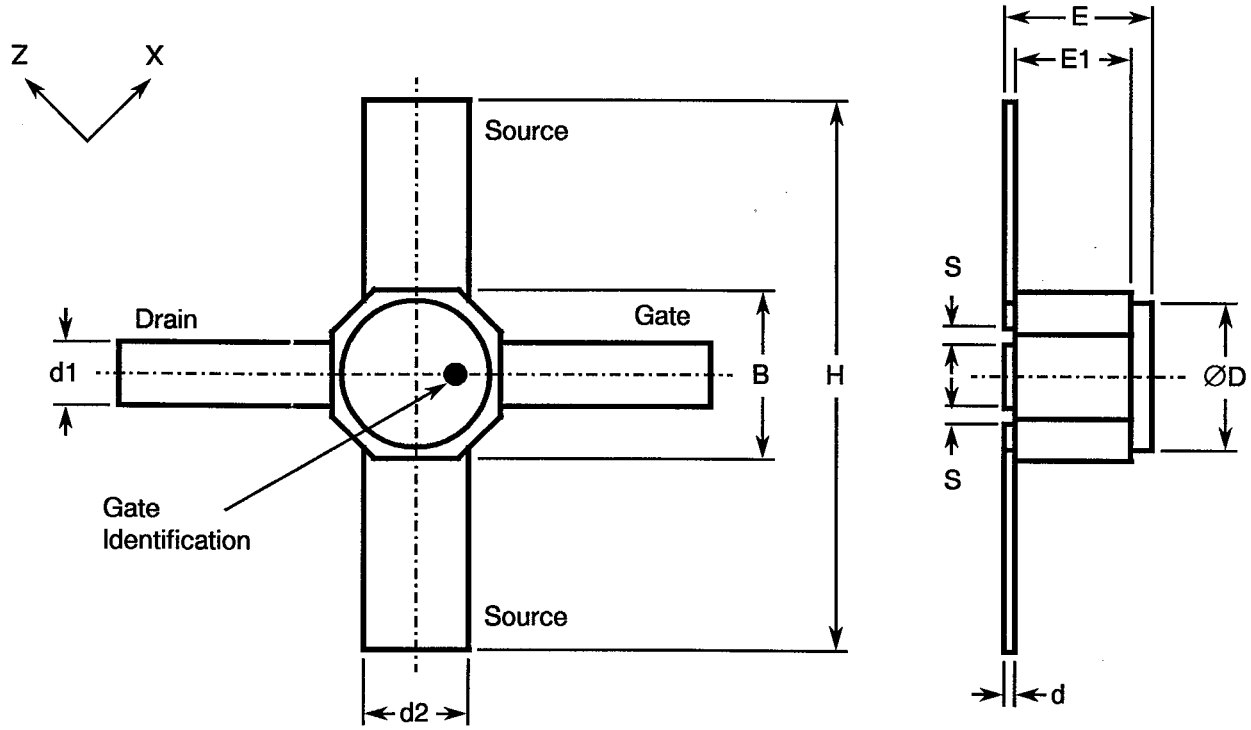


Power Dissipation versus Temperature

NOTES

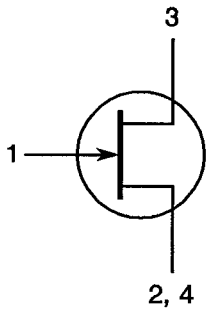
1. Thermal Resistance ($R_{TH(ch-c)}$)
   Variants 01 and 02: 175 °C/W.
   Variants 03 to 07: 410 °C/W.

FIGURE 2 - PHYSICAL DIMENSIONS



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
B	1.68	1.88	
d	0.07	0.15	
d1	0.40	0.60	
d2	0.92	1.12	
ØD	1.55	1.85	
E	0.85	1.25	
E1	0.66	0.86	
H	4.00	4.40	
S	0.08	0.30	

FIGURE 3 - FUNCTIONAL DIAGRAM



1. Gate
2, 4 Source
3. Drain

NOTES:

1. The gate is marked with a black dot.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following symbols are used:-

D	=	Drain.
G	=	Gate.
G_{lp}	=	Linear (small signal) Gain for Power Matching Condition.
G_p	=	Power Gain for Power Matching Condition.
g_m	=	Transconductance.
I_D	=	Drain Current.
$I_{Dpl, h}$	=	Drain Leakage Current at Pinch-off (l: at low voltages, h: at high voltages).
I_{Dq}	=	Drain Quiescent Current (Drain Operational Current without RF Excitation).
I_{DSS}	=	Drain Saturation Current for Shorted Gate ($V_{GS} = 0$).
I_G	=	Gate Current.
I_{GO}	=	Gate DC Current under RF (Gate Operational Mean Current under RF Excitation).
$I_{Gpl, h}$	=	Gate Leakage Current at Pinch-off (l: at low voltages, h: at high voltages).
P_c	=	Power Gain Compression Level.
P_{DC}	=	Dissipated DC Power.
P_{in}	=	RF Input Power.
P_{out}	=	RF Output Power.
P_{tot}	=	Power Dissipation ($= P_{DC} + P_{in} - P_{out}$).
P_{-1dB}	=	Output Power at 1dB Gain Compression.
R_D	=	External Drain Resistance.
R_G	=	External Gate Resistance.
R_S	=	External Source Resistance.
$R_{TH(ch-c)}$	=	Thermal Resistance, Channel to Case.
$R_{TH(S-A)}$	=	Thermal Resistance, Soldering Point to Ambient.
S	=	Source.
V_{DD}	=	Output Voltage from Drain Power Supply.
V_{DG}	=	Drain-Gate Voltage.
V_{DS}	=	Drain-Source Voltage.
V_{GG}	=	Output Voltage from Gate Power Supply.
V_{GS}	=	Gate-Source Voltage.
V_{GSth}	=	Gate-Source Threshold Voltage (Turn-on Voltage).
V_{SS}	=	Output Voltage from Source Power Supply (Ground).

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the components specified herein shall be as stated in this specification and ESCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Production Control

None.

4.2.2 Deviations from Final Production Tests (Chart II(b))

(a) Para. 9.5, Thermal Shock: May also be performed in accordance with MIL-STD-883, Test Method 1010, Test Condition C.

(b) Para. 9.7, Particle Impact Noise Detection (PIND) Test: May be performed at any point after the position indicated in Chart II(b), but before final seal test, gross leak and fine leak.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III(b))

(a) Para. 9.9.2, Table 3 measurements: May be performed at any stage after power burn-in.

(b) Para. 9.9.3, Table 2 measurements: May be performed at any stage after power burn-in.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Paras. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, Constant Acceleration shall not be performed.

(b) Para. 9.13, Shock Test: Shall not be performed.

(c) Para. 9.14, Vibration Test: Shall not be performed.

(d) Para. 9.15, Constant Acceleration: Shall not be performed.

(e) Para. 9.23, Special Testing: Shall not be performed.

(f) Assembly/Capability tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability test sequence.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Paras. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, Constant Acceleration shall not be performed.

(b) Para. 9.13, Shock Test: Shall not be performed.

(c) Para. 9.14, Vibration Test: Shall not be performed.

(d) Para. 9.15, Constant Acceleration: Shall not be performed.

(e) Para. 9.23, Special Testing: Shall not be performed.

(f) Assembly/Capability tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability test sequence.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the components specified herein shall be 0.03 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A' (Tension).

(b) Force: 2.2N.

(c) Duration: 5 seconds.

4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A'.

(b) Bond Strength:

Variants 01 and 02: 0.03N force minimum at pre-seal tests, 0.025N force minimum at post-seal tests.

Variants 03 to 07: 0.015N force minimum at pre-seal tests, 0.012N force minimum at post-seal tests.

4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be alternatively as follows:-

(a) Minimum acceptable die shear strengths:

Variants 01 and 02: 1.6N.

Variants 03 to 07: 0.7N.

(b) In those cases where the clearances in the package do not allow application of the die shear force with a suitable tool, the chip shall be pushed away with a suitable tool and the die attach area inspected afterwards.

Sufficient die attach quality is achieved if objective evidence for sufficient mechanical and thermal contact is found, i.e. more than 50% semiconductor material remains.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the

requirements of ESCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Terminal Identification.

(b) The ESCC Component Number.

(c) Traceability Information.

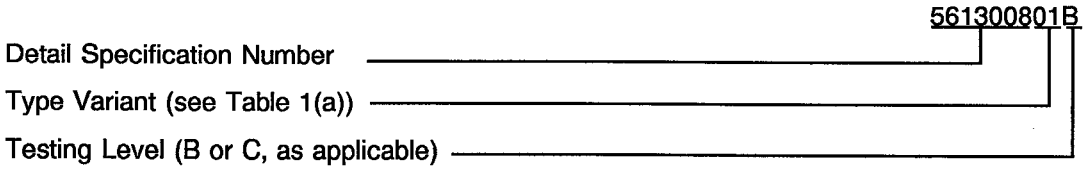
The primary package shall bear an "ESD sensitive" label.

4.5.2 Terminal Identification

Terminal identification shall be as shown in Figures 2 and 3 of this specification.

4.5.3 The ESCC Component Number

Each component shall bear the ESCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_{amb} = +25±3 °C.

Within their part types, those components which fail to achieve their specified RF Classification may be assigned to another type variant, after final electrical measurements.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at T_{amb} = +140(+0−5)°C.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

Burn-in shall be to Chart III(b) of ESCC Generic Specification No. 5010.

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_{amb} = +25±3 °C. The parameter

drift values (Δ) applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

The requirements for high temperature reverse bias burn-in are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for high temperature reverse bias burn-in shall be as specified in Table 5(a) of this specification.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn-in

The circuit for use in performing the high temperature reverse bias burn-in test is the general burn-in circuit shown in Figure 5 of this specification.

4.7.5 Electrical Circuit for Power Burn-in

The circuit for use in performing the power burn-in test is shown in Figure 5 of this specification.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESCC GENERIC SPECIFICATION No. 5010)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Conditions for Operating Life Test (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.4 Electrical Circuit for Operating Life Test

The circuit for use in performing the operating life test shall be the same as shown in Figure 5 of this specification for power burn-in.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - DC PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Drain Leakage Current at Pinch-off 1 (high V_{DS})	I_{Dph}	4(a)	V_{GS} = -4V Variants 01 and 02: V_{DS} = 7V Variants 03 to 07: V_{DS} = 3V	 - -	 480 300	µA
2	Gate Leakage Current at Pinch-off 1 (high V_{DS})	$-I_{Gph}$	4(a)	V_{GS} = −4V Variants 01 and 02: V_{DS} = 7V Variants 03 to 07: V_{DS} = 3V	 - -	 240 200	µA
3	Drain Leakage Current at Pinch-off 2 (low V_{DS})	I_{Dpl}	4(a)	V_{GS} = −3.5V Variants 01 and 02: V_{DS} = 3V Variants 03 to 07:	 - -	 96 N/A	µA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS})	$-I_{Gpl}$	4(a)	V_{GS} = −3.5V Variants 01 and 02: V_{DS} = 3V Variants 03 to 07:	 - -	 48 N/A	µA
5	Drain Saturation Current	I_{DSS}	4(a)	V_{GS} = 0V Variants 01 and 02: V_{DS} = 2V Variants 03, 05, 07: V_{DS} = 3V Variants 04, 06: V_{DS} = 3V	 150 25 15	 385 60 60	mA
6	Gate-Source Threshold Voltage	$-V_{Gth}$	4(a)	V_{DS} = 3.0V Variants 01 and 02: I_D = 12mA Variants 03 to 07: I_D = 1mA	 0.9 0.3	 3.2 3.0	V
7	Transconductance	g_m	4(a)	V_{DS} = 3.0V Variants 01 and 02: I_D = 120mA Variants 03 to 07: I_D = 15mA	 130 35	 - -	mS
8	Gate Quiescent Bias Current	$-I_{Gq}$	4(a)	V_{DS} = 3.0V Variants 01 and 02: Variants 03 to 07: I_D = 15mA	 - -	 N/A 2.0	µA

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - AC PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
9	Noise Figure (Note 1)	NF_{min}	4(b)	V_{DS} = 3V, f = 12GHz Variant 01: I_{Dq} = 120mA Variants 03 to 06: I_{Dq} = 15mA Variants 02, 07:	 - - -	 Note 2 Note 2 N/A	dB
10	Associated Gain (Note 1)	G_a	4(b)	V_{DS} = 3V, f = 12GHz Variant 01: I_{Dq} = 120mA Variants 03 to 06: I_{Dq} = 15mA Variants 02, 07:	 Note 3 Note 3 N/A	 - - -	dB
11	Output Power at 1dB Gain Compression (Note 4)	P_{-1dB}	4(c)	Variant 02: V_{DS} = 5V, f = 2.3GHz, I_{Dq} = 120mA Variants 03, 05, 07: V_{DS} = 3V, f = 12GHz, I_{Dq} = 20mA Variants 01, 04, 06	 Note 5 Note 5 N/A	 - - -	dBm
12	Linear Power Gain, P_{in} = 0dBm (Note 4)	G_{lp}	4(c)	Variant 02: V_{DS} = 5V, f = 2.3GHz, I_{Dq} = 120mA Variants 03, 05, 07: V_{DS} = 3V, f = 12GHz, I_{Dq} = 20mA Variants 01, 04, 06	 Note 6 Note 6 N/A	 - - -	dB
13	S-Parameters (Note 7)	S_{11}, S_{21}, S_{12}, S_{22}	4(d)	V_{DS} = 3V, f = 1 to 15GHz Variants 01 and 02: I_{Dq} = 120mA Variants 03 to 07: I_{Dq} = 15mA	(Note 8)		Mag, Ang

NOTES

1. Input and output matched for minimum Noise Figure.
2. See Column 5 of Table 1(a).
3. See Column 6 of Table 1(a).
4. Input and output matched for maximum P_{-1dB}.
5. See Column 7 of Table 1(a).
6. See Column 8 of Table 1(a).
7. Under matched condition (Z = 50Ω). Shall be performed on 4 assembled samples per wafer after Burn-in.
8. No specific limits applicable. The parameters are read and record for information only.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Drain Leakage Current at Pinch-off 1 (high V_{DS})	I_{Dph}	4(a)	See Table 2 Variants 01 and 02: Variants 03 to 07:	 - -	 2.4 1.5	mA
2	Gate Leakage Current at Pinch-off 1 (high V_{DS})	$-I_{Gph}$	4(a)	See Table 2 Variants 01 and 02: Variants 03 to 07:	 - -	 1.2 1.0	mA
3	Drain Leakage Current at Pinch-off 2 (low V_{DS}) (Note 1)	I_{Dpl}	4(a)	See Table 2 Variants 01 and 02: Variants 03 to 07:	 - -	 0.48 N/A	mA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS}) (Note 1)	$-I_{Gpl}$	4(a)	See Table 2 Variants 01 and 02: Variants 03 to 07:	 - -	 0.24 N/A	mA
6	Gate-Source Threshold Voltage (Note 1)	$-V_{Gth}$	4(a)	See Table 2 Variants 01 and 02: Variants 03 to 07:	 0.7 0.2	 3.4 3.2	V
7	Transconductance (Note 1)	g_m	4(a)	V_{DS} see Table 2 Variants 01 to 03: $I_D = 54mA$ Variants 03 to 07: see Table 2	 80 25	 - -	mS

NOTES:

1. Shall be performed on 5 assembled samples per wafer. If a failure occurs, 100% measurements shall be performed.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - TEST CIRCUIT FOR DC PARAMETERS

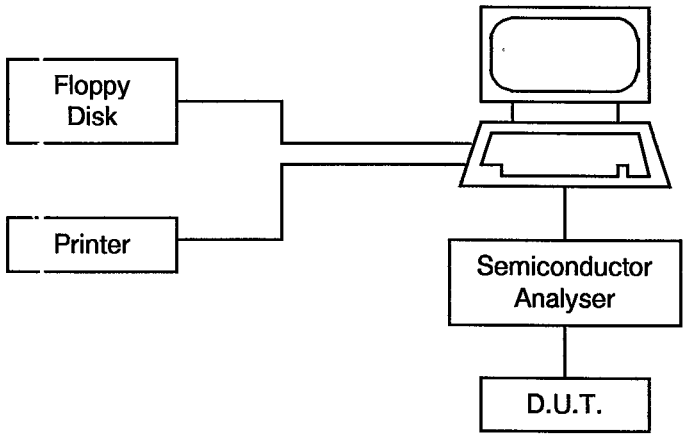


FIGURE 4(b) - TEST SET-UP FOR NOISE FIGURE MEASUREMENT

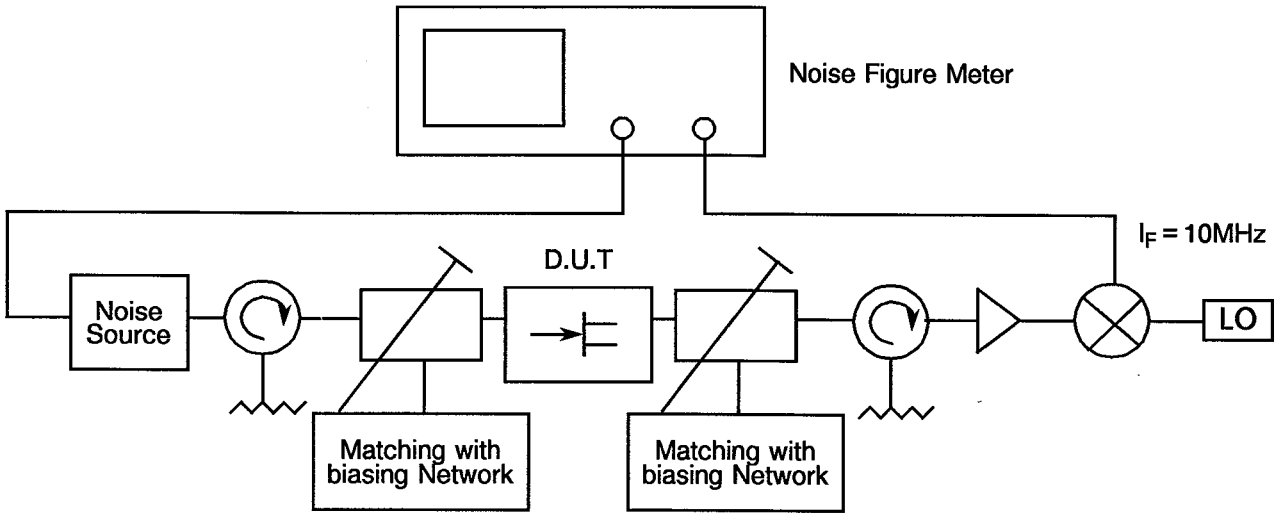


FIGURE 4(c) - TEST CIRCUIT FOR OUPUT POWER MEASURMENTS

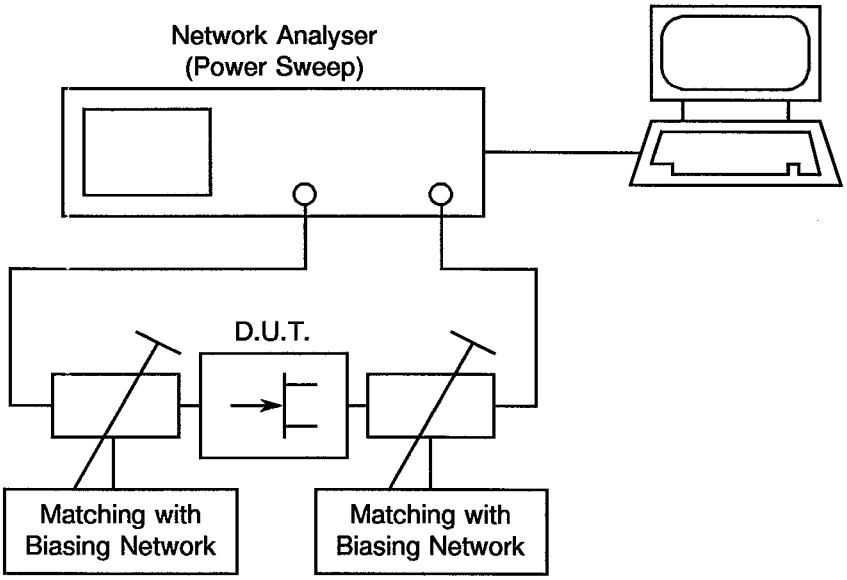


FIGURE 4(d) - TEST SET-UP FOR SCATTERING PARAMETER MEASUREMENTS

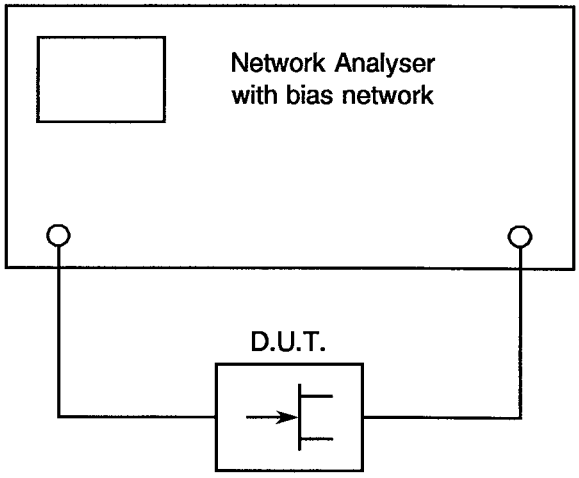


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Drain Leakage Current at Pinch-off 1 (high V_{DS})	I_{Dph}	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 N/A ±150	µA
2	Gate Leakage Current at Pinch-off 1 (high V_{DS})	$-I_{Gph}$	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 N/A ±100	µA
3	Drain Leakage Current at Pinch-off 2 (low V_{DS})	I_{Dpl}	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 ±48 N/A	µA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS})	$-I_{Gpl}$	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 ±24 N/A	µA
5	Drain Saturation Current	I_{DSS}	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 ±30 ±2.5	mA
6	Gate Source Threshold Voltage	$-V_{Gth}$	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 ±0.2 ±0.1	V
7	Transconductance	g_m	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 ±18 ±2.5	mS
9	Noise Figure (Note 1)	NF_{min}	4(b)	See Table 2 Variants 01, 03 to 06 Variants 02, 07	 ±0.15 N/A	dB
10	Associated Gain (Note 1)	G_a	4(b)	See Table 2 Variants 01, 03 to 06 Variants 02, 07	 ±0.4 N/A	dB
11	Output Power @ 1dB Gain Compression (Note 1)	P_{-1dB}	4(b)	See Table 2 Variants 01, 04, 06 Variants 02, 03, 05, 07	 N/A -0.2 / +0.5	dB
12	Linear Power Gain (Note 1)	G_{lp}	4(b)	See Table 2 Variants 01, 04, 06 Variants 02, 03, 05, 07	 N/A ±0.4	dB

NOTES

1. Drift in RF-performance shall only be evaluated for completed burn-in, i.e. initial measurements are before H.T.R.B. and final measurements are after burn-in.
2. $\Delta 1 = \Delta 2$.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+140 (+0 -5)	°C
2	Gate Source Voltage	V_{GS}	Variants 01, 02: -5 (+0.2 -0) Variants 03 to 07: -4 (+0.2 -0)	V
3	Drain Source Voltage	V_{DS}	Variants 01, 02: 6 (+0.2 -0) Variants 03 to 07: 3 (+0.2 -0)	V

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+125 (Note 1)	°C
2	Channel Temperature	T_{ch}	+175 (+0 -5)	°C
3	Drain Source Voltage	V_{DS}	3 (+0 -0.2)	V
4	Drain Current	I_D	Variants 01 and 02: 54 Variants 03 to 07: 30 (±10%, Note 2)	mA

NOTES

Because the components are mechanically clamped to the burn-in fixture, an additional thermal resistance soldering point to ambient, e.g. $R_{TH(S-A)} = 145°C/W$ must be considered for the calculation of T_{ch}.

1. T_{amb} shall be adjusted to provide the required T_{ch}.
2. The limits given for T_{ch} shall not be exceeded.

FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN

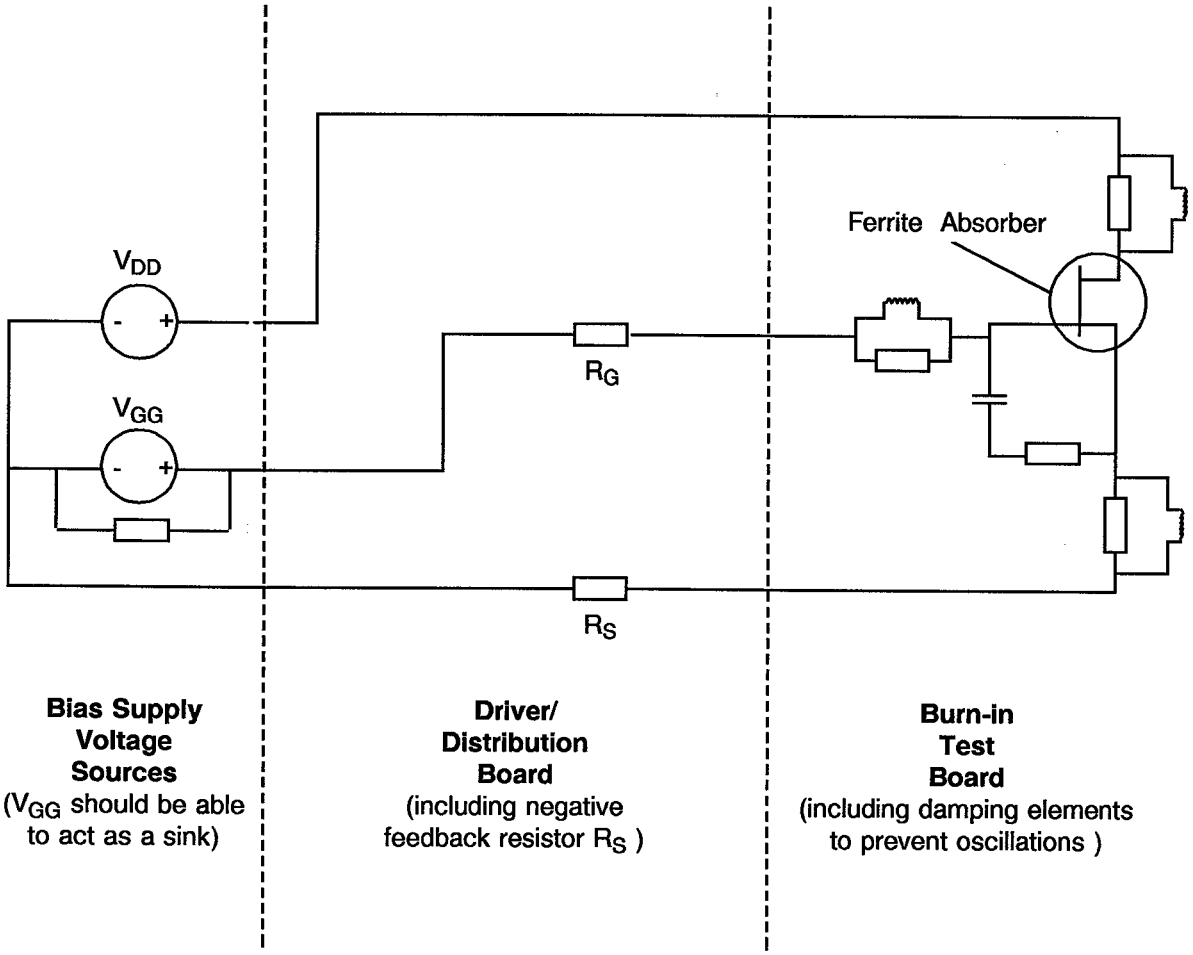
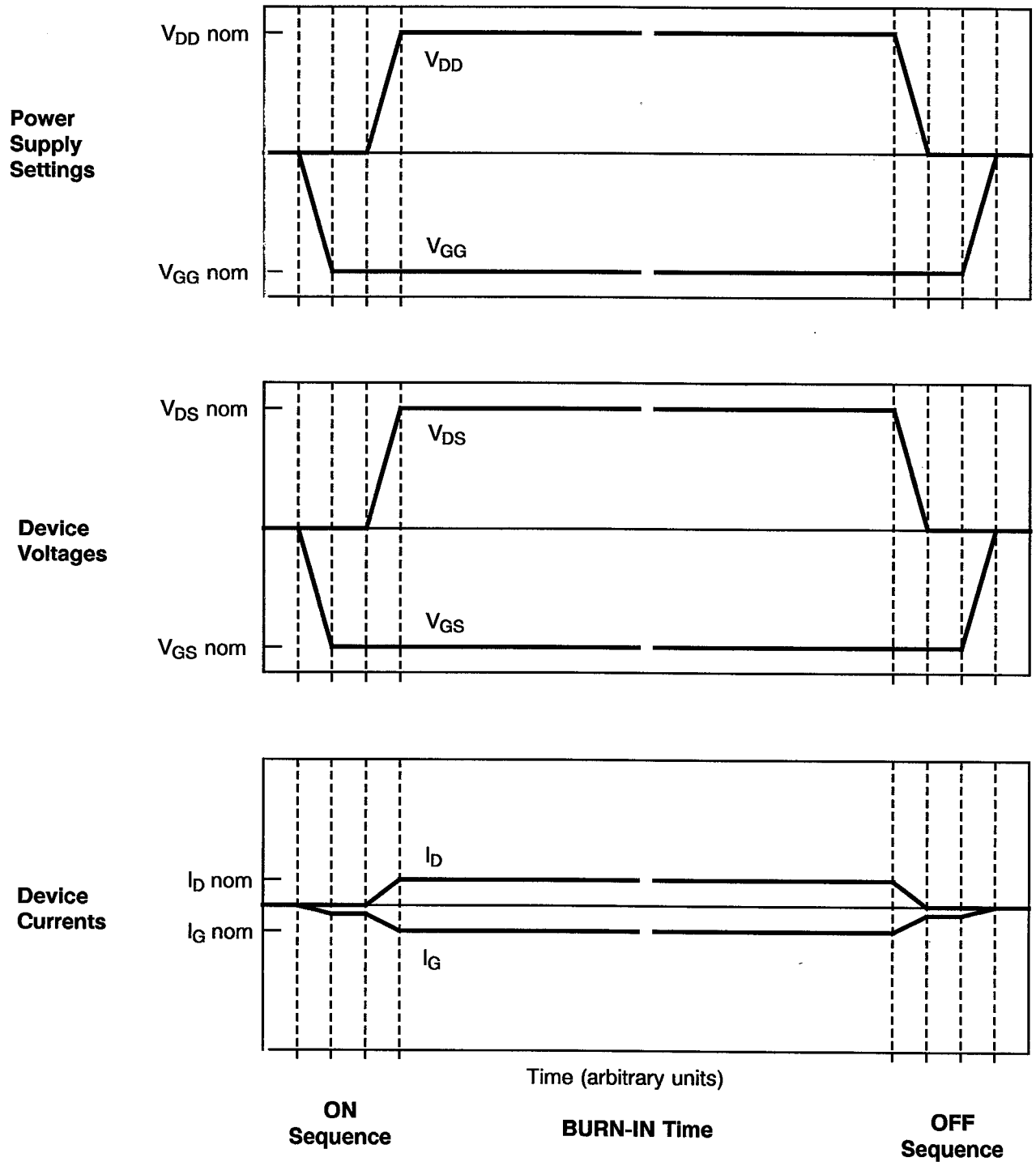


FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN (CONTINUED)

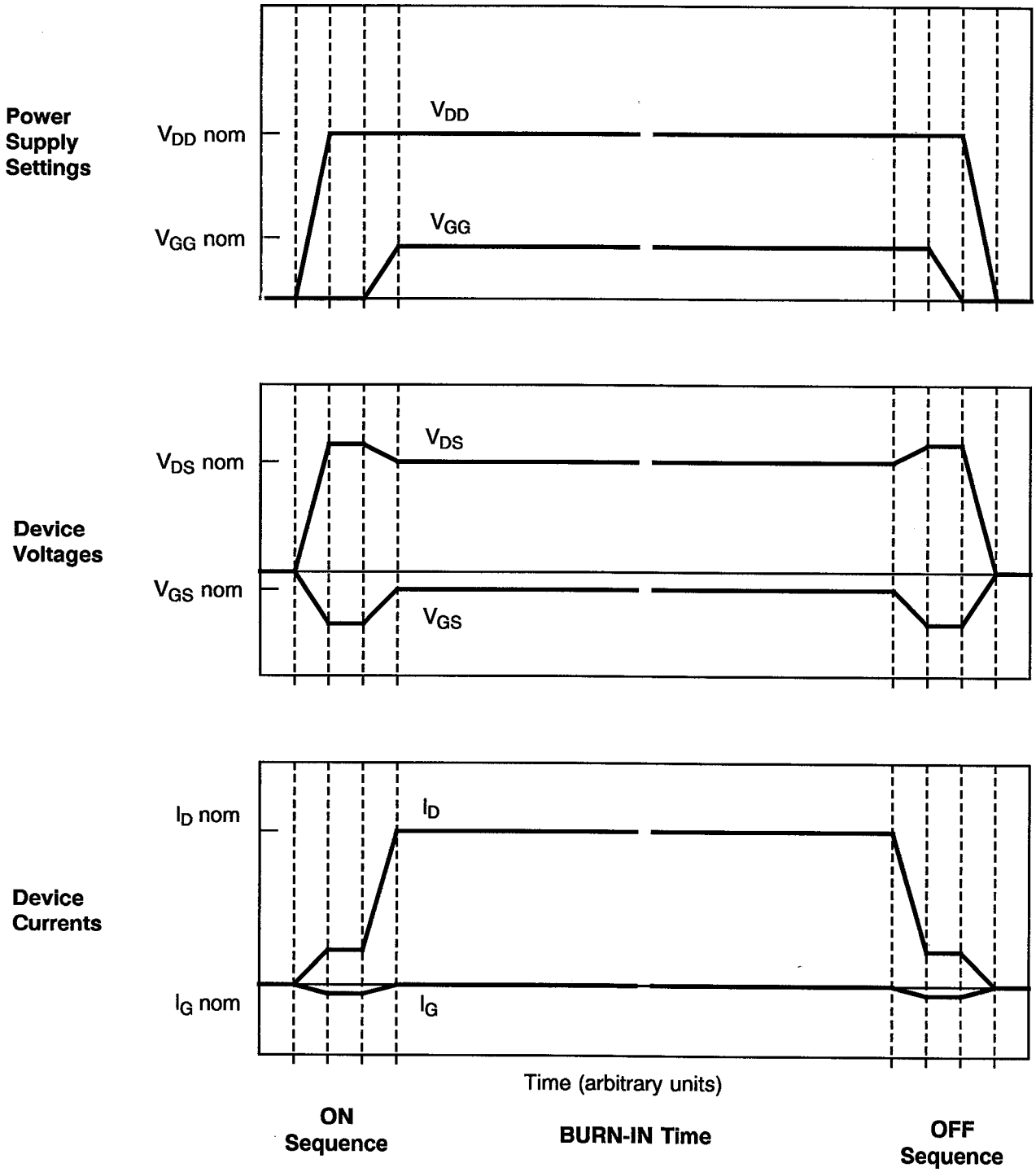
TIMING SEQUENCE FOR H.T.R.B. ON/OFF BIASING



NOTES: See Page 24.

FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN (CONTINUED)

TIMING SEQUENCE FOR POWER BURN-IN ON/OFF BIASING



NOTES:

1. The maximum ratings for V_{DS} and V_{GS} shall not be exceeded during the ON- or OFF-sequence. In case of jeopardy, increase of V_{DD} and V_{GG} during ON-sequence in multiple steps and decrease of V_{GG} and V_{DD} during OFF-sequence in multiple steps shall be performed.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		CHANGE LIMITS (Δ)	UNIT
					MIN.	MAX.		
1	Drain Leakage Current at Pinch-off 1 (high V_{DS})	I_{Dph}	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 - -	 600 375	 N/A ±150	µA
2	Gate Leakage Current at Pinch-off 1 (high V_{DS})	$-I_{Gph}$	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 - -	 300 250	 N/A ±100	µA
3	Drain Leakage Current at Pinch-off 2 (low V_{DS})	I_{Dpl}	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 - -	 120 N/A	 ±48 N/A	µA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS})	$-I_{Gpl}$	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 - -	 60 N/A	 ±24 N/A	µA
5	Drain Saturation Current	I_{DSS}	4(a)	See Table 2 Variants 01 and 02 Variants 03, 05, 07 Variants 04, 06	 140 20 14	 420 65 65	 ±30 ±2.5	mA
6	Gate-Source Threshold Voltage	$-V_{Gth}$	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 0.8 0.2	 3.3 3.1	 ±0.2 ±0.1	V
7	Transconductance	g_m	4(a)	See Table 2 Variants 01 and 02 Variants 03 to 07	 120 33	 - -	 ±18 ±2.5	mS
9	Noise Figure	NF_{min}	4(a)	See Table 2 Variants 01, 03 to 06 Variants 02, 07	 - -	 (Note 1) N/A	 ±0.15 N/A	dB
10	Associated Gain	G_a	4(b)	See Table 2 Variants 01, 03 to 06 Variants 02, 07	 (Note 2) N/A	 - -	 ±0.4 N/A	dB
11	Output Power @ 1dB Gain Compression	P_{-1dB}	4(b)	See Table 2 Variants 01, 04, 06 Variants 02, 03, 05, 07	 N/A (Note 2)	 - -	 N/A ±0.3	dBm
12	Linear Power Gain	G_{lp}	4(b)	See Table 2 Variants 01, 04, 06 Variants 02, 03, 05, 07	 N/A (Note 2)	 - -	 N/A ±0.4	dB

NOTES:

1. As per Table 2, increased by 0.1dB.
2. As per Table 2, reduced by 0.2dB.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

Not applicable.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

Not applicable.

APPENDIX 'A'

AGREED DEVIATIONS FOR INFINEON TECHNOLOGIES (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para 4.2.1	Paras. 5.2.4 and 10.5: If Wafer Lot Acceptance Test Data is specified in the purchase order, such data will not be delivered but will be available for review at Infineon Technologies.
Para. 4.2.2	Para. 9.11, Dimension Check: May be performed on a 100% basis using a gauge during RF Measurements.
Para. 4.2.3	Para. 9.12, Radiographic Inspection: May be replaced by a Visual Inspection for verifying the length, height and shape of the wire bonding.
Para. 4.2.5	Para. 8.2.3, Lot Acceptance Level 3 Testing (LA3), (e): Witnessing of LA3 testing by the Orderer is only forseen for the Electrical Measurements at Room Temperature - DC Parameters. Notification of the Orderer shall be made 5 working days before the commencement of this testing.