ESCC
European Space Components Coordination

INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS 32/40-BIT IEEE FLOATING POINT

DIGITAL SIGNAL PROCESSOR,

BASED ON TYPE TSC 21020 F

ESCC Detail Specification No. 9512/002

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DCR No.	CHANGE DESCRIPTION
142	Specification up issued to incorporate editorial/technical changes per DCR.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specfied in ESCC Basic specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 951200201R

- Detail Specification Reference: 9512002
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and/or Finish	Weight max g	Total Dose Radiation Level Letter
01	TSC21020F	MQFP-F256	G2	15	R [100kRAD(Si)]

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the purchase order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum rating shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to +7	V	1
Input Voltage	V_{IN}	-0.5 to V_{DD} +0.5	V	2
Output Current	I_{OUT}	50	mA	3
Power Dissipation (continuous)	P_D	3.4	W	
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Soldering Temperature	T_{sol}	+265	°C	4
Junction Temperature	T_j	+165	°C	
Thermal Resistance	$R_{th(J-C)}$	3	°C/W	Junction to Case

NOTES

1. Device is functional from +4.5V to +5.5V with reference to V_{SS} = 0V.
2. V_{DD} +0.5V should not exceed +7V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

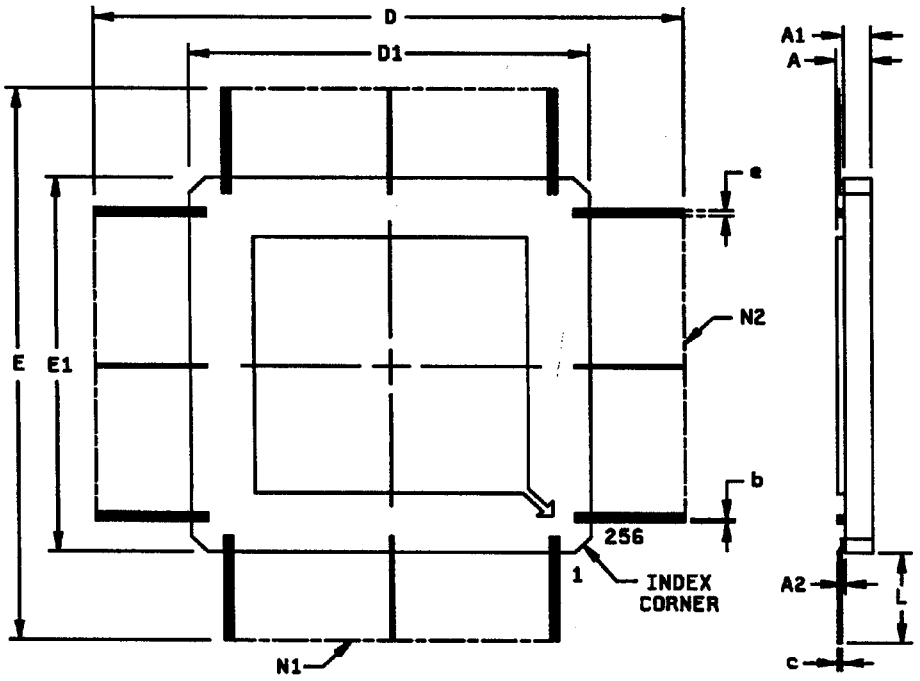
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 volts.

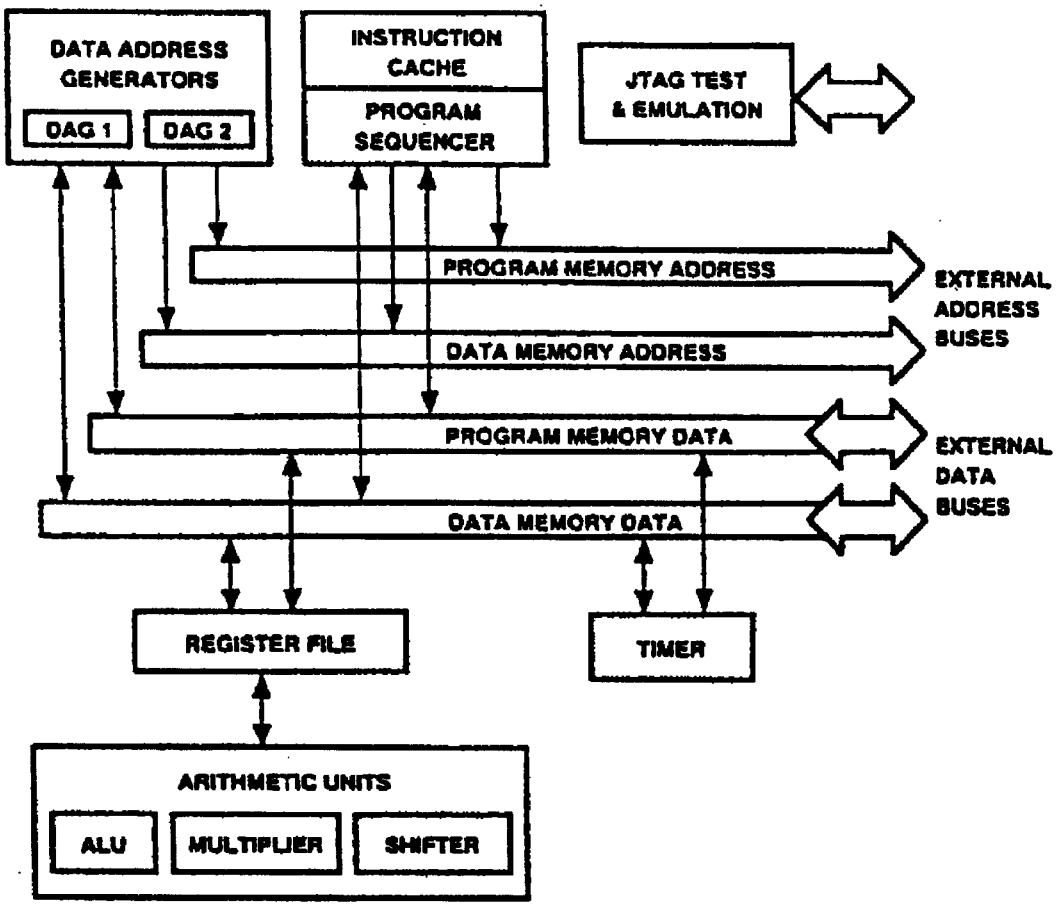
1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 256 Flat Leaded Multilayer Quad Flat Package - MQFP-F256



Dimension	mm	
	Min	Max
A	2.41	3.18
A1	2.06	2.56
A2	0.05	0.36
b	0.15	0.25
c	0.1	0.2
D, E	53.23	55.74
D1, E1	36.83	37.34
e	0.508 BSC	
L	8.2	9.2
N1, N2	64	

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT AND DESCRIPTION

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	IV_{SS}	33	IV_{SS}	65	IV_{SS}	97	IV_{SS}
2	IV_{DD}	34	IV_{DD}	66	IV_{DD}	98	IV_{DD}
3	$\overline{DMD_{19}}$	35	PMD_3	67	PMD_{25}	99	EV_{SS}
4	$\overline{DMD_{18}}$	36	EV_{DD}	68	PMD_{26}	100	$\overline{PMTS}$
5	$\overline{DMD_{17}}$	37	PMD_4	69	PMD_{27}	101	$\overline{PMWR}$
6	$\overline{DMD_{16}}$	38	PMD_5	70	EV_{DD}	102	PMACK
7	EV_{SS}	39	PMD_6	71	PMD_{28}	103	$\overline{PMRD}$
8	$\overline{DMD_{15}}$	40	PMD_7	72	PMD_{29}	104	RCMP
9	$\overline{DMD_{14}}$	41	EV_{SS}	73	PMD_{30}	105	EV_{DD}
10	$\overline{DMD_{13}}$	42	PMD_8	74	PMD_{31}	106	$\overline{RESET}$
11	$\overline{DMD_{12}}$	43	PMD_9	75	EV_{SS}	107	CLKIN
12	EV_{DD}	44	PMD_{10}	76	PMD_{32}	108	$\overline{DMRD}$
13	$\overline{DMD_{11}}$	45	PMD_{11}	77	PMD_{33}	109	DMACK
14	$\overline{DMD_{10}}$	46	EV_{DD}	78	PMD_{34}	110	$\overline{DMWR}$
15	$\overline{DMD_9}$	47	PMD_{12}	79	PMD_{35}	111	EV_{DD}
16	$\overline{DMD_8}$	48	PMD_{13}	80	EV_{DD}	112	$\overline{DMTS}$
17	IV_{SS}	49	IV_{SS}	81	IV_{SS}	113	IV_{SS}
18	IV_{DD}	50	IV_{DD}	82	IV_{DD}	114	IV_{DD}
19	EV_{SS}	51	PMD_{14}	83	PMD_{36}	115	TCK
20	$\overline{DMD_7}$	52	PMD_{15}	84	PMD_{37}	116	TMS
21	$\overline{DMD_6}$	53	EV_{SS}	85	PMD_{38}	117	TDI
22	$\overline{DMD_5}$	54	PMD_{16}	86	PMD_{39}	118	TDO
23	$\overline{DMD_4}$	55	PMD_{17}	87	EV_{SS}	119	$\overline{TRST}$
24	EV_{DD}	56	PMD_{18}	88	PMD_{40}	120	PMPAGE
25	$\overline{DMD_3}$	57	PMD_{19}	89	PMD_{41}	121	$\overline{PMS_0}$
26	$\overline{DMD_2}$	58	EV_{DD}	90	PMD_{42}	122	$\overline{PMS_1}$
27	$\overline{DMD_1}$	59	PMD_{20}	91	PMD_{43}	123	EV_{SS}
28	$\overline{DMD_0}$	60	PMD_{21}	92	EV_{DD}	124	PMA_{23}
29	EV_{SS}	61	PMD_{22}	93	PMD_{44}	125	PMA_{22}
30	PMD_0	62	PMD_{23}	94	PMD_{45}	126	PMA_{21}
31	PMD_1	63	EV_{SS}	95	PMD_{46}	127	PMA_{20}
32	PMD_2	64	PMD_{24}	96	PMD_{47}	128	EV_{DD}

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
129	IV_{SS}	161	IV_{SS}	193	IV_{SS}	225	IV_{SS}
130	IV_{DD}	162	IV_{DD}	194	IV_{DD}	226	IV_{DD}
131	PMA_{19}	163	$\overline{IRQ_3}$	195	DMA_{15}	227	$\overline{DMS_2}$
132	PMA_{18}	164	$\overline{IRQ_2}$	196	EV_{SS}	228	$\overline{DMS_3}$
133	PMA_{17}	165	$\overline{IRQ_1}$	197	DMA_{16}	229	$\overline{DMD_{39}}$
134	PMA_{16}	166	$\overline{IRQ_0}$	198	DMA_{17}	230	$\overline{DMD_{38}}$
135	EV_{SS}	167	EV_{DD}	199	DMA_{18}	231	EV_{SS}
136	PMA_{15}	168	$FLAG_0$	200	DMA_{19}	232	$\overline{DMD_{37}}$
137	PMA_{14}	169	$FLAG_1$	201	EV_{DD}	233	$\overline{DMD_{36}}$
138	PMA_{13}	170	$FLAG_2$	202	DMA_{20}	234	$\overline{DMD_{35}}$
139	PMA_{12}	171	$FLAG_3$	203	DMA_{21}	235	$\overline{DMD_{34}}$
140	EV_{DD}	172	EV_{SS}	204	DMA_{22}	236	EV_{DD}
141	PMA_{11}	173	DMA_0	205	DMA_{23}	237	$\overline{DMD_{33}}$
142	PMA_{10}	174	DMA_1	206	EV_{SS}	238	$\overline{DMD_{32}}$
143	PMA_9	175	DMA_2	207	DMA_{24}	239	$\overline{DMD_{31}}$
144	PMA_8	176	DMA_3	208	DMA_{25}	240	$\overline{DMD_{30}}$
145	IV_{SS}	177	IV_{SS}	209	IV_{SS}	241	IV_{SS}
146	IV_{DD}	178	IV_{DD}	210	IV_{DD}	242	IV_{DD}
147	EV_{SS}	179	EV_{DD}	211	DMA_{26}	243	EV_{SS}
148	PMA_7	180	DMA_4	212	DMA_{27}	244	$\overline{DMD_{29}}$
149	PMA_6	181	DMA_5	213	EV_{DD}	245	$\overline{DMD_{28}}$
150	PMA_5	182	DMA_6	214	DMA_{28}	246	$\overline{DMD_{27}}$
151	PMA_4	183	DMA_7	215	DMA_{29}	247	$\overline{DMD_{26}}$
152	EV_{DD}	184	EV_{SS}	216	DMA_{30}	248	EV_{DD}
153	PMA_3	185	DMA_8	217	DMA_{31}	249	$\overline{DMD_{25}}$
154	PMA_2	186	DMA_9	218	EV_{SS}	250	$\overline{DMD_{24}}$
155	PMA_1	187	DMA_{10}	219	DMPAGE	251	$\overline{DMD_{23}}$
156	PMA_0	188	DMA_{11}	220	$\overline{BR}$	252	EV_{SS}
157	EV_{SS}	189	EV_{DD}	221	$\overline{BG}$	253	$\overline{DMD_{22}}$
158	TIMEXP	190	DMA_{12}	222	$\overline{DMS_0}$	254	$\overline{DMD_{21}}$
159	EV_{DD}	191	DMA_{13}	223	$\overline{DMS_1}$	255	$\overline{DMD_{20}}$
160	EV_{SS}	192	DMA_{14}	224	EV_{DD}	256	EV_{DD}

Pin Name (Note 1)	Type (Notes 2, 3)	Function
PMA_{23-0}	O	Progam Memory Address. The TSC21020F outputs an address in program memory on these pins.
PMD_{47-0}	I/O	Program Memory Data. The TSC21020F inputs and outputs data and instructions on these pins. 32-bit fixed-point data and 32-bit single-precision floating-point data is transferred over bits 47-16 of the PMD bus.
$\overline{PMS}_{1-0}$	O	Progam Memory Select lines. These pins are asserted as chip selects for the corresponding banks of program memory. Memory banks must be defined in the memory control registers. These pins are decoded program memory address lines and provide an early indication of a possible bus cycle.
$\overline{PMRD}$	O	Program Memory Read strobe. This pin is asserted when the TSC212020F reads from program memory.
$\overline{PMWR}$	O	Program Memory Write strobe. This pin is asserted when the TSC21020F writes to program memory.
PMACK	O	Program Memory Acknowledge. An external device asserts this input to add wait states to a memory access.
PMPAGE	O	Program Memory Page Boundary. The TSC21020F asserts this pin to signal that a program memory page boundary has been crossed. Memory pages must be defined in the memory control registers.
$\overline{PMTS}$	I/S	Program Memory Three-State Control. $\overline{PMTS}$ places the program memory address, data, selects, and strobes in a high-impedance state. If $\overline{PMTS}$ is asserted while a PM access is occurring, the processor will halt and the memory access will not be completed. PMACK must be asserted for at least one cycle when $\overline{PMTS}$ is asserted to allow any pending memory access to complete properly. $\overline{PMTS}$ should only be asserted (low) during an active memory access cycle.
DMA_{31-0}	O	Data Memory Address. The TSC21020F outputs an address in data memory on these pins.
$\overline{DMD}_{39-0}$	I/O	Data Memory Data. The TSC21020F inputs and outputs data on these pins. 32-bit fixed-point data and 32-bit single-precision floating-point data is transferred over bits 39-8 of the DMD bus.
$\overline{DMS}_{3-0}$	O	Data Memory Select lines. These pins are asserted as chip selects for the corresponding banks of data memory. Memory banks must be defined in the memory control registers. These pins are decoded data memory address lines and provide an early indication of a possible bus cycle.
$\overline{DMRD}$	O	Data Memory Read strobe. This pin is asserted when the TSC21020F reads from data memory.
$\overline{DMWR}$	O	Data Memory Write strobe. This pin is asserted when the TSC21020F writes to data memory.
DMACK	I/S	Data Memory Acknowledge. An external device de-asserts this input to add wait states to a memory access.

Pin Name (Note 1)	Type (Notes 2, 3)	Function
DMPAGE	O	Data Memory Page Boundary. The TSC21020F asserts this pin to signal that a data memory page boundary has beeen crossed. Memory pages must be defined in the memory control registers.
$\overline{\text{DMTS}}$	I/S	Data Memory Three-State Control. $\overline{\text{DMTS}}$ places the data memory address, data, selects and strobes in a high-impedance state. If $\overline{\text{DMTS}}$ is asserted while a DM access is occurring, the processor will halt and the memory access will not be completed. DMACK must be asserted for at least one cycle when $\overline{\text{DMTS}}$ is de-asserted to allow any pending memory access to complete properly. $\overline{\text{DMTS}}$ should only be asserted (low) during an active memory access cycle.
CLKIN	I	External clock input to the TSC21020F. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	Sets the TSC21020F to a known state and begins execution at the program memory location specified by the hardware reset vector (address). This input must be asserted (low) at power-up.
$\overline{\text{IRQ}}_{3\text{-}0}$	I/A	Interrupt request lines; may be either edge triggered or level sensitive.
$\text{FLAG}_{3\text{-}0}$	I/O/A	External Flags. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{\text{BR}}$	I/A	Bus Request. Used by an external device to request control of the memory interface. When $\overline{\text{BR}}$ is asserted, the processor halts execution after completion of the current cycle, places all memory data, addresses, selects and strobes in a high impedance state, and asserts $\overline{\text{BG}}$. The processor continues normal operation when $\overline{\text{BR}}$ is released.
$\overline{\text{BG}}$	O	Bus Grant. Acknowledges a bus request ($\overline{\text{BR}}$), indicating that the external device may take control of the memory interface. $\overline{\text{BG}}$ is asserted (held low) until $\overline{\text{BR}}$ is released.
TIMEXP	O	Timer Expired. Asserted for four cycles when the value of TCOUNT is decremented to zero.
RCOMP		Not available. Can be set to any voltage level.
EV_{DD}	P	Power Supply (for output drivers), nominally +5V DC (10 pins).
EV_{SS}	G	Power Supply return (for output drivers); 16 pins.
IV_{DD}	P	Power Supply (for internal circuitry); nominally +5V DC (4 pins).
IV_{SS}	G	Power Supply return (for internal circuitry); (7 pins).
TCK	I	Test Clock. Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select. Used to control the test state machine. TMS has a 20kΩ internal pull-up resistor.

Pin Name (Note 1)	Type (Notes 2, 3)	Function
TDI	I/S	Test Data Input. Provides serial data for the boundary scan logic. TDI has a 20kΩ internal pull-up resistor.
TDO	O	Test Data Output. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test Reset. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the TSC21020F. TRST has a 20kΩ internal pull-up resistor.
NC	-	No Connect. No Connects are reserved pins that must be left open and unconnected.

NOTES:
1. When groups of pins are identified with subscripts, e.g. PMD_{47-0}, the highest numbered pin is the MSB (in this case, PMD_{47}).
2. O = Output; I = Input; S = Synchronous; A = Asynchronous; P = Power Supply; G = Ground.
3. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI, and TRST). Those that are asynchronous (A) can be asserted asynchronously to CLKIN.

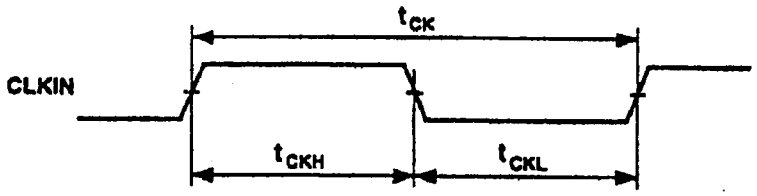
1.10 INSTRUCTION SET AND TIMING DIAGRAMS

The TSC21020F instruction set provides a wide variety of programming capabilites. Every instruction assembles into a single word and can execute in a single processor cycle. Multifunction instructions enable simultaneous multiplier and ALU operations, as well as computations executed in parallel with data transfers.

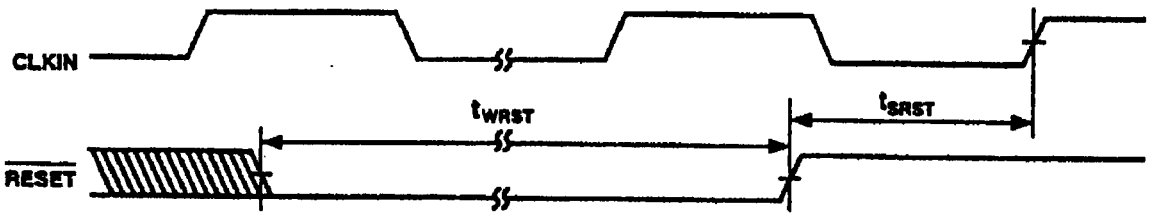
For complete information, see the ADSP-21020 User's Manual from Analog Devices.

The timing diagrams applicable to parameters specified in this specification are as follows:

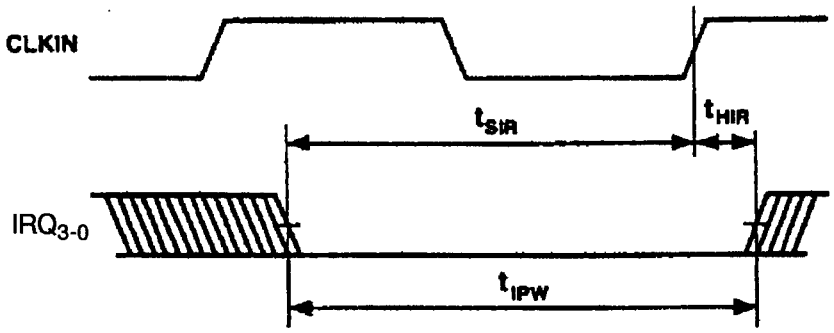
CLOCK TIMING



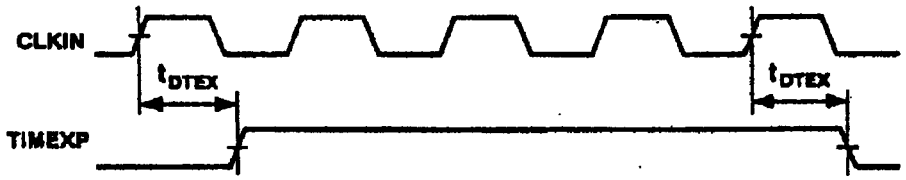
RESET TIMING



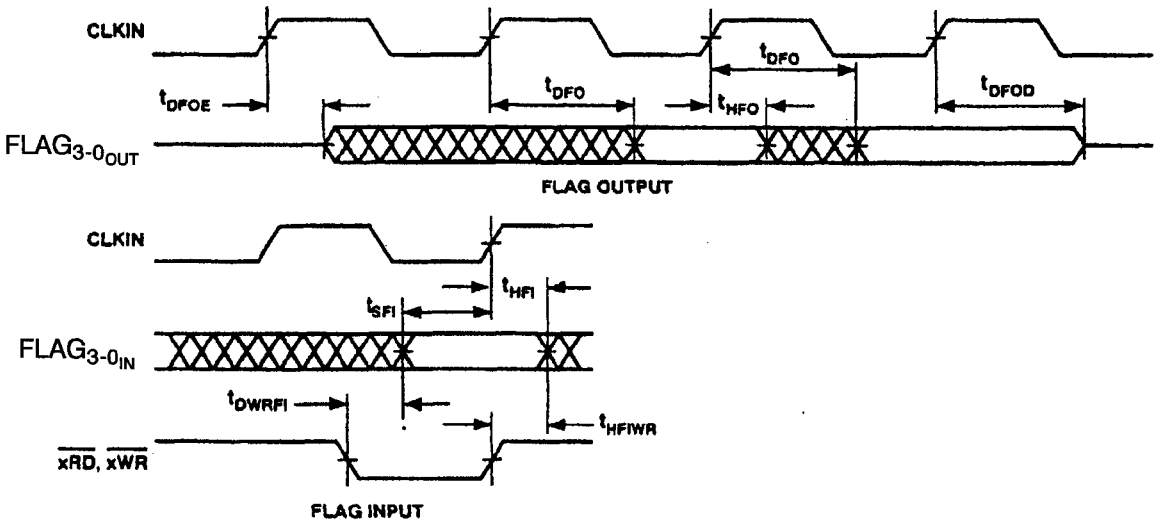
INTERRUPTS TIMING



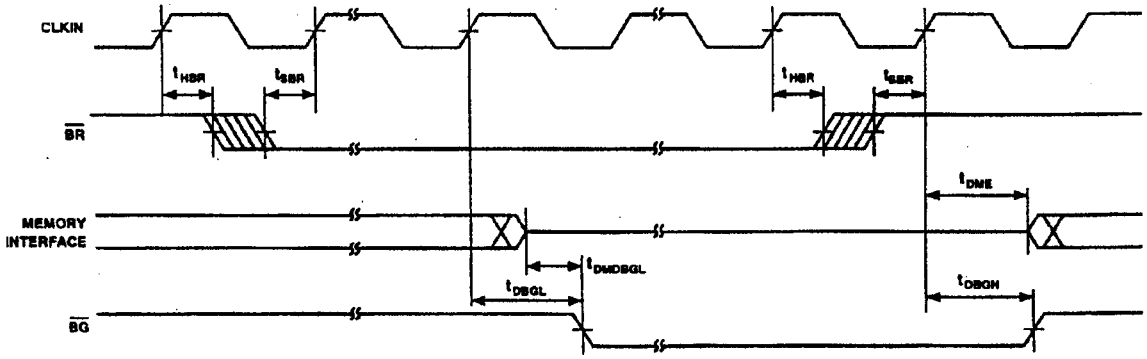
TIMER TIMING



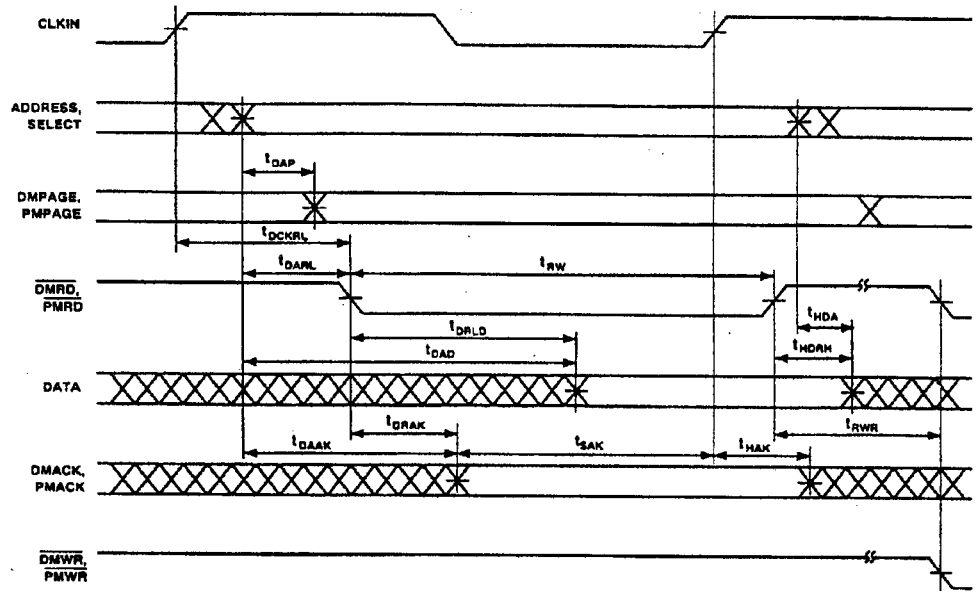
FLAGS TIMING



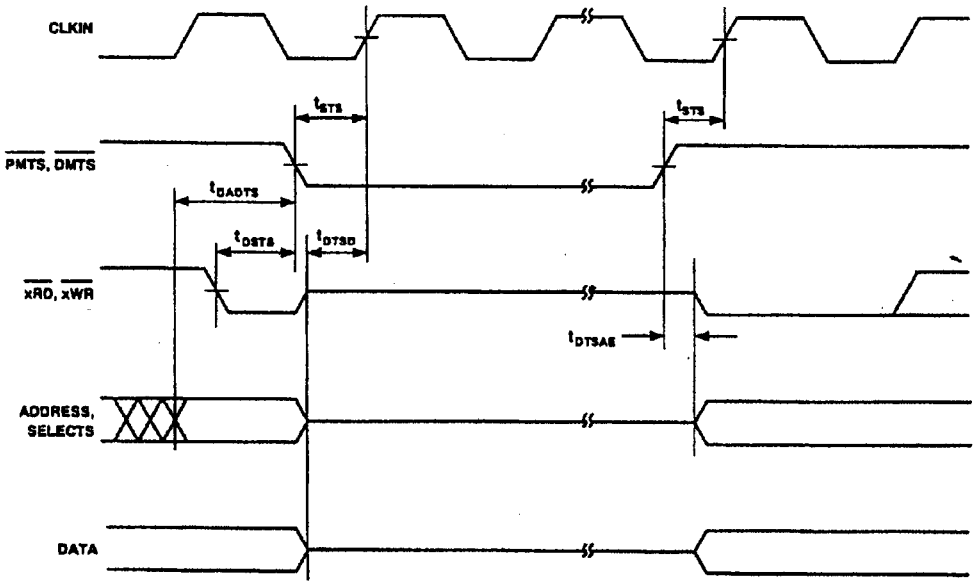
BUS REQUEST / BUS GRANT TIMING



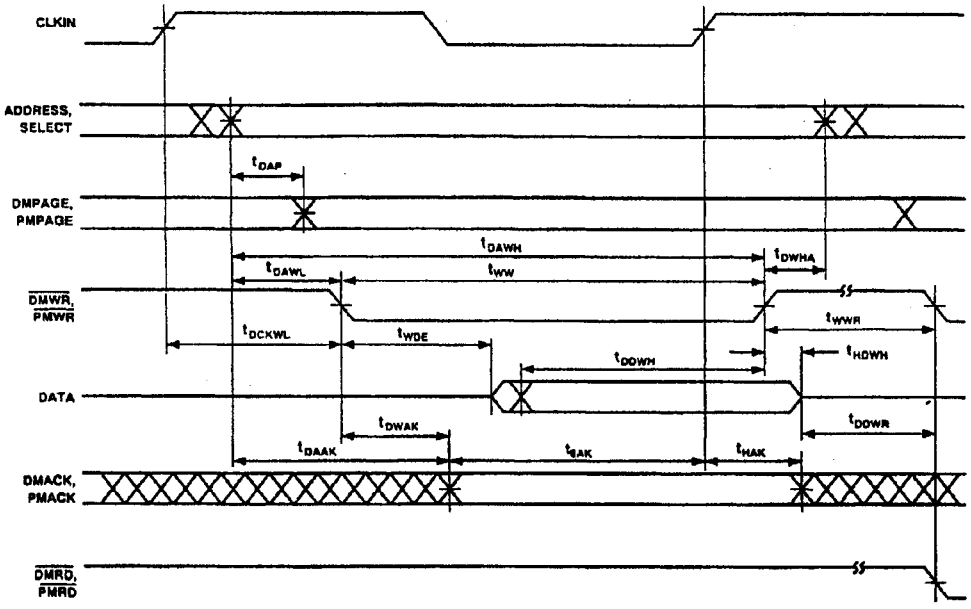
MEMORY READ TIMING



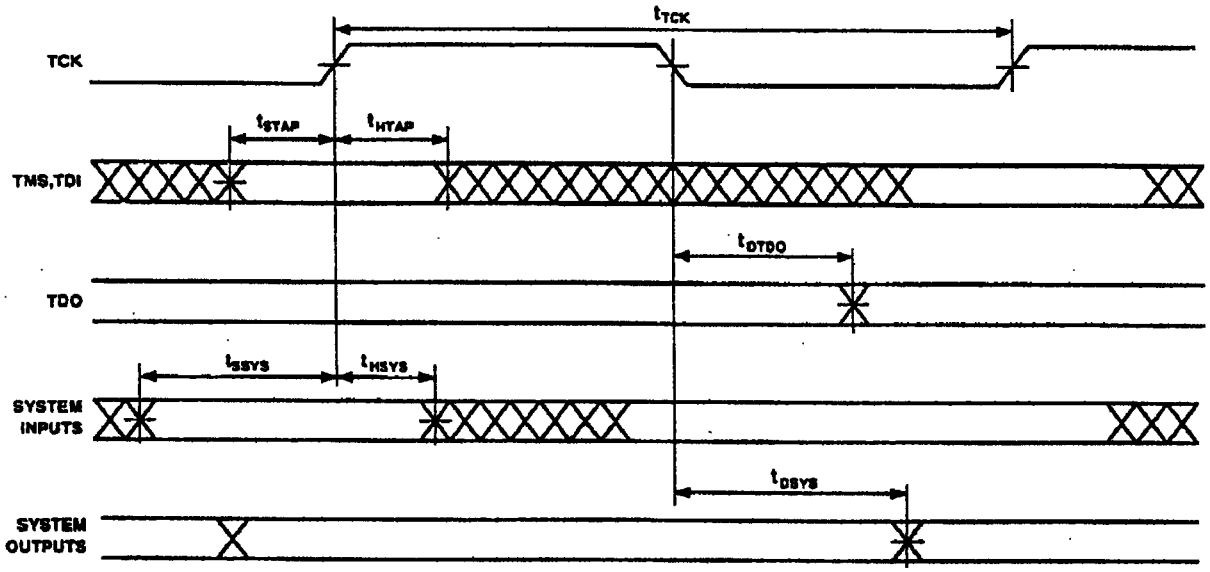
EXTERNAL MEMORY THREE-STATE CONTROL TIMING



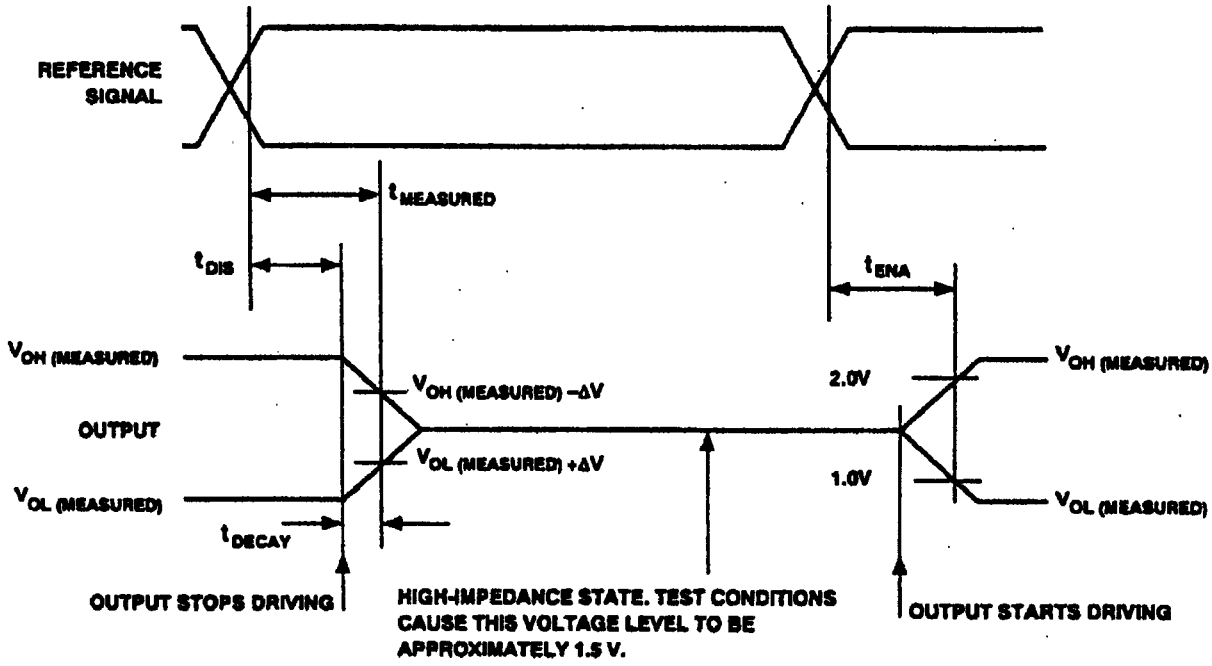
MEMORY WRITE TIMING



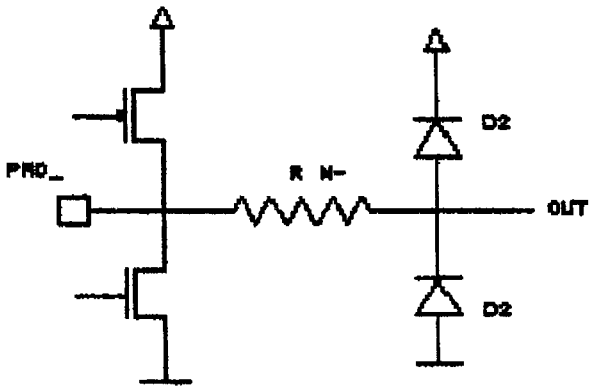
IEEE 1149.1 TEST ACCESS PORT TIMING



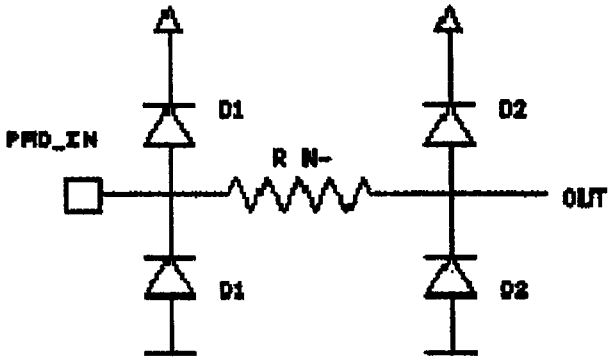
OUTPUT ENABLE / DISABLE TIMING



1.11 PROTECTION NETWORKS



Input/output and output pads



Input pads

2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the applicable ESCC Generic Specification. Permitted deviations from the applicable Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1 Basic Functional	-	-	Verify functionality V_{IL} = 0V, V_{IH} = 3V V_{DD} = 4.5V, 5V and 5.5V V_{SS} = 0V Note 2	-	-	-
Functional Test 2 Control Test	-	-	Verify functionality V_{IL} = 0V, V_{IH} = 3V V_{DD} = 4.5V, 5V and 5.5V V_{SS} = 0V Note 2	-	-	-
Functional Test 3 Complex Test	-	-	Verify functionality V_{IL} = 0V, V_{IH} = 3V V_{DD} = 4.5V, 5V and 5.5V V_{SS} = 0V Note 2	-	-	-
Functional Test 4 JTAG Test	-	-	Verify functionality V_{IL} = 0V, V_{IH} = 3V V_{DD} = 4.5V, 5V and 5.5V V_{SS} = 0V Note 2	-	-	-
Supply Current (Internal)	I_{DDIN}	3005	V_{IL} = V_{ILC} = 0.4V V_{IH} = 2.4V, V_{IHCR} = 3V t_{CK} = 50ns V_{DD} = 5.5V V_{SS} = 0V IV_{DD} Pins	-	430	mA
Supply Current (Idle)	I_{DDIDLE}	3005	V_{IN} = 0V or V_{DD} V_{DD} = 5.5V V_{SS} = 0V IV_{DD} Pins	-	150	mA
Low Level Input Current 1	I_{IL}	3009	V_{DD} = 5.5V V_{SS} = 0V V_{IN} = 0V Pins List 4 (Note 3)	-10	-	µA
Low Level Input Current 2	I_{ILT}	3009	V_{DD} = 5.5V V_{SS} = 0V V_{IN} = 0V Pins List 5 (Note 3)	-350	-	µA
High Level Input Current	I_{IH}	3010	V_{DD} = 5.5V V_{SS} = 0V V_{IN} = V_{DD} Pins Lists 4, 5 (Note 3)	-	10	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3020	V_{DD} = 5.5V V_{SS} = 0V V_{OUT} = 0V Pins List 6 (Note 3)	-10	-	µA
Output Leakage Current Third State (High Level Applied)	I_{OZH}	3021	V_{DD} = 5.5V V_{SS} = 0V V_{OUT} = V_{DD} Pins List 6 (Note 3)	-	10	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD} = 4.5V V_{SS} = 0V I_{OL} = 4mA Pins List 3 (Note 3)	-	400	mV
High Level Output Voltage	V_{OH}	3006	V_{DD} = 4.5V V_{SS} = 0V I_{OH} = -1mA Pins List 3 (Note 3)	2.4	-	V
Low Level Input Voltage 1	V_{IL}	-	V_{DD} = 4.5V V_{SS} = 0V Pins Lists 1 and 7 (Note 3) Note 4	-	800	mV
Low Level Input Voltage 2	V_{ILC}	-	V_{DD} = 4.5V V_{SS} = 0V Pins List 2 (Note 3) Note 4	-	600	mV
High Level Input Voltage 1	V_{IH}	-	V_{DD} = 5.5V V_{SS} = 0V I_{OL} = 4mA Pins List 1 (Note 3) Note 4	2	-	V
High Level Input Voltage 2	V_{IHCR}	-	V_{DD} = 5.5V V_{SS} = 0V Pins List 2 and 7 (Note 3) Note 4	3	-	V
Input Capacitance	C_{IN}	3012	V_{IN} (not under test) = 0V V_{DD} = V_{SS} = 0V f = 1MHz All signal pins Note 5	-	10	pF
CLKIN Period	t_{CK}	-	V_{DD} = 4.5V V_{SS} = 0V Clock Timing Note 6	50	150	ns
CLKIN Width High	t_{CKH}	-	V_{DD} = 4.5V V_{SS} = 0V Clock Timing Note 6	10	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
CLKIN Width Low	t_{CKL}	-	V_{DD} = 4.5V V_{SS} = 0V Clock Timing Note 6	10	-	ns
$\overline{\text{RESET}}$ Width Low	t_{WRST}	-	V_{DD} = 4.5V V_{SS} = 0V Reset Timing Note 6	200	-	ns
$\overline{\text{RESET}}$ Setup before CLKIN High	t_{SRST}	-	V_{DD} = 4.5V V_{SS} = 0V Reset Timing Note 6	29	50	ns
$\overline{IRQ_{3-0}}$ Setup before CLKIN High	t_{SIR}	-	V_{DD} = 4.5V V_{SS} = 0V Interrupts Timing Note 6	38	-	ns
$\overline{IRQ_{3-0}}$ Hold after CLKIN High	t_{HIR}	-	V_{DD} = 4.5V V_{SS} = 0V Interrupts Timing Note 6	0	-	ns
$\overline{IRQ_{3-0}}$ Pulse Width	t_{IPW}	-	V_{DD} = 4.5V V_{SS} = 0V Interrupts Timing Note 6	55	-	ns
CLKIN High to TIMEXP	t_{DTEX}	-	V_{DD} = 4.5V V_{SS} = 0V Timer Timing Note 6	-	24	ns
$FLAG_{3-0IN}$ Setup before CLKIN High	t_{SFI}	-	V_{DD} = 4.5V V_{SS} = 0V Flags Timing Note 6	19	-	ns
$FLAG_{3-0IN}$ Setup after CLKIN High	t_{HFI}	-	V_{DD} = 4.5V V_{SS} = 0V Flags Timing Note 6	0	-	ns
$\overline{FLAG_{3-0IN}}$ Delay from $\overline{xRD}$, $\overline{xWR}$ Low	t_{DWRFI}	-	V_{DD} = 4.5V V_{SS} = 0V Flags Timing Note 6	-	12	ns
$\overline{FLAG_{3-0IN}}$ Delay from $\overline{xRD}$, $\overline{xWR}$ Deasserted	t_{HFIWR}	-	V_{DD} = 4.5V V_{SS} = 0V Flags Timing Note 6	0	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
$FLAG_{3-0OUT}$ Delay from CLKIN High	t_{DFO}	-	V_{DD} = 4.5V V_{SS} = 0 Flags Timing Note 6	-	24	ns
$FLAG_{3-0OUT}$ Hold after CLKIN High	t_{HFO}	-	V_{DD} = 4.5V V_{SS} = 0 Flags Timing Note 6	5	-	ns
CLKIN High to $FLAG_{3-0OUT}$ Enable	t_{DFOE}	-	V_{DD} = 4.5V V_{SS} = 0 Flags Timing Note 5	1	-	ns
CLKIN High to $FLAG_{3-0OUT}$ Disable	t_{DFOD}	-	V_{DD} = 4.5V V_{SS} = 0 Flags Timing Note 6	-	24	ns
$\overline{BR}$ Hold after CLKIN High	t_{HBR}	-	V_{DD} = 4.5V V_{SS} = 0V Bus Request/Bus Grant Timing Note 6	0	-	ns
$\overline{BR}$ Setup before CLKIN High	t_{SBR}	-	V_{DD} = 4.5V V_{SS} = 0V Bus Request/Bus Grant Timing Note 6	18	-	ns
Memory Interface Disable to $\overline{BG}$ Low	t_{DMDBGL}	-	V_{DD} = 4.5V V_{SS} = 0V Bus Request/Bus Grant Timing Note 5	-2	-	ns
CLKIN High to Memory Interface Enable	t_{DME}	-	V_{DD} = 4.5V V_{SS} = 0V Bus Request/Bus Grant Timing Note 6	25	-	ns
CLKIN High to $\overline{BG}$ Low	t_{DBGL}	-	V_{DD} = 4.5V V_{SS} = 0V Bus Request/Bus Grant Timing Note 6	-	22	ns
CLKIN High to $\overline{BG}$ High	t_{DBGH}	-	V_{DD} = 4.5V V_{SS} = 0V Bus Request/Bus Grant Timing Note 6	-	22	ns
$\overline{xTS}$ Setup before CLKIN High	t_{STS}	-	V_{DD} = 4.5V V_{SS} = 0V External Memory Three-State Control Timing Note 6	14	50	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
$\overline{xTS}$, Delay after Address, Select	t_{DADTS}	-	V_{DD} = 4.5V V_{SS} = 0V External Memory Three-State Control Timing Note 6	-	28	ns
$\overline{xTS}$, Delay after $\overline{xRD}$, xWR Low	t_{DSTS}	-	V_{DD} = 4.5V V_{SS} = 0V External Memory Three-State Control Timing Note 6	-	16	ns
Memory Interface Disable before CLKIN High	t_{DTSD}	-	V_{DD} = 4.5V V_{SS} = 0V External Memory Three-State Control Timing Note 6	0	-	ns
$\overline{xTS}$ High to Address, Select Enable	t_{DTSAE}	-	V_{DD} = 4.5V V_{SS} = 0V External Memory Three-State Control Timing Note 6	0	-	ns
Address, Select to Data Valid	t_{DAD}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	-	37	ns
$\overline{xRD}$ Low to Data Valid	t_{DRLD}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	-	24	ns
Data Hold from Address, Select	t_{HDA}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	0	-	ns
Data Hold from $\overline{xRD}$ High	t_{HDRH}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	-1	-	ns
xACK Delay from Address	t_{DAAK}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	-	27	ns
xACK Delay from $\overline{xRD}$ Low	t_{DRAK}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	-	15	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
xACK Setup before CLKIN High	t_{SAK}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	14	-	ns
xACK Hold after CLKIN High	t_{HAK}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	0	-	ns
Address, Select to $\overline{xRD}$ Low	t_{DARL}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	8	-	ns
xPAGE Delay from Address, Select	t_{DAP}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	-	1	ns
CLKIN High to $\overline{xRD}$ Low	t_{DCKRL}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	16	26	ns
$\overline{xRD}$ Pulse Width	t_{RW}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	26	-	ns
$\overline{xRD}$ High to $\overline{xRD}$, $\overline{xWR}$ Low	t_{RWR}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Read Timing Note 6	17	-	ns
xACK Delay from $\overline{xWR}$ Low	t_{DWAK}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	-	15	ns
Address, Select to $\overline{xWR}$ Deasserted	t_{DAWH}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	37	-	ns
Address, Select to $\overline{xWR}$ Low	t_{DAWL}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	11	-	ns
$\overline{xWR}$ Pulse Width	t_{WW}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	26	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Data Setup before xWR High	t_{DDWH}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	23	-	ns
Address, Select Hold after xWR Deasserted	t_{DWHA}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	1	-	ns
Data Hold after xWR Deasserted	t_{HDWH}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 5	0	-	ns
CLKIN High to xWR Low	t_{DCKWL}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	16	26	ns
xWR High to xWR or xRD Low	t_{WWR}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	17	-	ns
Data Disable before xWR or xRD Low	t_{DDWR}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	13	-	ns
xWR Low to Data Enabled	t_{WDE}	-	V_{DD} = 4.5V V_{SS} = 0V Memory Write Timing Note 6	0	-	ns
TCK Period	t_{TCK}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	50	-	ns
TDI, TSM Setup before TCK High	t_{STAP}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	5	-	ns
TDI, TSM Hold after TCK High	t_{HTAP}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	6	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
System Inputs Setup before TCK High	t_{SSYS}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	7	-	ns
System Inputs Hold after TCK High	t_{HSYS}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	9	-	ns
$\overline{TRST}$ Pulse Width	t_{TRSTW}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	200	-	ns
TDO Delay from TCK Low	t_{DTDO}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	-	15	ns
System Outputs Delay from TCK Low	t_{DSYS}	-	V_{DD} = 4.5V V_{SS} = 0V IEEE 1149.1 Test Access Port Timing Note 6	-	26	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Functional tests shall be performed at each supply voltage with f_{CK} = 20MHz, $t_r = t_f \leq 5$ns, Duty cycle 50%, with timings per specified limits and $V_{OL} \leq 1.45$V, $V_{OH} \geq 1.55$V. Unless otherwise specified, all timings per the timing diagrams specified herein shall be verified.
3. The pins to be tested for the given characteristic are per the following lists:
   (1) PMD_{47-0}, PMACK, $\overline{PMTS}$, $\overline{DMD}_{39-0}$, DMACK, $\overline{DMTS}$, $\overline{IRQ}_{3-0}$, $FLAG_{3-0}$, $\overline{BR}$, TMS, TDI.
   (2) CLKIN, TCK.
   (3) PMA_{23-0}, PDM_{47-0}, $\overline{PMS}_{1-0}$, $\overline{PMRD}$, $\overline{PMWR}$, PMPAGE, DMA_{31-0}, $\overline{DMD}_{39-0}$, $\overline{DMS}_{3-0}$, $\overline{DMRD}$, $\overline{DMWR}$, DMPAGE, $FLAG_{3-0}$, TIMEXP, $\overline{BG}$.
   (4) PMACK, $\overline{PMTS}$, DMACK, $\overline{DMTS}$, $\overline{IRQ}_{3-0}$, $\overline{BR}$, CLKIN, $\overline{RESET}$, TCK.
   (5) TMS, TDI, $\overline{TRST}$.
   (6) PMA_{23-0}, PDM_{47-0}, $\overline{PMS}_{1-0}$, $\overline{PMRD}$, $\overline{PMWR}$, PMPAGE, DMA_{31-0}, $\overline{DMD}_{39-0}$, $\overline{DMRD}$, $\overline{DMWR}$, DMPAGE, $FLAG_{3-0}$, TDO.
   (7) $\overline{RESET}$, $\overline{TRST}$

4. Tested go-no-go during functional tests.
5. Guaranteed but not tested.
6. Timing characteristics are tested go-no-go during functional tests.

x = PM or DM.
Address = PMA_{23-0}, DMA_{31-0}
Data = PMD_{47-0}, DMD_{39-0}
Select = PMS_{1-0}, DMS_{3-0}.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current (Internal)	I_{DDIN}	±43	-	430	mA
Supply Current (Idle)	I_{DDIDLE}	±15	-	150	mA
Low Level Input Current 1	I_{IL}	±1	-10	-	µA
High Level Input Current	I_{IH}	±1	-	10	µA
Output Leakage Current Third State (Low Level Applied)	I_{OZL}	±1	-10	-	µA
Output Leakage Current Third State (High Level Applied)	I_{OZH}	±1	-	10	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0, -3)	°C
Inputs PMD_0 to PMD_{47}	V_{IN}	V_{DD}, V_{SS} per Note 1	V
Input CLKIN	V_{IN}	V_{GEN1} (Note 2)	V
Input $\overline{RESET}$	V_{IN}	V_{GEN2} (Note 2)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD} (Note 3)	V
Pulse Voltage	V_{GEN1}, V_{GEN2}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	1.6M 50 50±15% Duty Cycle $t_r = t_f \leq 5ns$	Hz
Positive Supply Voltage IV_{DD}, EV_{DD}	V_{DD}	5 (+0.5, -0)	V
Negative Supply Voltage IV_{SS}, EV_{SS}	V_{SS}	0	V

NOTES:

1. The 48-bit (PMD_0 to PMD_{47}) input instruction code shall be configured as follows. Each input shall be connected through a 4.7kΩ ±10% protection resistor.

Input	Condition	Input	Condition	Input	Condition	Input	Condition
PMD_0	V_{SS}	PMD_{12}	V_{SS}	PMD_{24}	V_{SS}	PMD_{36}	V_{DD}
PMD_1	V_{SS}	PMD_{13}	V_{DD}	PMD_{25}	V_{SS}	PMD_{37}	V_{DD}
PMD_2	V_{SS}	PMD_{14}	V_{DD}	PMD_{26}	V_{DD}	PMD_{38}	V_{SS}
PMD_3	V_{SS}	PMD_{15}	V_{DD}	PMD_{27}	V_{DD}	PMD_{39}	V_{SS}
PMD_4	V_{SS}	PMD_{16}	V_{SS}	PMD_{28}	V_{DD}	PMD_{40}	V_{SS}
PMD_5	V_{DD}	PMD_{17}	V_{SS}	PMD_{29}	V_{DD}	PMD_{41}	V_{SS}
PMD_6	V_{SS}	PMD_{18}	V_{SS}	PMD_{30}	V_{DD}	PMD_{42}	V_{SS}
PMD_7	V_{SS}	PMD_{19}	V_{DD}	PMD_{31}	V_{DD}	PMD_{43}	V_{SS}
PMD_8	V_{SS}	PMD_{20}	V_{DD}	PMD_{32}	V_{DD}	PMD_{44}	V_{DD}
PMD_9	V_{SS}	PMD_{21}	V_{SS}	PMD_{33}	V_{DD}	PMD_{45}	V_{DD}
PMD_{10}	V_{DD}	PMD_{22}	V_{DD}	PMD_{34}	V_{SS}	PMD_{46}	V_{SS}
PMD_{11}	V_{DD}	PMD_{23}	V_{DD}	PMD_{35}	V_{DD}	PMD_{47}	V_{SS}

2. CLKIN and RESET shall each be connected through a 1kΩ ±10% protection resistor.
3. All other inputs and outputs shall be connected through a 10kΩ ±10% protection resistor/load.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the purchase order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ±3	°C
Inputs PMD_0 to PMD_{47}	V_{IN}	V_{SS} (Note 1)	V
Input CLKIN	V_{IN}	V_{GEN}	V
Input $\overline{RESET}$	V_{IN}	V_{DD} (Note 1, 2)	V
All other Inputs and Outputs	V_{IN}, V_{OUT}	V_{DD} (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	7M 50±15% Duty Cycle $t_r = t_f \leq 5$ns	Hz
Positive Supply Voltage IV_{DD}, EV_{DD}	V_{DD}	5 (+0.5, -0)	V
Negative Supply Voltage IV_{SS}, EV_{SS}	V_{SS}	0	V

NOTES:

1. Input protection resistor = Output load = 4.7kΩ ±10%.
2. $\overline{RESET}$ is pulsed low (V_{SS}) for at least 200ns at power up then held at V_{DD}.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Characteristics	Symbols	Limits		Units
		Min	Max	
Supply Current (Internal)	I_{DDIN}	-	450	mA
Supply Current (Idle)	I_{DDIDLE}	-	150	mA
Low Level Input Current 1	I_{IL}	-10	-	µA
Low Level Input Current 2	I_{ILT}	-350	-	µA
High Level Input Current	I_{IH}	-	10	µA
Output Leakage Current Third State (Low Level Applied)	I_{OZL}	-10	-	µA
Output Leakage Current Third State (High Level Applied)	I_{OZH}	-	10	µA
Low Level Output Voltage	V_{OL}	-	400	mV
High Level Output Voltage	V_{OH}	2.4	-	V