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ESCC QUALIFIED MANUFACTURERS LIST

REP006

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
478	Specification updated to incorporate new Technology Flow entry per DCR.

FOREWORD

This document contains a list of qualified manufacturers that have been certified by the European Space Agency for Technology Flows to the rules of the ESCC System with principle reference to ESCC Basic Specification No. 25400.

The qualified electronic components produced from the Technology Flows are intended for use in ESA and other spacecraft and associated equipment in accordance with the requirements of the ECSS Standard ECSS-Q-60.

Each Technology Flow qualification and its subsequent maintenance is monitored and overseen by the ESCC Executive. ESA certifies the qualification upon receipt of a formal application from the Executive stating that all applicable ESCC requirements have been met by the pertinent manufacturer. The qualified status of a Technology Flow is noted by an entry in this document, a corresponding entry in the European Space Components Information Exchange System, ESCIES, and the issue of a certificate to the qualified manufacturer.

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1. PROMOTION

It is permitted to advertise the ESCC qualification status of a component provided such publicity or advertisement does not state or imply that the component is the only qualified one of that particular type, range or family.

2. PROCURER'S RESPONSIBILITY

When procuring ESCC qualified components, the procurer is responsible for ensuring that the qualification status is valid and that delivered components fulfil the specified requirements of the applicable ESCC specifications. The procurer is advised to utilise the ESCC non-conformance system, per ESCC Basic Specification No. 22800, in the event that a qualified manufacturer delivers non-conforming components.

3. QML ORGANISATION

3.1 TECHNOLOGY FLOWS

The individual Technology Flows are listed in this document by manufacturer in alphabetical order. They may also be found on the ESCIES web site, https://escies.org.

The controlling ESCC specifications are identified and a Technology Flow Abstract is provided to describe the main features of the qualified Technology Flow.

3.2 QUALIFIED COMPONENTS

Under each technology flow a list of the qualified components is provided. As new components are specified in an ESCC Detail Specification and are produced within the Technology Flow the list will be updated accordingly.

3.3 TYPE DESIGNATION

Wherever possible the referenced type (style) designations are derived from industrial standards (i.e., JEDEC, PRO-ELECTRON, MIL, IEC and CECC). The purpose is to identify the similarity of a listed qualified component, to a standard type designation. Where no standardised type designation is applicable the manufacturer's designation is referenced.

3.4 COMPONENT CHARACTERISTICS

The electrical characteristics described in the Technology Flow Abstract are provided for guidance only and, unless otherwise stated, are specified at +25^{o}C. The precise characteristics of the qualified component are defined in the referenced ESCC specifications.

3.5 MANUFACTURER

Contact information and plant locations are indicated in the individual Technology Flow listings. Contact information may also be found in the ESCC QML section of the ESCIES web site, https://escies.org.

4. REVISION PROCEDURE

Amendments to earlier issues of the ESCC QML, implemented herein, are indicated by the issue date and by the content of the relevant "Document Change Request".

5. QUALIFIED TECHNOLOGY FLOWS

The following Technology Flows are qualified:

5.1 ATMEL

Contact Information

Address	ESCC Chief Inspector
Atmel Nantes BP 70602 44306 Nantes Cedex 3 France	Mr C. Ferré Tel. +33 24 01 81 913 FAX +33 24 01 81 946

Initial Qualification

Qualification Certificate No.	Validity Dates	Type Designation
278	Dec. 2006 - Dec. 2008	Integrated Circuits, Silicon Monolithic, CMOS Gate/ Embedded Array based on type MH1RT

Maintenance of Qualification

Qualification Certificate No.	Validity Dates	Comment

Applicable Documents

ESCC Generic Specification No. 9000

ESCC Detail Specification No. 9202/076

Atmel Process Identification Document PID 0026

List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/076. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document. Availability of the ASIC sheet is indicated in the table by an * in the final column.

ASIC Sheet	Component Type	ESCIES
FPK	Integrated Motor Controller for Mechanisms	*

Technology Flow Abstract

1. Technology Flow
   The MH1RT gate array family is designed with a 0.35µm radiation tolerant CMOS technology. The offering is based on a 4 metal layer 3.3volts AT56KRT process.

   The family features arrays with up to 1.6 million routeable gates and 596 pads. The MH1RT is suitable for high speed, low power digital applications working in a radiation intensive environment.

   The Technology Flow covers the foundry design, fabrication, assembly and testing of the MH1RT Sea of Gates family.

	Scope	Site
Design Centre	Array Sizes: - 99K - 156K - 242K - 332K - 3V and 5V tolerant/compliant	Atmel Nantes BP 70602 44306 Nantes Cedex 3 France
Wafer Fabrication	Process Flow: AT56KLRT	Atmel Rousset Zone Industrielle 131106 Rousset Cedex France
Assembly	Packages: - Multilayer Quad Flat Pack 196, 256, 352 pins - Multilayer Column Grid Array 349, 472 pins	E2V Grenoble BP 123 38521 Saint-Egrève Cedex France

	Scope	Site
Test	Lot Formation Wafer Acceptance Inspection - SEM - Wafer Lot Acceptance In-process Inspection Test Testing Flow Sampling Plans Test Procedures - Test Vector Generation - Test Program Validation Customer Source Inspection Qualification Testing Lot Acceptance Support Qualification Test Plan/Report Technology Characterization Reliability Monitoring	Atmel Nantes BP 70602 44306 Nantes Cedex 3 France
	Incoming Inspection Final Test - Credence, Type Octet Screening External Visual Inspection	MHS Nantes 92, route de Gachet La Chantrerie BP60601 44306 Nantes Cedex 3

(a) Basic Information

– 0.35µm CMOS technology AT56KRT Process.
– High Speed Performance
  • 170 ps typical gate delay (NAND, fanout 2) @ 3V
  • 800 MHz typical toggle frequency @ 3.3V

– Triple Supply Operation
  • 3.3, 3 and 2.55 V operation
  • 5V compliant
  • 5V tolerant

– Low Supply Current
  • Operating Maximum Value
    0.32 µW/gate/MHz @ 2.5V,
    0.54 µW/gate/MHz @ 3V,
    0.69 µW/gate/MHz @ 3.3V
  • Maximum Stand-by Value
    4nA/gate@ 2.5V
    5nA/gate@ 3 and 3.3V

– 472 pins maximum (MCGA 472 package)
– I/O Interface
  • CMOS, LVTTL, LVDDS, PCI, USB
  • Output Currents Programmable from 2 to 24 mA, by Steps of 2 mA
  • Cold Sparing Buffers (2µA maximum leakage current at 3.6V and 125^{o}C)

– Radiation
  - qualified to 1000 Gy(Si) letter R per ESCC Basic Specification No. 22900, tested successfully to 2000 Gy(Si)
  - No Single Event Latch-up below a LET Threshold of 70 MeV/mg/cm^2
  - SEU Hardened Flip-flops

– Four Arrays and Four Composite Arrays
  - Device Types
    Refer to ESCC Detail Specification No. 9202/076

(b) Component Types
This table presents the available couples (array, package) as defined in the Variants table in the Detail Specification.

Array Designation	TH1099E TH1M099E	TH1156E TH1M156E	TH1242E TH1M242E	TH1332E TH1M332E
Array size	99K	156K	242K	332K
Package				
MQFP-T352	X	X	X	X
MQFP-F256	X	X	X	
MQFP-F196	X			
MCGA 472		X	X	X
MCGA 349	X	X	X	

2. Design
The design manual and the ASIC library data books cover design at the Atmel Nantes Design Centre.
– MH1RT Design Manual ATD-TS-LR-R0232
– MH1RT 2V5 ASIC Library Data book ATD-TS-LR-R0236
– MH1RT 3V ASIC Library Data book ATD-TS-LR-R0235
– MH1RT 3V3 ASIC Library Data book ATD-TS-LR-R0238

ASIC designs are performed by the Atmel customer at their own site, with Atmel supported tools (front end) provided as a design tool kit.

3. Fabrication
The AT56KRT Radiation Tolerant process at Atmel Rousset is a 0.35µm CMOS, 4 metal, Ti, TiN and AlCu process.

4. Assembly
Atmel Nantes assembles the MH1RT devices at E2V Grenoble.
This Technology Flow covers the following capabilities.

Package	Die Attach	Wire Bond	Lid Seal	Leads
MQFP	Silver Glass (QMI2569)	Ultrasonic Wedge, 32 µm Al	Brazed Sealed with Au/Sn Alloy	Au Plated
MCGA	MCGA Cyanate Ester (JM7600)	Ultrasonic Wedge, 32 µm Al	Brazed Sealed with Au/Sn Alloy	Sn/Pb

5. Test
TCVs and SEC
The TH1156E matrix is used for both test vehicles.
(a) Test Vehicle V37
The V37 is a buffer test vehicle representative of the range of buffers available for performance testing in the MQFP 256 package.
(b) Test Vehicle V38
The V38 is developed for performance and radiation testing in the MQFP 256 package. It tests the following library elements;
– LVDS input and output buffers
– PCI 3V and 5V output buffers
– PLL (125 MHz and 250 MHz)
– DPRAM memory cell for GENESYS tool

(c) SEC
The standard evaluation circuit for reliability testing is the 65609E.

6. Radiation Characteristics
The MH1RT family has been developed to fulfil the following characteristics in terms of radiation tolerance:
– Tested up to 2000 Gy(Si)
– No Single Event Latch-up below a LET Threshold of 70MeV/mg/cm^2
– Availability in the library of SEU hardened cells

The radiation capability of the MH1RT family has been tested during development and evaluated in total dose and for single event effects to confirm the stated characteristics. Lot radiation verification testing is performed if specified by the procurer's purchase order requirements.

5.2 VISHAY SFERNICE FRANCE

Contact Information

Address	ESCC Chief Inspector
Vishay S.A. Division Résistances de Très Haute Précision 199, Boulevard de la Madeleine B.P. 1159 06003 Nice Cedex 1 France	Mr. E. Quehen Tel: +33 4 93 37 27 27 FAX: +33 4 93 37 27 26 EMAIL: Erwan.Quehen@vishay.com

Initial Qualification

Qualification Certificate No.	Validity Dates	Type Designation
287	Feb. 2009 - Feb. 2011	Thin Film Technology for Chip, Wraparound, Single and Network Resistors, Fixed, Based on Types P for Single Chip, PRA and CNW for Resistor Networks

Maintenance of Qualification

Qualification Certificate No.	Validity Dates	Comment

Applicable Documents

ESCC Generic Specification No. 4001

ESCC Detail Specification Nos. 4001/023, 4001/025

Vishay Process Identification Document PID PID-TFD P PRA CNW

List of Qualified Components

Variant No. By Form Factor	Component Type	ESCC Detail Specification
01 and 05	P 0603 HR	4001/023 (1)
02 and 06	P 0805 HR	4001/023 (1)
03 and 07	P 1206 HR	4001/023 (1)
04 and 08	P 2010 HR	4001/023 (1)
01 to 07 and 22 to 28	PRA 100 HR	4001/025
08 to 14 and 29 to 35	PRA 135 HR	4001/025
15 to 21 and 36 to 42	PRA 182 HR	4001/025

NOTES:
1. Note that gold finish variants are not intended for de-golding and tinning.

Technology Flow Abstract

1. Technology Flow
   The thin film technology for chip, fixed, wraparound, single and network resistors are designed on types based on P for single chip, PRA for 2 to 8 resistors of similar value and CNW for 2 to 8 resistors with at least two different values with the same form factor as PRA.

Technology Flow	Scope	Site
Design Centre	Single resistor chips in 0605, 0805, 1206 and 2010 formats 2 to 8 resistors of similar value in formats 0603, 0805 and 1206 2 to 8 resistors with at least 2 different values with the same form factor, 0603, 0805 or 1206	Vishay S.A. Division Résistances de Très Haute Précision 199, Boulevard de la Madeleine B.P. 1159 06003 Nice Cedex 1 France
Fabrication	Film deposition Photolithography Thermal treatment Passivation Thermal stabilization and control	As above
Assembly	Laser trim Protective layer Termination and Test	As above
Test	Chart 2, 3 and 4 Periodic Testing	As above

(a) Basic Information
The technology consists of:
- Substrate: High purity alumina (99.5%)
- Resistive Layer: Nickel chromium
- Protection: Silicon Nitride

– Termination: Nickel barrier
– Processes: Thin film deposition
– Finish: SnPbAg or Au

Critical resistance by style:
– P 0603: 12.25 kΩ
– P 0805: 45 kΩ
– P 1206: 40 kΩ
– P 2010: 45 kΩ
– PRA 100: 12.25 kΩ
– PRA 135: 56.25 kkΩ
– PRA 182: 100 kΩ

(b) Component Types
The available formats are defined in the variants table in the Detail Specifications.

2. Design
The design manual covers the design rules and limits:
– HP-BE/001 (Maîtrise de la conception)
– HP-BE/004 (Données technologiques, Régles d'implementation, Performances)

Critical design characteristics:
– Minimum metal width: 10µm
– Power dissipation lower than 250mW/mm^2
– Current density lower than 7000 A/mm^2
– Electrical field lower than 5V/µm

3. Fabrication/Assembly
The manufacturing flows and procedures are described in section 4 of Vishay PID.

4. Test
Complete test sequence as detailed in ESCC Generic 4001 and the relevant Detail Specifications is conducted by Vishay Sfernice.

The deletion of the Third Harmonic Control requirement from ESCC Detail Specification No. 4001/023 for thin film wraparound technology is documented in reference report MAT/3HC/07.02 revision 3 dated 2007-06-20.

The efficiency of the Overload Test is increased with the implementation of a resistance change rejection criteria of 500 ppm and approved by TRB decisions on 2007-04-04

5. Radiation Characteristics
The resistors covered in this technology domain is considered insensitive to radiation effects.