INTEGRATED CIRCUITS, SILICON MONOLITHIC,

BIPOLAR OPERATIONAL AMPLIFIERS

BASED ON TYPE LM108A

ESCC Detail Specification No. 9101/005

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Pages 1 to 34

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BIPOLAR OPERATIONAL AMPLIFIERS

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ESA/SCC Detail Specification No. 9101/005

space components
coordination group

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		SCCG Chairman	ESA Director General or his Deputy
Issue 4	August 1983	-	-
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Revision 'D'	October 1994		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This issue supersedes Issue 3 and incorporates all modifications agreed on the basis of Policy DCR 21019 (Appendices to Detail Specification), DCR 23058 (new Table 2, 3(a), 3(b) and Figure 4 format) and the following DCR's:-		
		P1.	Cover Page : Page numbers changed	None
		P5.	Appendix 'A' : Added	24023
		P7.	Table 1(a) : Lead material and finish redefined	21025
		P14.	Para. 2 : MIL-STD-1276 deleted	21025
		P16.	Para. 4.4.2 : Lead material and finish redefined	21025
		P19.	Table 2 : Test 9, Limit changed to 0.6mA	23089
		P33.	Appendix 'A' : Added	24033
'A'	Sep. '84	P1.	Cover Page	None
		P2.	DCN	None
		P5.	Appendices : Appendix 'B' added	24038/35
		P7.	Table 1(b) : P_D rating changed	22291
			Notes to Table 1(b) : Note 3, 4 and 5 derating factors amended. Format amended	22291
		P8.	Figure 1 : Amended	22291
		P14.	Para. 4.2.2 : PIND testing added	22240
		P16.	Para. 4.4.2 : Rewritten	21025
		P20.	Table 2 : Test 16 and 17 Limits amended	23115
		P22.	Table 3(a) : Typographical deletion	23159
		P23.	Table 3(b) : Limits of Tests 10 and 11 amended	22232
			: Limits for Test 13 added	23159
		P34.	Appendices : New Appendix 'B' added	24038/35
'B'	Nov. '84	P1.	Cover page	None
		P2.	DCN	None
		P22.	Table 3(a) : Test No. 10 Note corrected	23197

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
'C'	Dec. '91	P1. Cover page		None
		P2A. DCN	: Page added	None
		P3. T of C	: Para. 4.3.3 deleted	None
		P7. Table 1(a)	: Variant 07 added	22914
		Table 1(b)	: No. 5, Characteristics amended to include Variant 07	22914
		P8. Figure 1	: Note 2 amended to include Variant 07	22914
		P14. Para. 4.2.2	: Deviation deleted, "None." added	21048
		P15. Para. 4.2.4	: Deviation deleted, "None." added	22919
		Para. 4.2.5	: Deviation deleted, "None." added	22919
		Para. 4.3.2	: Paragraph amended to include Variant 07	22914
		Para. 4.3.3	: Paragraph deleted	22921
		P16. Para. 4.4.2	: Paragraph amended	22914
		Para. 4.5.2	: Paragraph amended to include Variant 07	22914
'D'	Oct. '94	P1. Cover page		None
		P2A. DCN	: Page added	None
		P7. Table 1(a)	: Variant 08, "Chip Carrier" added	221110
		Table 1(b)	: Item 5, Variant 08 added	221110
		P8. Figure 1	: Note 1, Variant 08 added	221110
		P9. Figure 2(a)	: Imperial dimensions deleted, number of pins added to Title	221110
		P10. Figure 2(b)	: Imperial dimensions deleted, number of pins added to Title	221110
		P11. Figure 2(c)	: Imperial dimensions deleted, number of pins added to Title	221110
		P12. Figure 2(d)	: "Chip Carrier Package" added, old Page 12 renumbered "12A"	221110
		P12A. Figure 3(a)	: Renumbered from Page 12. "Chip Carrier Package" added	221110
		Figure 3(c)	: "Chip Carrier Package" added to Pin Configuration table	221110
		P15. Para. 4.3.2	: Variant 08 added	221110
		P16. Para. 4.4.2	: Variant 08 added and text rewritten	221110
		Para. 4.5.2	: Variant 08 added and text rewritten	221110
		P20. Table 2	: No. 20 and 21, Limit amended to 18V	221150
		P22. Table 3(a)	: No. 20 and 21, Limit amended to 18V	221150
		P23. Table 3(b)	: No. 20 and 21, Limit amended to 18V	221150
		This specification has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.		

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TABLES

FIGURES

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, bipolar operational amplifier, based on Type LM108A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

As per Figure 1.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE (FIGURE 3(b))

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	FLAT	2(a)	D2
02	FLAT	2(a)	D3 or D4
03	TO99	2(b)	D2
04	TO99	2(b)	D3 or D4
05	DIL	2(c)	D2
06	DIL	2(c)	D3 or D4
07	TO99	2(b)	D9
08	CHIP CARRIER	2(d)	2

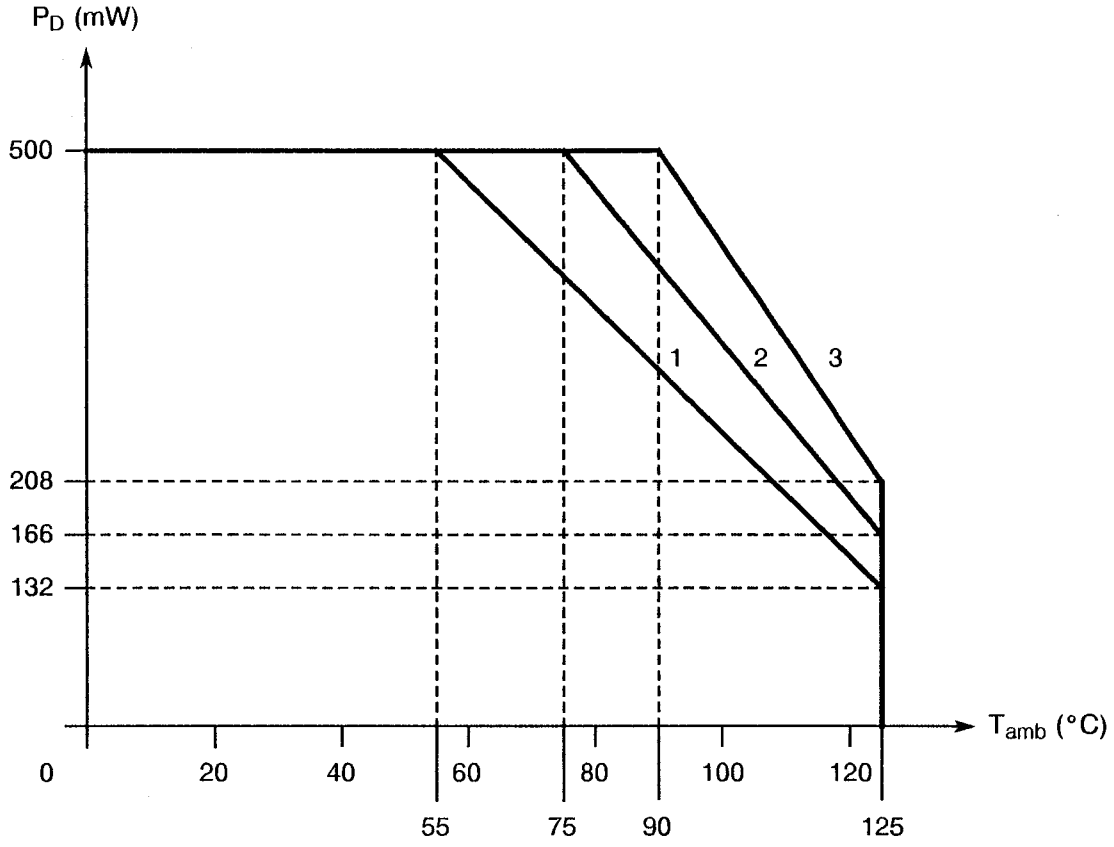
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V_S	±22	V	
2	Differential Input Voltage Range	V_{ID}	±30	V	Note 1
3	Input Voltage Range	V_I	±15	V	Note 2
4	Input Current Range	I_I	−0.1 to +10	mA	
5	Device Power Dissipation - Type Variants 01-02-08 - Type Variants 03-04-07 - Type Variants 05-06	P_D	500	mW	 Note 3 Note 4 Note 5
6	Output Short Circuit Duration	-	Indefinite	-	Note 6
7	Operating Temperature Range	T_{amb}	−55 to +125	°C	
8	Storage Temperature Range	T_{stg}	−55 to +150	°C	
9	Soldering Temperature	T_{sol}	+300	°C	Note 7
10	Junction Temperature	T_j	+150	°C	

NOTES

1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential voltage in excess of 1.0V is applied between the inputs, unless some limiting resistance is used.
2. If the supply voltage is less than +15V, the maximum input voltage is equal to the supply voltage.
3. Derate above T_{amb} = +55°C at 5.26mW/°C. See Figure 1.
4. Derate above T_{amb} = +75°C at 6.67mW/°C. See Figure 1.
5. Derate above T_{amb} = +90°C at 8.33mW/°C. See Figure 1.
6. Continuous short circuit is allowed for an ambient temperature of +70°C and a case temperature of +125°C.
7. Duration: ≤5 seconds.

FIGURE 1 - DEVICE DISSIPATION DERATING WITH TEMPERATURE

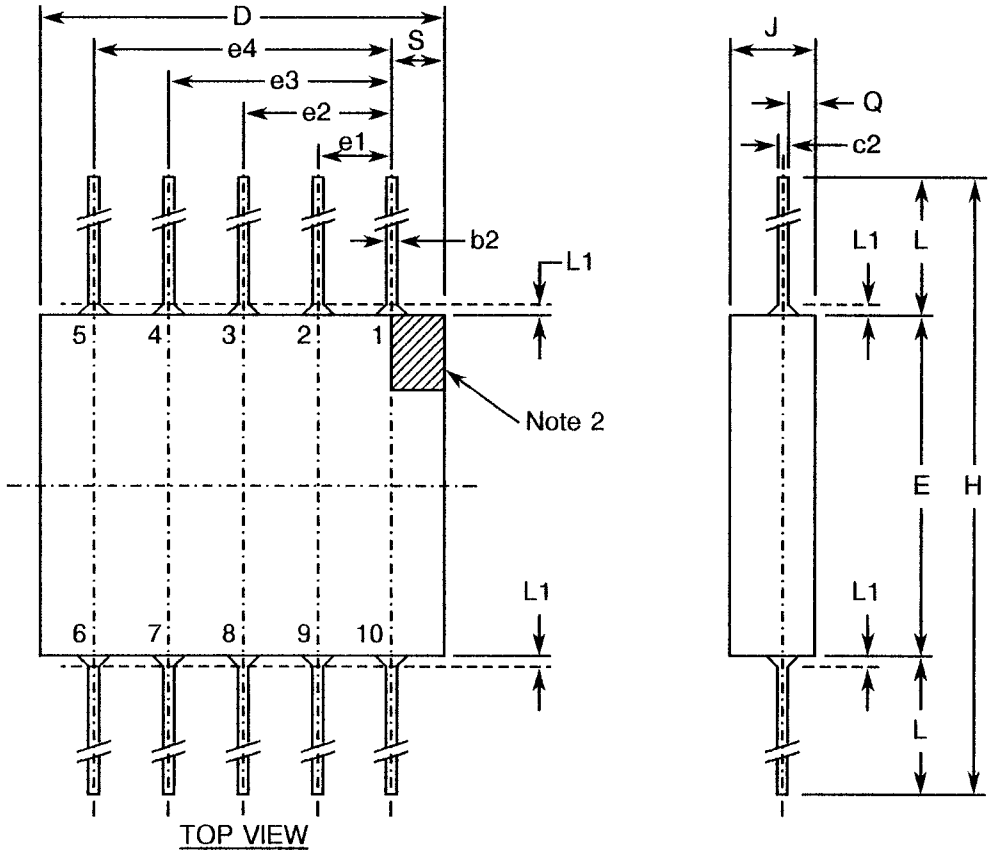


NOTES

1. Derating for type variants 01, 02 and 08.
2. Derating for type variants 03, 04 and 07.
3. Derating for type variants 05 and 06.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 10-PIN



The metric dimensions are calculated from the original dimensions in inches.

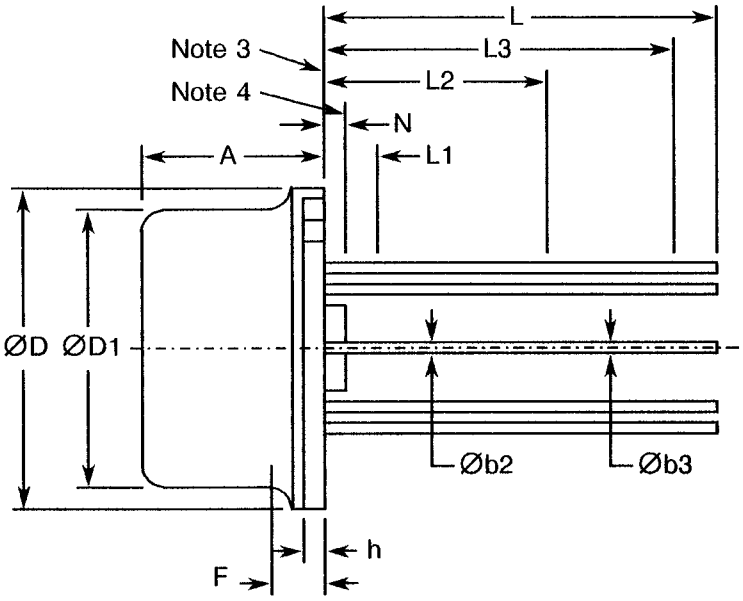
SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
b2	0.254	0.482	
c2	0.077	0.152	
D	6.10	6.98	
E	6.10	6.60	
e1	1.15	1.39	1
e2	2.42	2.66	1
e3	3.69	3.93	1
e4	4.96	5.20	1
H	13.72	19.81	
J	0.77	1.77	
L	3.81	6.60	
L1	-	0.38	
Q	0.13	0.83	
S	0.52	0.86	

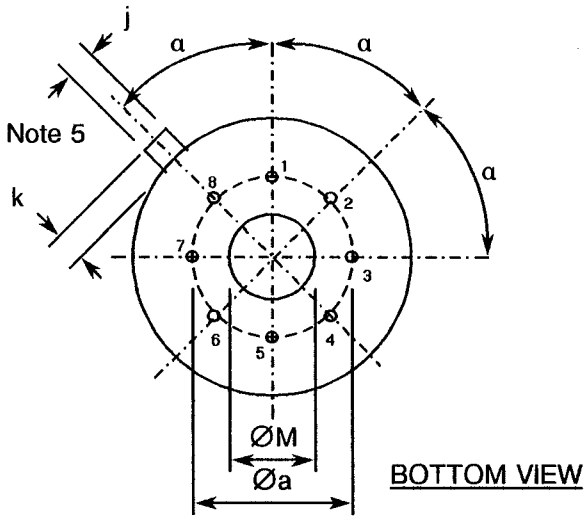
NOTES

1. The space between terminals has to be measured at a distance of 0.76mm maximum from where the terminals emerge from the case.
2. The top face and Pin No. 1 are marked.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - TO99 PACKAGE, 8-PIN





BOTTOM VIEW

SYMBOL	MILLIMETRES			DEGR. NOM.	NOTES
	MIN.	NOM.	MAX.		
Øa	-	5.08 (*)	-		1
A	4.20	-	4.69		
Øb2	0.407	-	0.508		
Øb3	-	-	0.53		
ØD	8.51	-	9.39		
ØD1	7.75	-	8.50		
F	-	-	1.27		
h	0.15	-	1.01		
j	0.712	-	0.863		
k	0.74	-	1.14		2
L	12.50	-	14.50		
L1	-	-	1.27		
L2	6.35	-	-		
L3	12.70	-	-		
ØM	3.56	-	4.06		
N	0.26	-	1.01		
α				45° (*)	1

NOTES

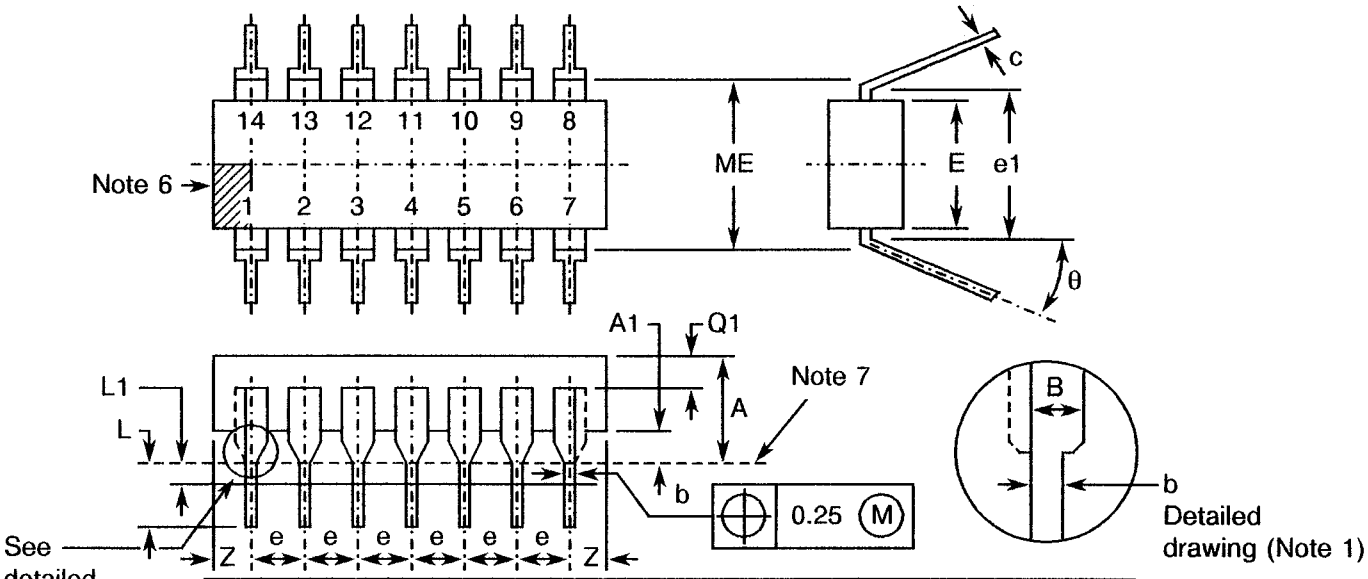
1. The section of each terminal, from a distance of 1.37mm to the reference plane, shall be located in a ring whose diameter is 0.99mm, centred on the accurate geometrical point defining the terminal axis.
2. Measured from the D diameter.
3. Reference plane.
4. Base plane.
5. Reference index of Pin 8.

* = accurate geometrical location.

The metric dimensions are calculated from the original dimensions in inches.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - DUAL-IN-LINE PACKAGE, 14-PIN



SYMBOL	MILLIMETRES			DEGREES		NOTES
	MIN.	NOM.	MAX.	MIN.	MAX.	
A	-	-	5.08			
A1	0.51	-	-			
B	-	-	1.77			1
b	0.381	-	0.508			1
c	0.204	-	0.304			
E	-	6.3	-			
e	-	2.54 *	-			2
e1	-	7.62 *	-			3
L	2.5	-	3.9			(a)
L1	-	-	0.76			
ME	7.62	-	8.25			3
Q1	-	-	2.03			
Z						4
θ				0	15	
n =	7×2					5

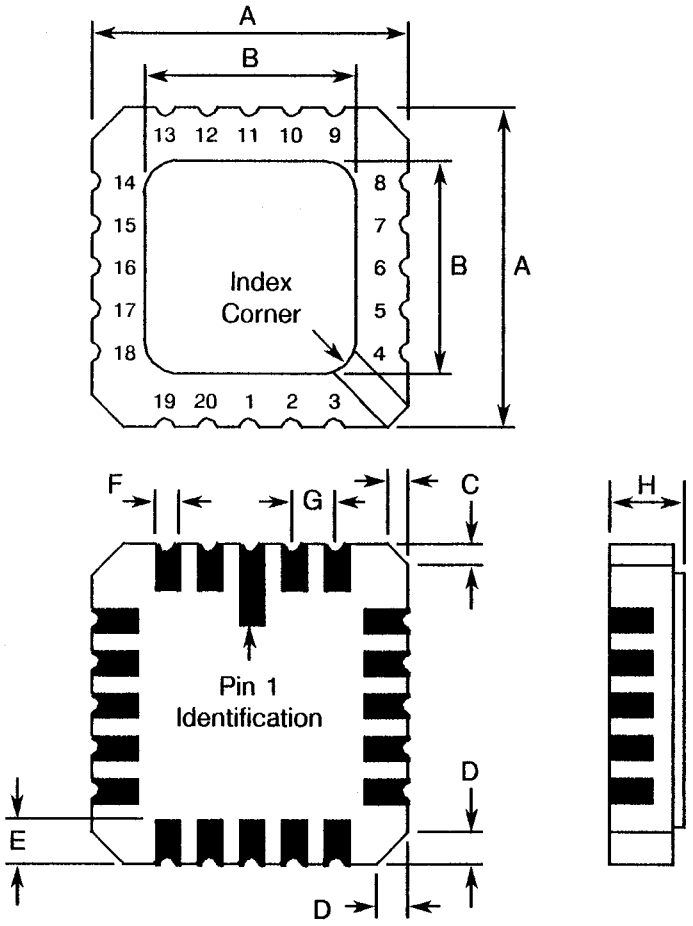
NOTES

1. The lead profile is not required for transition from B to b. The outline of the extreme outputs in the case of F.105A may differ from that of the others, as shown in the Figure.
2. The space between leads is measured on the area L1.
3. Measured when the value of the angle θ is zero.
4. Case F.105: Z between e/2 and e (1.27mm < Z < 2.54mm).
   Case F.105A: Z less than e/2 (Z < 1.27mm).
5. n = quantity of leads.
6. Area for visible reference mark on top face.
7. Base plane.
   * = accurate geometrical location.

(a) Recommended dimensions for the future: minimum 3.0mm.
maximum 3.9mm.
The metric dimensions are calculated from the original dimensions in inches.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - CHIP CARRIER PACKAGE, 20-TERMINAL



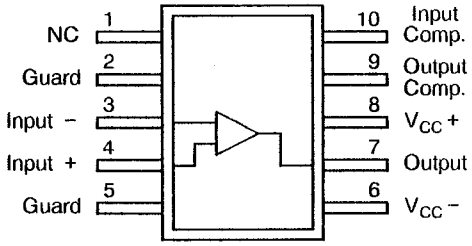
SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	8.69	9.09	-
B	7.80	9.09	-
C	0.25	0.51	4
D	0.89	1.14	5
E	1.14	1.40	2
F	0.56	0.71	2
G	1.27 TYPICAL		1, 3
H	1.63	2.54	-

NOTES

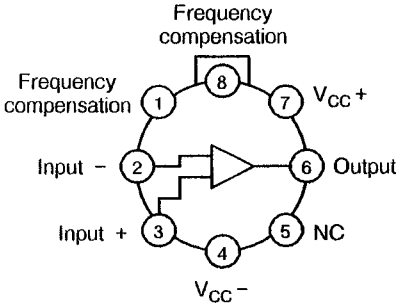
1. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of its true longitudinal position relative to Pins 1 and the highest pin number.
2. All terminals.
3. 16 spaces.
4. Index corner only - 2 dimensions.
5. 3 non-index corners - 6 dimensions.

FIGURE 3(a) - PIN ASSIGNMENT

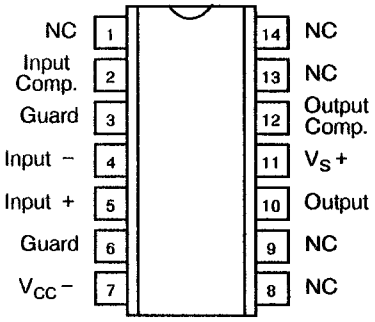
(i) TO91 FLAT PACKAGE



(ii) TO99 METAL CAN



(iii) TO116 (CB2) DUAL-IN-LINE PACKAGE



(iv) - CHIP CARRIER PACKAGE

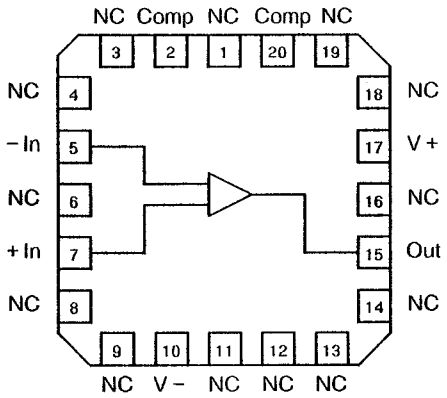
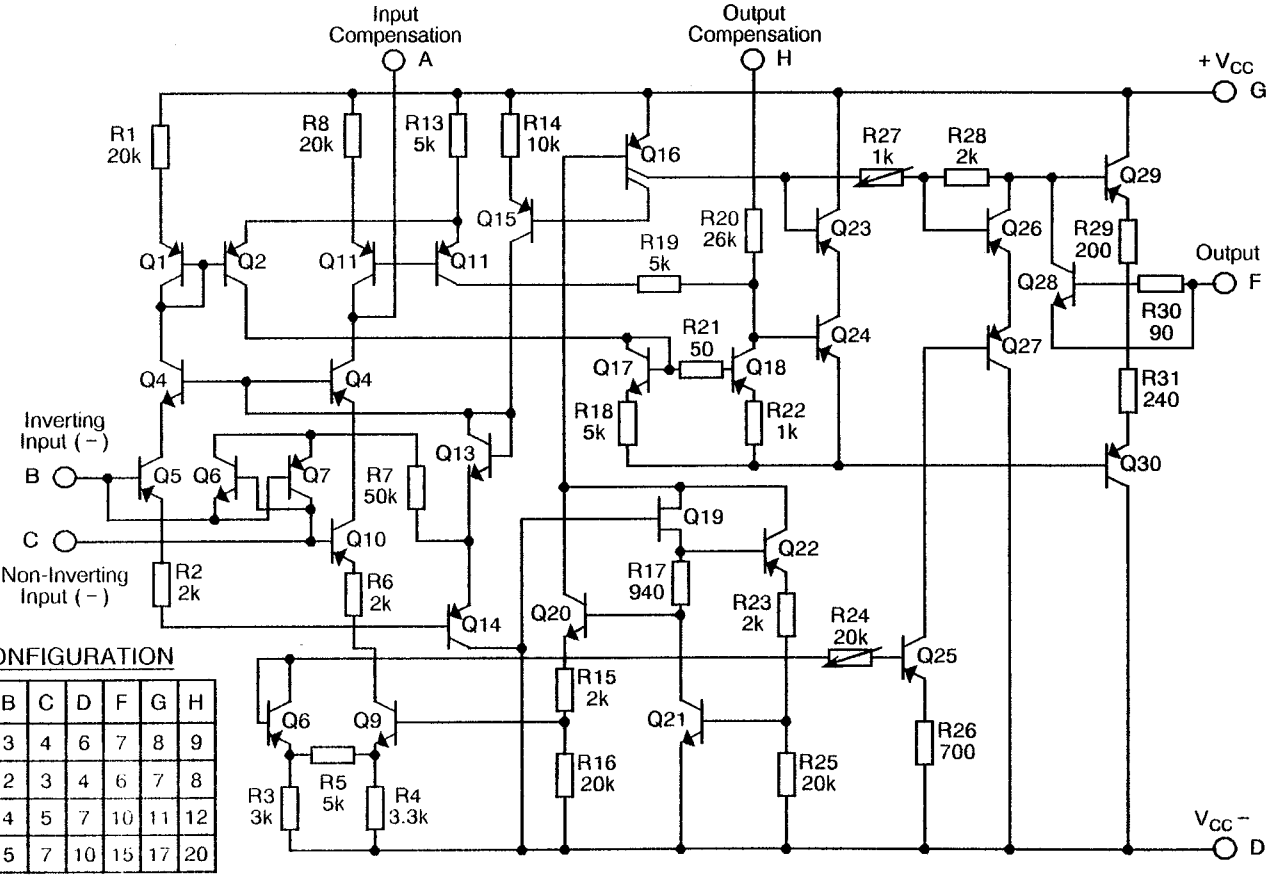


FIGURE 3(b) - TRUTH TABLE

Not applicable.

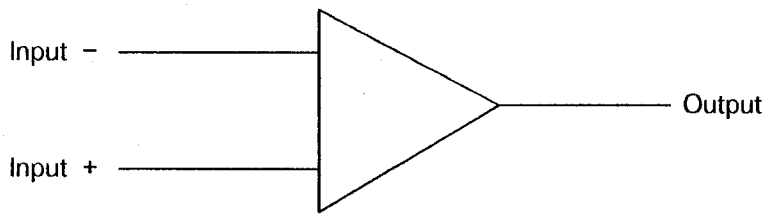
FIGURE 3(c) - CIRCUIT SCHEMATIC (FOR INFORMATION ONLY)



PIN CONFIGURATION

	A	B	C	D	F	G	H
FP	10	3	4	6	7	8	9
TO99	1	2	3	4	6	7	8
DIP	2	4	5	7	10	11	12
CCP	2	5	7	10	15	17	20

FIGURE 3(d) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

K_{OV} = Overshoot.
S_{VR} = Supply Voltage Rejection Ratio.
V_{OM} = Maximum Range of Output Voltage.
I_{OS} = Output Short Circuit Current.
I_I = Input Current.
I_{CC} = Supply Current.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

Subpara. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification, Environmental and Endurance Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be for:-

Variants 01 and 02: 0.35 grammes.
Variants 03, 04 and 07: 1.50 grammes.
Variants 05 and 06: 2.00 grammes.
Variant 08: 0.60 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For flat, TO99 and dual-in-line packages, the lead material shall be Type 'D' with either Type '2', Type '3 or 4' or Type '9' finish in accordance with ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be Type '2' in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

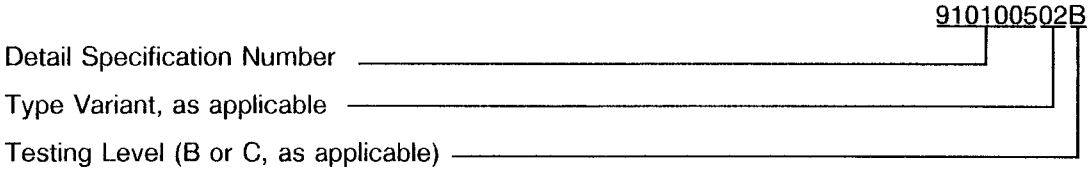
(c) Traceability Information.

4.5.2 Lead Identification

For flat and dual-in-line packages, an index shall be located at the top of the package in the position defined in Note 2 to Figure 2(a) and Note 6 to Figure 2(c) or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering shall be read with the index or tab on the left-hand side. For TO99 packages, a tab shall be used to identify Pin No. 8 as defined in Note 5 to Figure 2(b). For chip carrier packages, the index shall be as defined in Note 4 to Figure 2(d).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL CHARACTERISTICS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3(a) and 3(b). The measurements shall be performed at $T_{amb} = +125$°C and -55°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Burn-in

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $V_{IN}=0V$	-	0.5	mV
2	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}=5.0V$, $-V_{CC}=-5.0V$ $V_{IN}=0V$	-	0.5	mV
3	Input Offset Current	I_{IO1}	4001	4(b)	E_3 (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $R_S=5.0M$, $V_{IN}=0V$	-	0.2	nA
4	Input Offset Current	I_{IO2}	4001	4(b)	E_4 (V)	$+V_{CC}=5.0V$, $-V_{CC}=-5.0V$ $R_S=5.0M$, $V_{IN}=0V$	-	0.2	nA
5	Input (Plus) Bias Current	I_{+IB1}	4001	4(c)	E_5 (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $R_S=5.0M$, $V_{IN}=0V$	-	2.0	nA
6	Input (Plus) Bias Current	I_{+IB2}	4001	4(c)	E_6 (V)	$+V_{CC}=5.0V$, $-V_{CC}=-5.0V$ $R_S=5.0M$, $V_{IN}=0V$	-	2.0	nA
7	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_7 (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $R_S=5.0M$, $V_{IN}=0V$	-	2.0	nA
8	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_8 (V)	$+V_{CC}=5.0V$, $-V_{CC}=-5.0V$ $R_S=5.0k$, $V_{IN}=0V$	-	2.0	nA
9	Power Supply Current	$I_{CC(-)}$	4005	4(e)	I_{CC}	$+V_{CC}=20V$, $-V_{CC}=-20V$	-	0.6	mA
10	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC}=15V$, $-V_{CC}=-15V$ $V_{IN}=-15V$ Note 1	-15	-2.0	mA
11	Short Circuit Output Current (Minus)	$I_{OS(-)}$	3011	4(f)	I_{OS}	$+V_{CC}=15V$, $-V_{CC}=-15V$ $V_{IN}=+15V$ Note 1	2.0	15	mA
12	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_9 (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $V_{IN}=-15V$, $R_L=10k$	80	-	V/mV
13	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{10} (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $V_{IN}=+15V$, $R_L=10k$	80	-	V/mV

NOTES: See Page 21.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
14	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_{11} (V)	$+V_{CC} = +5.0V, -V_{CC} = -5.0V$ $V_{IN} = -2.0V, R_L = 10k$	20	-	V/mV
15	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{12} (V)	$+V_{CC} = +5.0V, -V_{CC} = -5.0V$ $V_{IN} = +2.0V, R_L = 10k$	20	-	V/mV
16	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(h)	E_{13} (V)	$+V_{CC} = 10V, -V_{CC} = -20V$ $V_{IN} = 0V$	-100	100	µV/V
17	Power Supply Rejection Ratio (Minus)	-PSRR	4003	4(h)	E_{14} (V)	$+V_{CC} = 20V, -V_{CC} = -10V$ $V_{IN} = 0V$	-100	100	µV/V
18	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{15} (V)	$+V_{CC} = 35V, -V_{CC} = -5.0V$ $V_{IN} = -15V$	96	-	dB
19					E_{16} (V)	$+V_{CC} = 5.0V, -V_{CC} = -35V$ $V_{IN} = 15V$			
20	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{17} (V)	$+V_{CC} = 20V, -V_{CC} = -20V$ $V_{IN} = -20V, R_L = 10k$	18	-	V
21	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{18} (V)	$+V_{CC} = 20V, -V_{CC} = -20V$ $V_{IN} = +20V, R_L = 10k$	-	-18	V

NOTES: See Page 21.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Test Conditions	Limits		Unit
						Min	Max	
22	Slew Rate (Plus)	SR(+)	4002	4(j)	$+V_{CC} = \pm 20V$ $V_{IN} = -5.0V$ to $+5.0V$ square $R_L = 10k$ Note 2	0.1	-	V/µs
23	Slew Rate (Minus)	SR(−)	4002	4(j)	$+V_{CC} = \pm 20V$ $V_{IN} = -5.0V$ to $+5.0V$ square $R_L = 10k$ Note 2	0.1	-	V/µs
24	Rise Time	RT	4002	4(j)	$V_{CC} = \pm 20V$, $V_{IN} = 50mV$ $R_L = 10k$ Note 2	-	1000	ns
25	Overshoot	OS	4002	4(j)	$V_{CC} = \pm 20V$, $V_{IN} = 50mV$ $R_L = 10k$ Note 2	-	40	%

NOTES

1. For sampling inspections and end-point tests, the duration of measurement of I_{OS} shall be 5 seconds minimum. For other tests, this duration may be reduced to be consistent with automatic test procedures provided that the same limits are maintained.
2. Sample Test Inspection Level = II, AQL = 2.5%.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = 0V	-	1.0	mV
2	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V V_{IN} = 0V	-	1.0	mV
3	Input Offset Current	I_{IO1}	4001	4(b)	E_3 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V R_S = 5.0M, V_{IN} = 0V	-	0.2	nA
4	Input Offset Current	I_{IO2}	4001	4(b)	E_4 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V R_S = 5.0M, V_{IN} = 0V	-	0.2	nA
5	Input (Plus) Bias Current	I_{+IB1}	4001	4(c)	E_5 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V R_S = 5.0M, V_{IN} = 0V	-	2.0	nA
6	Input (Plus) Bias Current	I_{+IB2}	4001	4(c)	E_6 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V R_S = 5.0M, V_{IN} = 0V	-	2.0	nA
7	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_7 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V R_S = 5.0M, V_{IN} = 0V	-	2.0	nA
8	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_8 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V R_S = 5.0k, V_{IN} = 0V	-	2.0	nA
9	Power Supply Current	$I_{CC(-)}$	4005	4(e)	I_{CC}	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V	-	0.8	mA
10	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_{IN} = −15V Note 1	−15	-	mA
11	Short Circuit Output Current (Minus)	$I_{OS(-)}$	3011	4(f)	I_{OS}	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_{IN} = +15V Note 1	-	15	mA
12	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_9 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = −15V, R_L = 10k	40	-	V/mV
13	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{10} (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = +15V, R_L = 10k	40	-	V/mV
20	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{17} (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = −20V, R_L = 10k	18	-	V
21	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{18} (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = +20V, R_L = 10k	-	−18	V

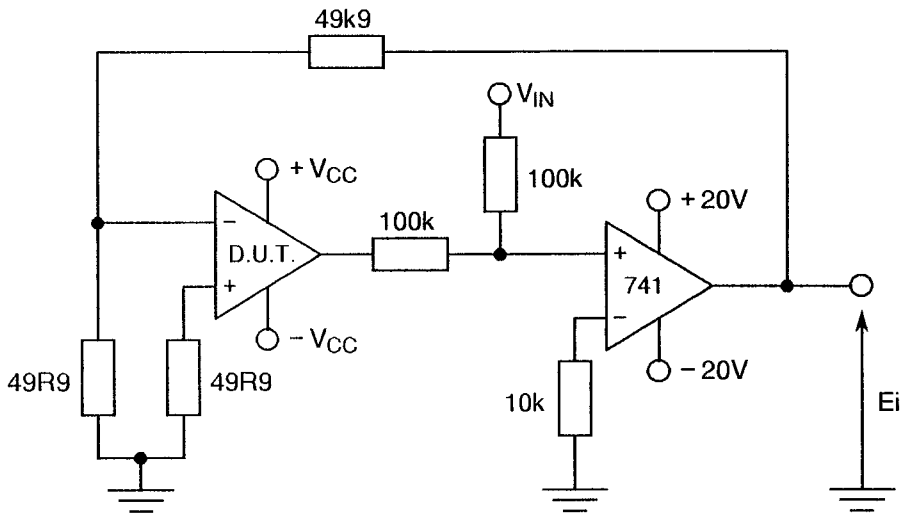
NOTES: See Page 21.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions	Limits		Unit
							Min	Max	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = 0V	-	1.0	mV
2	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V V_{IN} = 0V	-	1.0	mV
3	Input Offset Current	I_{IO1}	4001	4(b)	E_3 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V R_S = 5.0M, V_{IN} = 0V	-	0.4	nA
4	Input Offset Current	I_{IO2}	4001	4(b)	E_4 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V R_S = 5.0M, V_{IN} = 0V	-	0.4	nA
5	Input (Plus) Bias Current	I_{+IB1}	4001	4(c)	E_5 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V R_S = 5.0M, V_{IN} = 0V	-	3.0	nA
6	Input (Plus) Bias Current	I_{+IB2}	4001	4(c)	E_6 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V R_S = 5.0M, V_{IN} = 0V	-	3.0	nA
7	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_7 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V R_S = 5.0M, V_{IN} = 0V	-	3.0	nA
8	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_8 (V)	$+V_{CC}$ = 5.0V, $-V_{CC}$ = −5.0V R_S = 5.0k, V_{IN} = 0V	-	3.0	nA
9	Power Supply Current	$I_{CC(-)}$	4005	4(e)	I_{CC}	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V	-	1.6	mA
10	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_{IN} = −15V Note 1	−15	-	mA
11	Short Circuit Output Current (Minus)	$I_{OS(-)}$	3011	4(f)	I_{OS}	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_{IN} = +15V Note 1	-	15	mA
12	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_9 (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = −15V, R_L = 10k	40	-	V/mV
13	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{10} (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = +15V, R_L = 10k	40	-	V/mV
20	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{17} (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = −20V, R_L = 10k	18	-	V
21	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{18} (V)	$+V_{CC}$ = 20V, $-V_{CC}$ = −20V V_{IN} = +20V, R_L = 10k	-	−18	V

NOTES: See Page 21.

FIGURE 4(a) - INPUT OFFSET VOLTAGE

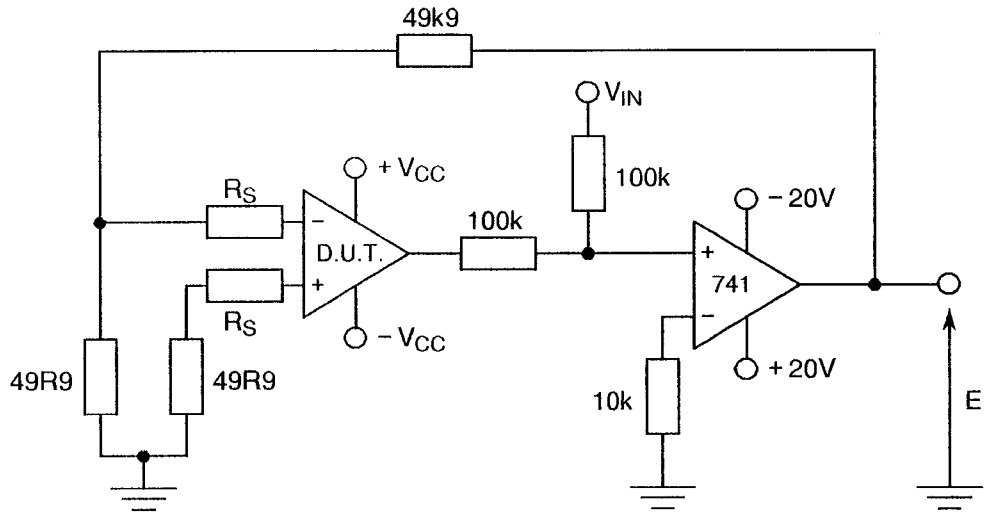


V_{IO1} (mV) = E_1 (V), V_{IO2} (mV) = E_2 (V).

NOTES

1. All resistors to be 0.1% tolerance.

FIGURE 4(b) - INPUT OFFSET CURRENT

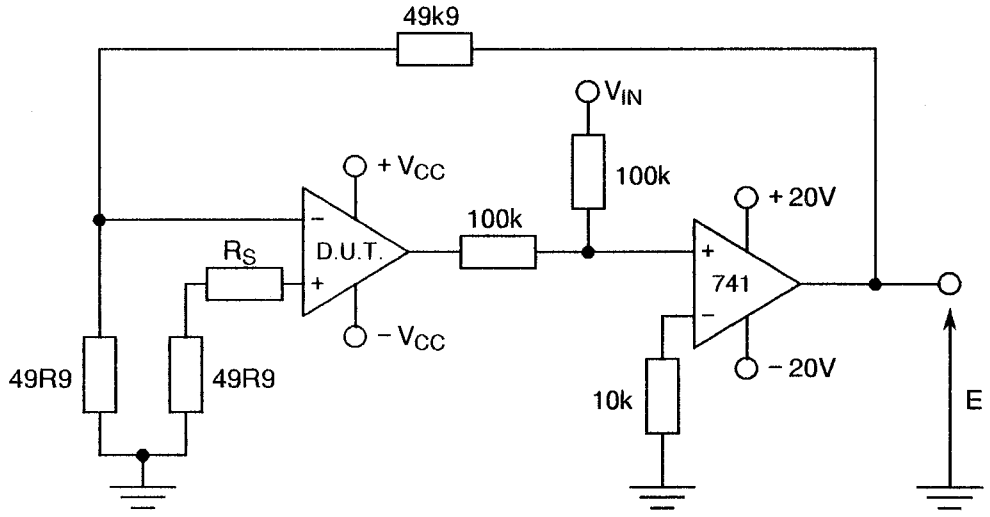


$$I_{IO1}\ (nA) = \frac{(E_1\ (V) - E_3\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{IO2}\ (nA) = \frac{(E_2\ (V) - E_4\ (V))\ 10^6}{R_S\ (k\Omega)}$$

NOTES

1. All resistors to be 0.1% tolerance.

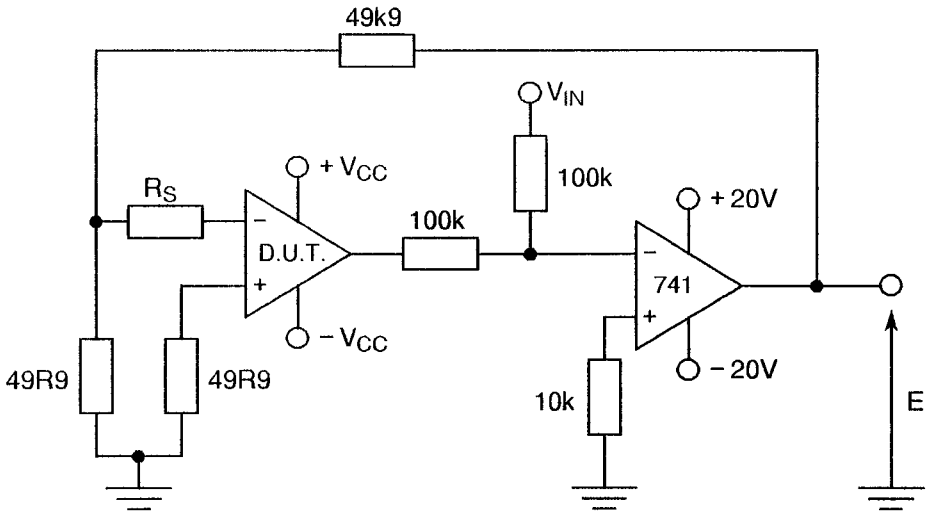
FIGURE 4(c) - INPUT (PLUS) BIAS CURRENT



$$I_{+IB1}\ (nA) = \frac{(E_1\ (V) - E_5\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{+IB2}\ (nA) = \frac{(E_2\ (V) - E_6\ (V))\ 10^6}{R_S\ (k\Omega)}$$

NOTES
1. All resistors to be 0.1% tolerance.

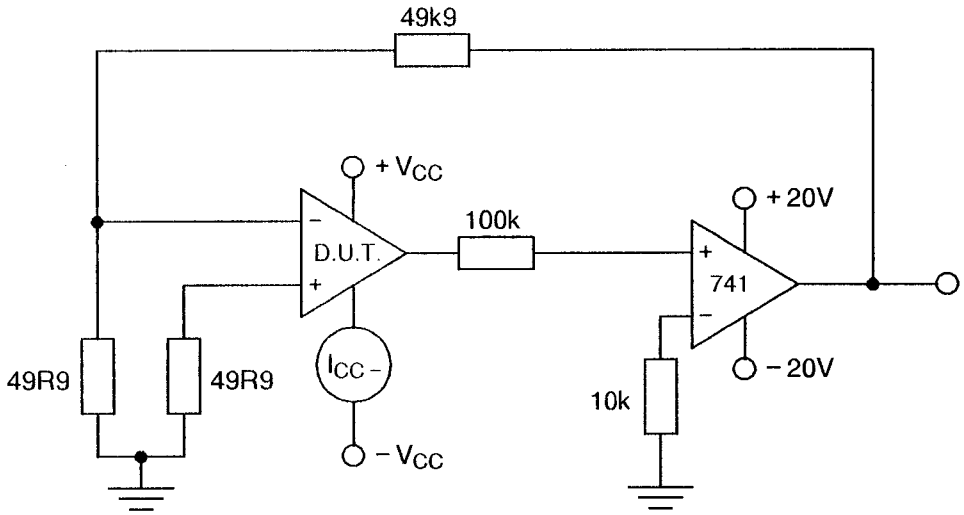
FIGURE 4(d) - INPUT (MINUS) BIAS CURRENT



$$I_{-IB1}\ (nA) = \frac{(E_7\ (V) - E_1\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{-IB2}\ (nA) = \frac{(E_8\ (V) - E_2\ (V))\ 10^6}{R_S\ (k\Omega)}$$

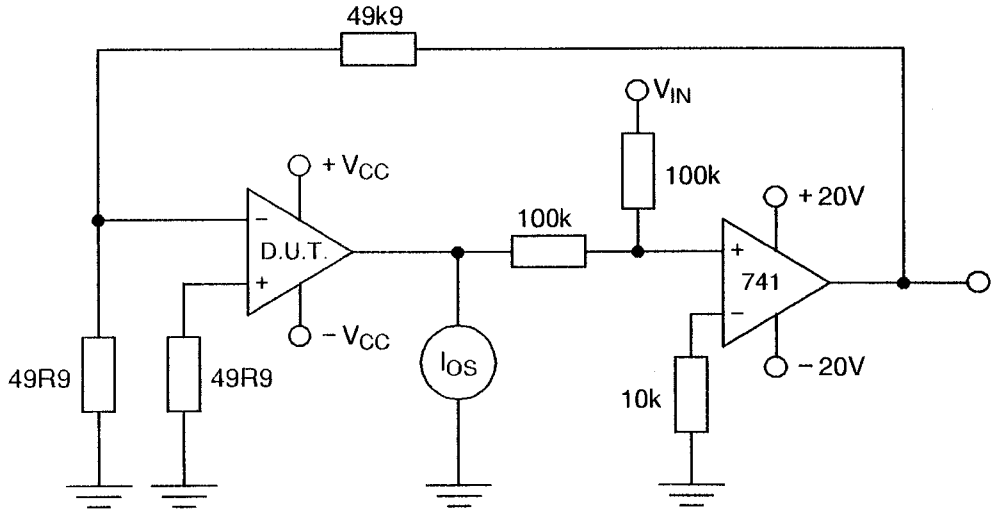
NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(e) - SUPPLY CURRENT



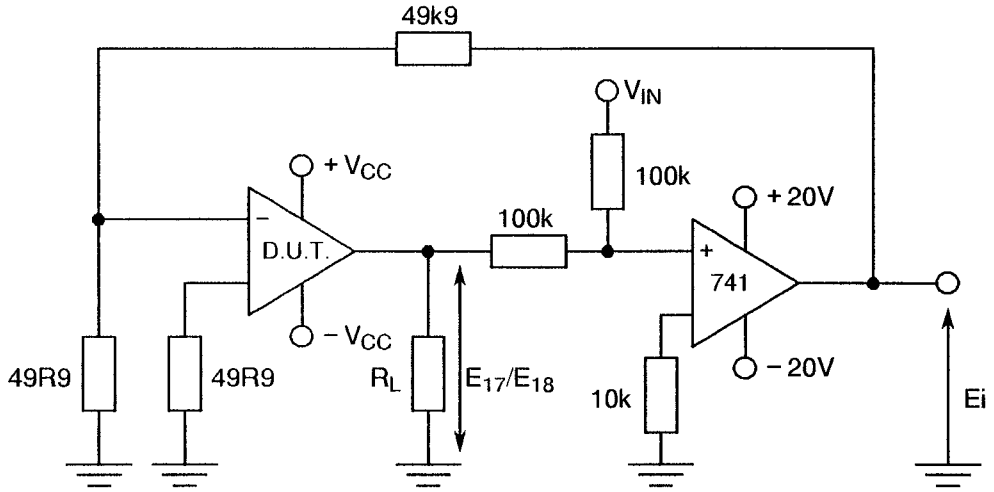
NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(f) - SHORT CIRCUIT OUTPUT CURRENT



NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(g) - OUTPUT VOLTAGE SWING
- OPEN LOOP VOLTAGE GAIN



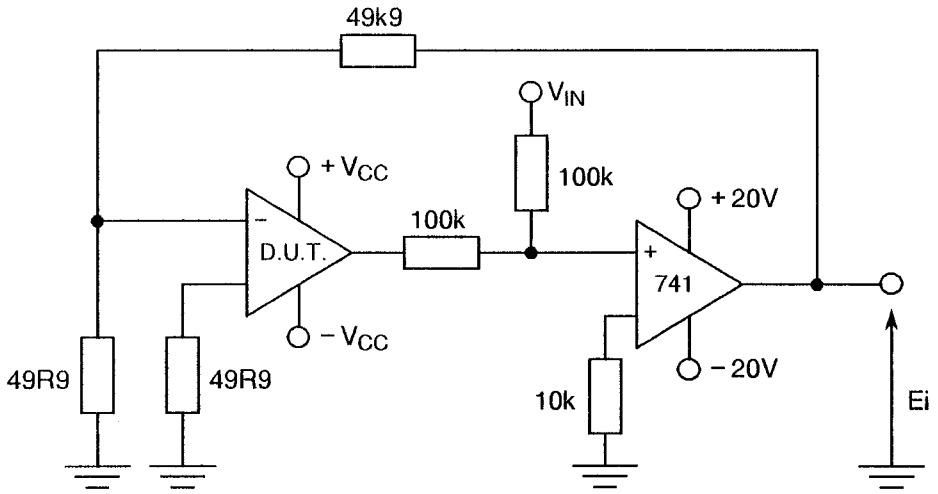
1. $V_{OUT} = (E_{17}, E_{18})$

2. $+A_{VS} = \frac{15}{E_1 - E_9}$, $+A_{VS} = \frac{2}{E_2 - E_{11}}$

3. $-A_{VS} = \frac{15}{E_{10} - E_1}$, $-A_{VS} = \frac{2}{E_{12} - E_2}$

NOTES
1. E_9, E_{10}, E_{11}, E_{12} is in Volts.
2. All resistors to be 0.1% tolerance.

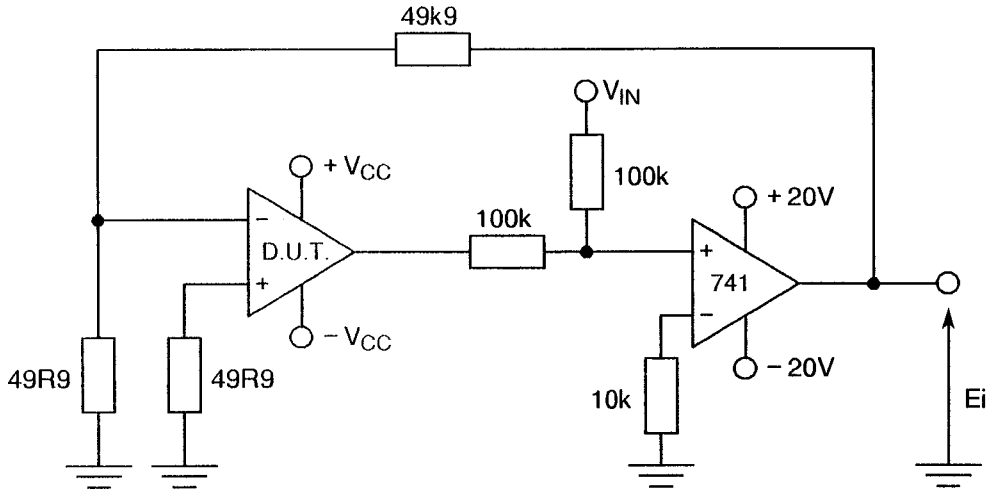
FIGURE 4(h) - POWER SUPPLY REJECTION RATIO



$+PSRR\ (\mu V/V) = (E_1\ (V) - E_{13}\ (V))\ 10^2$, $-PSRR\ (\mu V/V) = (E_1\ (V) - E_{14}\ (V))\ 10^2$

NOTES
1. All resistors to be 0.1% tolerance.
2. Ei is measured to four digits accuracy.

FIGURE 4(i) - COMMON MODE REJECTION RATIO

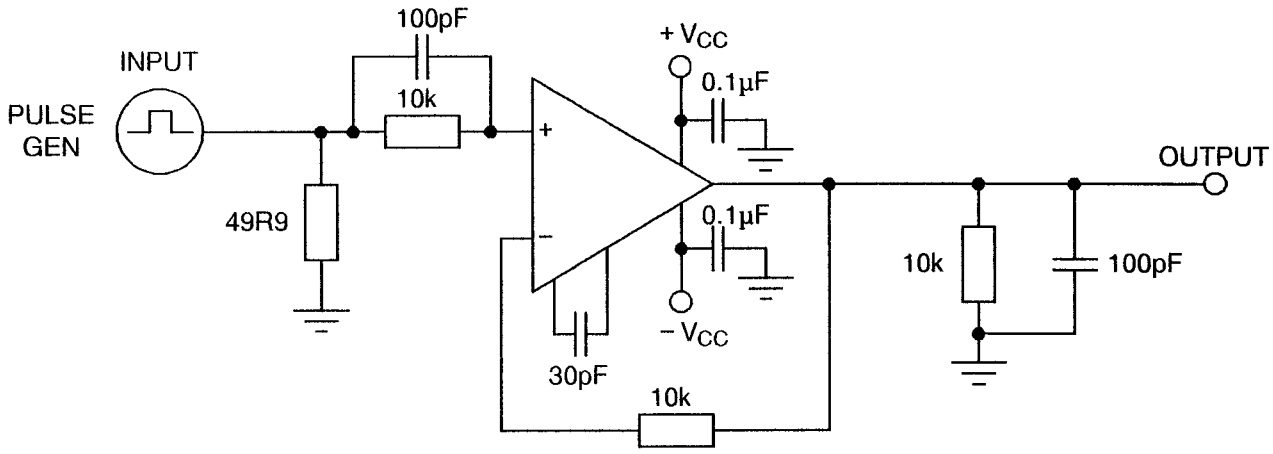


$$CMRR\ (dB) = 20\ LOG\ \frac{30.10^3}{E_{15}\ (V) - E_{16}\ (V)}$$

NOTES

1. Resistors of 49R9Ω at inputs shall be of 0.01% tolerance matched to 0.001%. Remaining resistors shall be of 0.1% tolerance.

FIGURE 4(k) - DYNAMIC TEST MEASUREMENT CIRCUIT



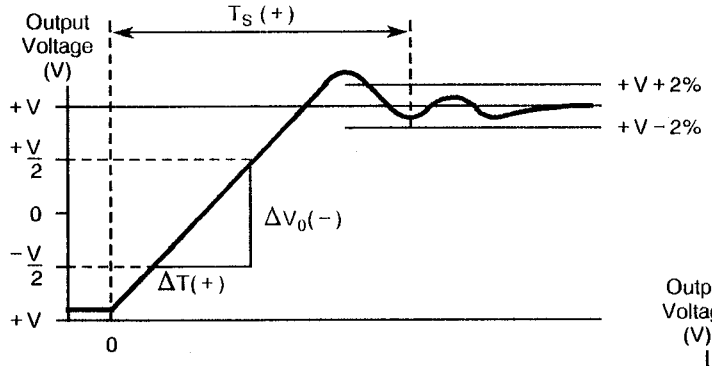
NOTES

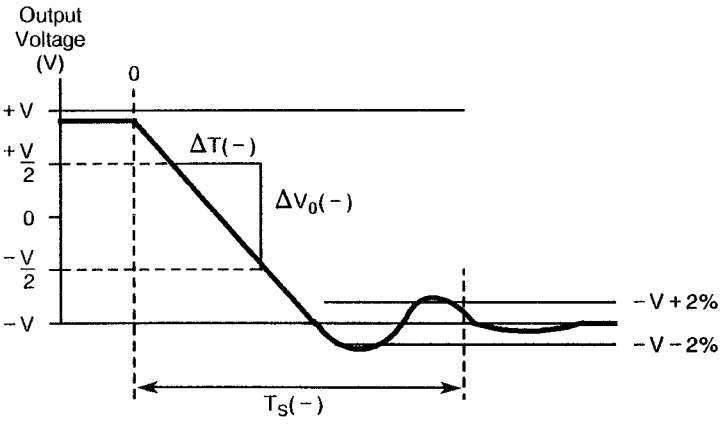
1. Pulse Generator:
   - Rise time ≤ 10ns
   - Repetition rate 1.0kHz (max.)
   - Pulse voltage: −5.0V to +5.0V for slew rate measurement
   - Pulse voltage: 50mV for rise time and overshoot measurement

$$SR = \left| \frac{\Delta V_0}{\Delta T} \right| \ (V/\mu s)$$

$$RT = t \ (\mu s)$$

$$OS = \frac{\Delta V}{50} \ 100(\%)$$





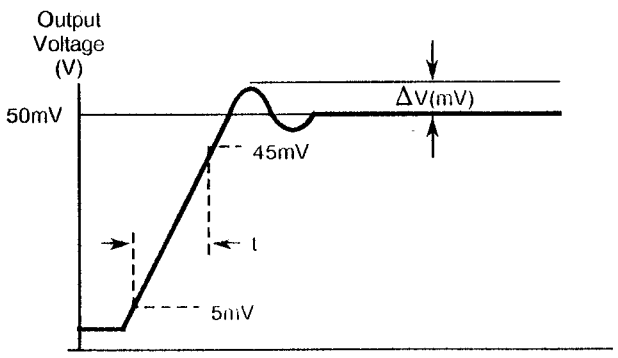


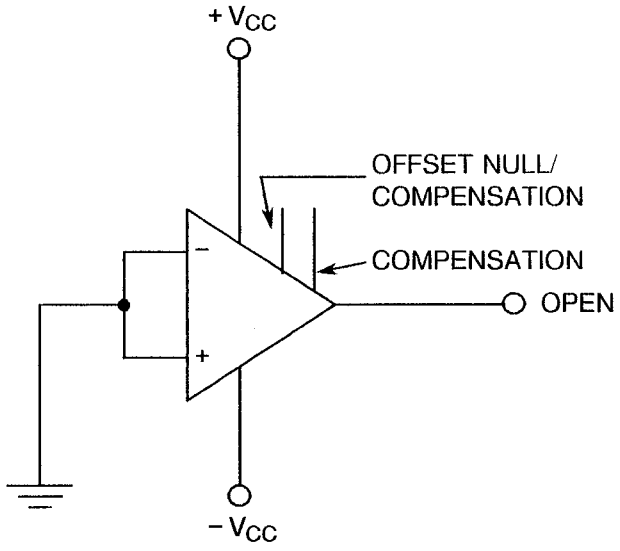
TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Input Offset Voltage Change	V_{IO}	As per Table 2	As per Table 2	± 0.25	mV
3	Input Offset Current Change	I_{IO}	As per Table 2	As per Table 2	± 0.2	nA
5	Input Bias Current Change	I_{IB}	As per Table 2	As per Table 2	± 0.4	nA

TABLE 5 - CONDITIONS FOR BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125 ± 5	°C
2	Supply Voltage	V_{CC}	± 20	V

FIGURE 5 - BURN-IN CIRCUIT



4.8 ENVIRONMENTAL AND ENDURANCE TESTS

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Input Offset Voltage	V_{IO}	As per Table 2	As per Table 2	-	0.5	mV
3	Input Offset Current	I_{IO}	As per Table 2	As per Table 2	-	0.2	nA
5	Input Bias Current	I_{IB}	As per Table 2	As per Table 2	-	2.0	nA
9	Power Supply Current	I_{CC}	As per Table 2	As per Table 2	-	0.6	mA
12	Open Loop Voltage Gain	$+A_{VS}$	As per Table 2	As per Table 2	80	-	V/mV

APPENDIX 'A'

AGREED DEVIATIONS FOR THOMSON-CSF/DCI

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Tables 2, 3(a) and 3(b)	Tests 3 through to 8: I_{ID} and I_{IB}, change R_S condition to 1.0MΩ.

APPENDIX 'B'

AGREED DEVIATIONS FOR MOTOROLA (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Table 2 (a.c.)	Tests 22 through to 25: Change V_{CC} condition to $V_{CC} = \pm 18V$.
Tables 2, 3(a) and 3(b)	Tests 3 through to 8: Change R_S condition to $R_S = 100k\Omega$.