INTEGRATED CIRCUITS, SILICON MONOLITHIC,

DUAL, BIPOLAR OPERATIONAL AMPLIFIERS,

BASED ON TYPE LM 747

ESCC Detail Specification No. 9101/008

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Pages 1 to 39

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space components
coordination group

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		SCCG Chairman	ESA Director General or his Deputy
Issue 2	November 1981	-	-
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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This issue incorporates all modifications agreed on the basis of Policy DCR 21016 for adaption to new qualification requirements and Policy DCR 21019 (Appendices to Detail Specifications)		
'A'	Jul. '84	P1. Cover page		None
		P2. DCN		None
		P4. T of C	: Table 6 title amended	23121
		P7. Table 1(a)	: Lead Material and Finish redefined	21025
		P15. Para. 2	: MIL-STD-1276 deleted	21025
		P17. Para. 4.4.2	: Rewritten	21025
		P21. Table 2	: Test 34 to 35, variant 12 changed to 10	23121
		P25. Table 3(a)	: As Table 2	23121
		P28. Table 3(b)	: As Table 2	23121
		P33. Figure 4(g)	: Note 1 corrected	23121
		P39. Table 6	: Units of Test 34 to 35 corrected	23121
'B'	Dec. '91	P1. Cover page		None
		P2. DCN		None
		P3. T of C	: Para. 4.3.3 deleted	None
		P15. Para. 4.2.2	: Deviation deleted, "None" added	21048
		P16. Para. 4.2.4	: Deviation deleted, "None" added	22919
		Para. 4.2.5	: Deviation deleted, "None" added	22919
		Para. 4.3.3	: Paragraph deleted	22921
'C'	Jul. '93	P1. Cover page		None
		P2. DCN		None
		P2A. DCN	: Page added	None
		P7. Table 1(a)	: Table standardised	22975
			: Variant "13" added	22975
			: Note 1, G^1 amended to G'	22975
		P8. Table 1(b)	: No. 4, Variant "13" added to "Type Variants 05-08" in Characteristics	22975
		P9. Notes to Fig. 1	: Note 2, Variant "13" added to "Type Variants 05 to 08"	22975

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.
		P16. Para. 4.3.2	: Variant "13" added to "Type Variants 05 to 08"	22975
		P17. Para. 4.4.2	: "or Type 9" added	22975
		Para. 4.5.2	: Variant "13" added to "Type Variants 05 to 08"	22975
		P21. Table 2	: Nos. 34 to 35, Characteristics amended to read "09, 10 and 13"	22975
		P25. Table 3(a)	: Nos. 34 to 35, Characteristics amended to read "09, 10 and 13"	22975
		P28. Table 3(b)	: Nos. 34 to 35, Characteristics amended to read "09, 10 and 13"	22975
		P39. Table 6	: Nos. 34 to 35, Characteristics amended to read "09, 10 and 13"	22975
		This specification has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist.		

TABLE OF CONTENTS

TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, dual, bipolar operational amplifier, based on Type LM 747. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

As per Figure 1.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE (FIGURE 3(b))

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH	NOTE
01	FLAT	2(a)	D2	
02	FLAT	2(a)	D3 or D4	
03	FLAT	2(a)	D2	1
04	FLAT	2(a)	D3 or D4	1
05	TO100	2(b)	D2	
06	TO100	2(b)	D3 or D4	
07	TO100	2(b)	D2	1
08	TO100	2(b)	D3 or D4	1
09	DIL	2(c)	D2	
10	DIL	2(c)	D3 or D4	
11	DIL	2(c)	D2	1
12	DIL	2(c)	D3 or D4	1
13	TO100	2(b)	D9	

NOTES

1. G and G' internally connected.

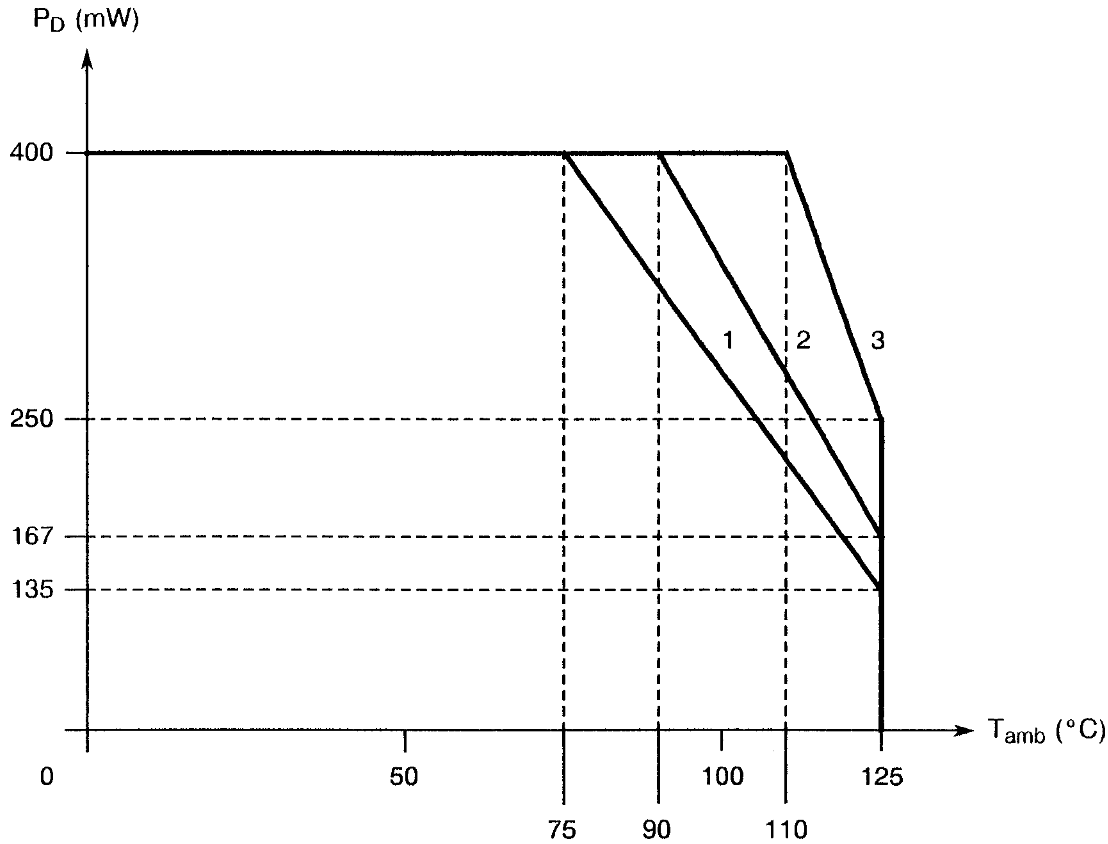
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage Range	V_S	±22	V	
2	Differential Input Voltage Range	V_{ID}	±30	V	
3	Input Voltage Range	V_I	±15	V	Note 1
4	Device Power Dissipation, Both amplifiers - Type Variants 01-04 - Type Variants 05-08,13 - Type Variants 09-12	P_{DISS}	800	mW	 Note 2 Note 3 Note 4
5	Output Short Circuit Duration	-	Indefinite		Note 5
6	Operating Temperature Range	T_{amb}	−55 to +125	°C	
7	Storage Temperature Range	T_{stg}	−55 to +150	°C	
8	Soldering Temperature	T_{sol}	+300	°C	Note 6
9	Junction Temperature	T_j	+150	°C	

NOTES

1. If the supply voltage is less than +15V, the maximum input voltage is equal to the supply voltage.
2. Derate above T_{amb} = +76°C at 5.41mW/°C.
3. Derate above T_{amb} = +90°C at 6.67mW/°C.
4. Derate above T_{amb} = +110°C at 10mW/°C.
5. Continuous short circuit is allowed for an ambient temperature of +70°C and a case temperature of +125°C.
6. Duration: 2 to 5 seconds.

FIGURE 1 - DEVICE DISSIPATION DERATING WITH TEMPERATURE (PER AMPLIFIER)

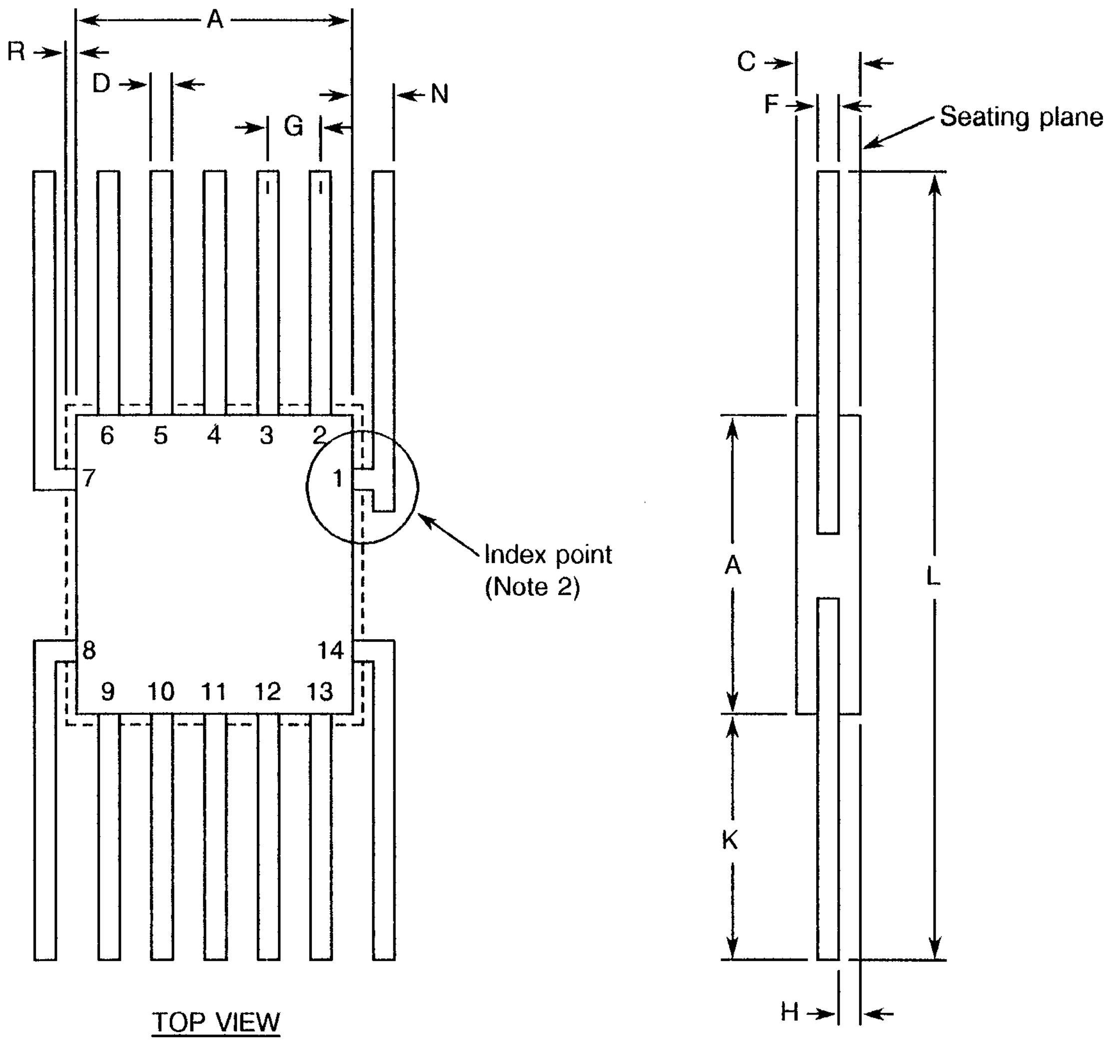


NOTES

1. Derating for type variants 01 to 04.
2. Derating for type variants 05 to 08 and 13.
3. Derating for type variants 09 to 12.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE



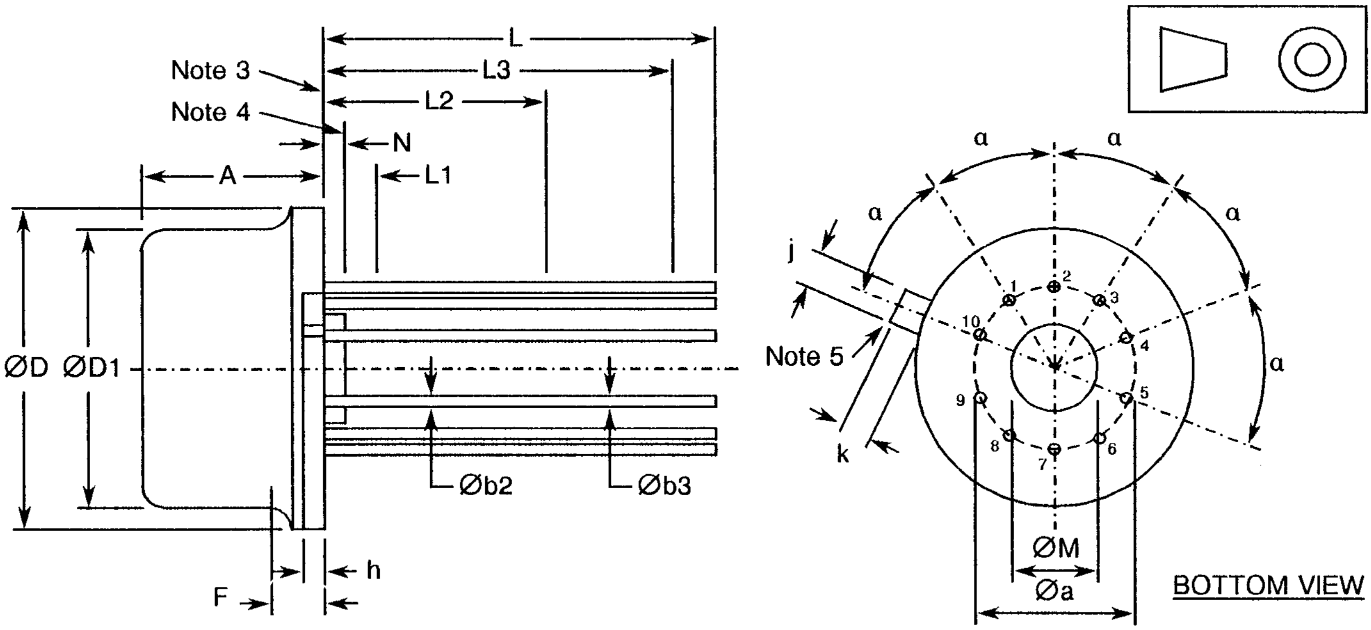
SYMBOL	MILLIMETRES		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	-	6.985	-	0.275	
C	-	2.032	-	0.080	
D	0.381	0.482	0.015	0.019	
F	0.101	0.152	0.004	0.006	
G	1.143	1.397	0.045	0.055	1
H	-	-	0.020	0.040	
K	6.032	6.299	0.2375	0.2480	
L	19.05	19.558	0.750	0.770	
N	0.444	0.876	0.0175	0.0345	

NOTES

1. The space between terminals has to be measured at a distance of 0.76mm maximum (0.030 inch) from where the terminals emerge from the case.
2. Pin 1 index shall be within the area shown.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - METAL CAN TO100



SYMBOL	MILLIMETRES			INCHES			DEGR. NOM.	NOTES
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Øa	-	5.84 (*)	-	-	0.230 (*)	-		1
A	4.20	-	4.69	0.165	-	0.185		
Øb2	0.407	-	0.508	0.016	-	0.020		
Øb3	-	-	0.53	-	-	0.021		
ØD	8.51	-	9.39	0.335	-	0.370		
ØD1	7.75	-	8.50	0.305	-	0.335		
F	-	-	1.27	-	-	0.050		
h	0.23	-	1.01	0.009	-	0.040		
j	0.712	0.787	0.863	0.028	0.031	0.034		
k	0.74	-	1.14	0.029	-	0.045		2
L	12.70	-	-	0.500	-	-		
L1	-	-	1.27	-	-	0.050		
L2	6.35	-	-	0.250	-	-		
L3	12.70	-	-	0.500	-	-		
ØM	3.56	-	4.06	0.140	-	0.160		
N	-	-	1.01	0.010	-	0.040		
α							36° (*)	1

NOTES

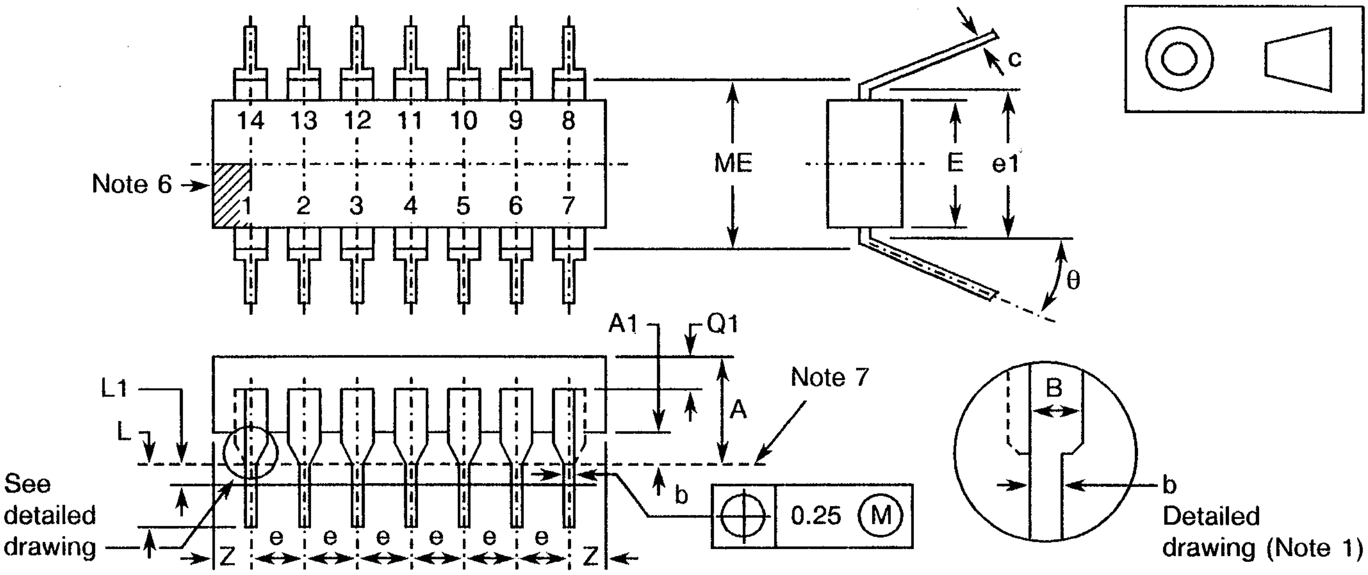
1. The section of each terminal, from a distance of 1.37mm (0.054 inch) to the reference plane, shall be located in a ring whose diameter is 0.99mm (0.039 inch), centred on the accurate geometrical point defining the terminal axis.
2. Measured from the D diameter.
3. Reference plane.
4. Base plane.
5. Reference index of Pin 10.

   * = accurate geometrical location.

   The metric dimensions are calculated from the original dimensions in inches.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - CERAMIC DIP



SYMBOL	MILLIMETRES			INCHES			DEGREES		NOTES
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	MAX.	
A	-	-	5.08	-	-	0.200			
A1	0.51	-	-	0.020	-	-			
B	-	-	1.77	-	-	0.070			1
b	0.381	-	0.508	0.015	-	0.020			1
c	0.204	-	0.304	0.008	-	0.012			
E	-	6.3	-	-	0.25	-			
e	-	2.54 *	-	-	0.100 *	-			2
e1	-	7.62 *	-	-	0.300 *	-			3
L	2.5	-	3.9	0.098	-	0.154			(a)
L1	-	-	0.76	-	-	0.030			
ME	7.62	-	8.25	0.300	-	0.325			3
Q1	-	-	2.03	-	-	0.080			
Z									4
θ							0	15	
n =	7×2								5

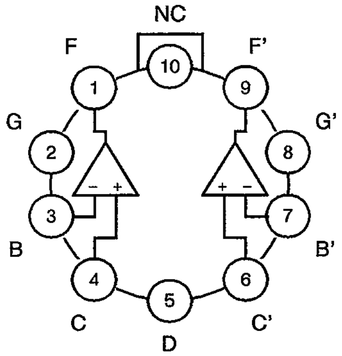
NOTES

1. The lead profile is not required for transition from B to b. The outline of the extreme outputs in the case of F.105A may differ from that of the others, as shown in the Figure.
2. The space between leads is measured on the area L1.
3. Measured when the value of the angle θ is zero.
4. Case F.105: Z between e/2 and e (1.27mm < Z < 2.54mm).
   Case F.105A: Z less than e/2 (Z < 1.27mm).
5. n = quantity of leads.
6. Area for visible reference mark on top face.
7. Base plane.
   * = accurate geometrical location.

(a) Recommended dimensions for the future: minimum 3.0mm (0.122 inch).
maximum 3.9mm (0.154 inch).
The metric dimensions are calculated from the original dimensions in inches.

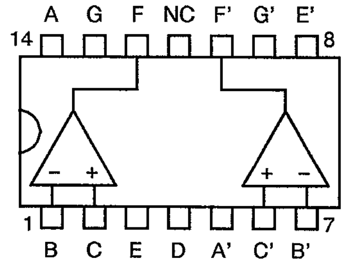
FIGURE 3(a) - PIN ASSIGNMENT

TO-100 METAL CAN



TOP VIEW

DUAL-IN-LINE PACKAGE



TOP VIEW

FIGURE 3(b) - TRUTH TABLE

Not applicable.

FIGURE 3(c) - CIRCUIT SCHEMATIC (FOR INFORMATION ONLY)

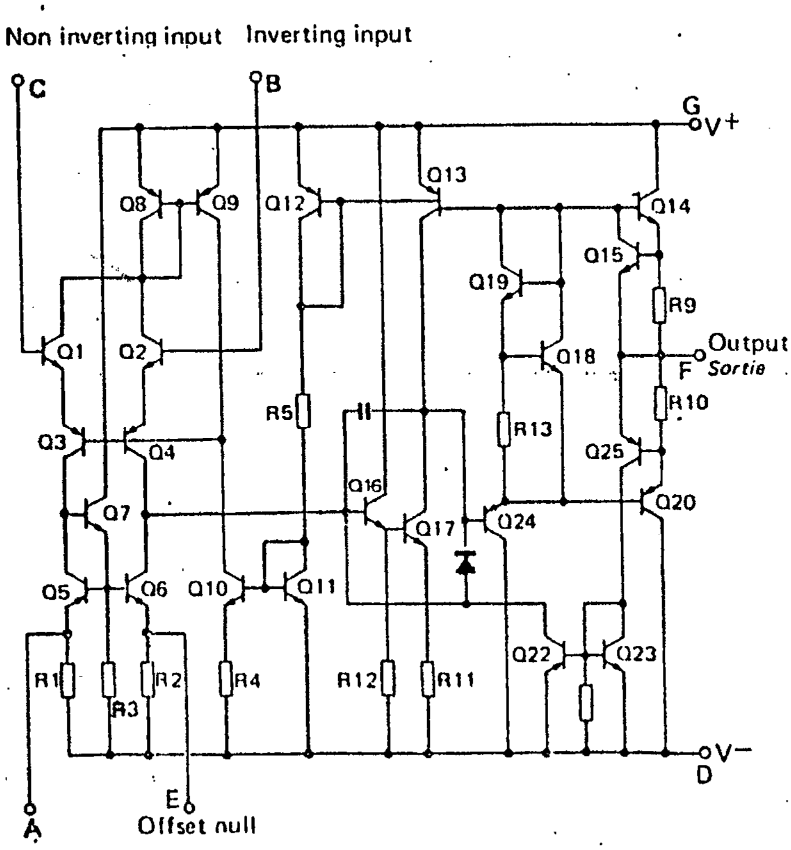
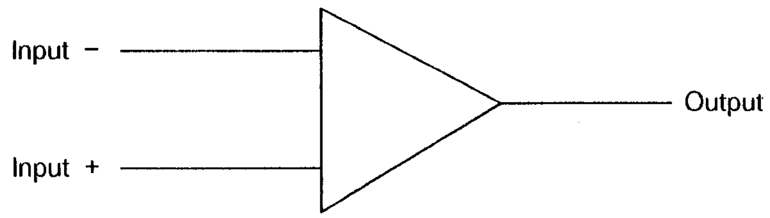


FIGURE 3(d) - FUNCTIONAL DIAGRAM



Repeated 2 times

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

PSRR = Power Supply Rejection Ratio.
OS = Overshoot.
RT = Rise Time.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

The following deviations from ESA/SCC Generic Specification No. 9000 shall apply:-

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

Subpara. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification, Environmental and Endurance Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be for:-

Variants 01 to 04:	0.35 grammes.
Variants 05 to 08 and 13:	1.50 grammes.
Variants 09 to 12:	2.00 grammes.

4.4 MATERIALS

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

The leads shall be Type 'D' with either Type '2', Type '3 or 4' or Type '9' finish in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 2 of Figure 2 (Variants 01 to 04), Note 5 of Figure 2 (Variants 05 to 08 and 13) or Note 6 of Figure 2 (Variants 09 to 12). Alternatively, a tab may be used to identify Pin No. 1. The pin numbering shall be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

910100802B

Detail Specification Number (9101008)

Type Variant, as applicable (02)

Testing Level (B or C, as applicable) (B)

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.5.5 Marking of Small Components

When it is considered that the component is too small to accommodate the marking as specified above, as much as space permits shall be marked. The order of precedence shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

The marking information in full shall accompany each component in its primary package.

4.6 ELECTRICAL CHARACTERISTICS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3(a) and 3(b). The measurements shall be performed at $T_{amb} = +125(+0-5)$°C and $-55(+5-0)$°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Burn-in

Circuits for use in performing the burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits Min	Limits Max	Unit
1 to 2	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $V_{IN} = -15V$	-	5.0	mV
3 to 4	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $V_{IN} = 15V$	-	5.0	mV
5 to 6	Input Offset Voltage	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = 0V$	-	5.0	mV
7 to 8	Input Offset Voltage	V_{IO4}	4001	4(a)	E_4 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = 0V$	-	5.0	mV
9 to 10	Input Offset Current	I_{IO1}	4001	4(b)	E_5 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	200	nA
11 to 12	Input Offset Current	I_{IO2}	4001	4(b)	E_6 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	200	nA
13 to 14	Input Offset Current	I_{IO3}	4001	4(b)	E_7 (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	200	nA
15 to 16	Input Offset Current	I_{IO4}	4001	4(b)	E_8 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	200	nA
17 to 18	Input (Plus) Bias Current	I_{+IB1}	4001	4(c)	E_9 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	500	nA
19 to 20	Input (Plus) Bias Current	I_{+IB2}	4001	4(c)	E_{10} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	500	nA
21 to 22	Input (Plus) Bias Current	I_{+IB3}	4001	4(c)	E_{11} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA
23 to 24	Input (Plus) Bias Current	I_{+IB4}	4001	4(c)	E_{12} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA
25 to 26	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_{13} (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	500	nA
27 to 28	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_{14} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	500	nA
29 to 30	Input (Minus) Bias Current	I_{-IB3}	4001	4(d)	E_{15} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA
31 to 32	Input (Minus) Bias Current	I_{-IB4}	4001	4(d)	E_{16} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits Min	Limits Max	Unit
33	Power Supply Current Variants 03, 04, 07, 08, 11 and 12	$I_{CC(-)1}$	4005	4(e)	I_{CC1}	$+V_{CC} = +15V$, $-V_{CC} = -15V$	-	5.6	mA
34 to 35	Power Supply Current Variants 01, 02, 05, 06, 09, 10 and 13	$I_{CC(-)2}$	4005	4(e)	I_{CC2}	$+V_{CC} = +15V$, $-V_{CC} = -15V$	-	2.8	mA
36 to 37	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = -15V$ Note 2	-45	-9.0	mA
38 to 39	Short Circuit Output Current (Minus)	$I_{OS(-)}$	3011	4(f)	I_{OS}	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = +15V$ Note 2	9.0	45	mA
40 to 41	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_{17} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = -15V$, $R_L = 2.0k\Omega$	50	-	V/mV
42 to 43	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{18} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = +15V$, $R_L = 2.0k\Omega$	50	-	V/mV
44 to 45	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_{19} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = -2.0V$, $R_L = 2.0k\Omega$	10	-	V/mV
46 to 47	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{20} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = +2.0V$, $R_L = 2.0k\Omega$	10	-	V/mV
48 to 49	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(h)	E_{21} (V)	$+V_{CC} = 10V$, $-V_{CC} = -20V$ $V_{IN} = 0V$	-50	+50	µV/V
50 to 51	Power Supply Rejection Ratio (Minus)	-PSRR	4003	4(h)	E_{22} (V)	$+V_{CC} = 20V$, $-V_{CC} = -10V$ $V_{IN} = 0V$	-50	+50	µV/V
52 to 53	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{23} (V)	$+V_{CC} = 35V$, $-V_{CC} = -5.0V$ $V_{IN} = -15V$	70	-	dB
54 to 55	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{24} (V)	$+V_{CC} = 5.0V$, $-V_{CC} = -35V$ $V_{IN} = 15V$	70	-	dB
56 to 57	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{25} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = -20V$, $R_L = 10k\Omega$	16	-	V
58 to 59	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{26} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = +20V$, $R_L = 10k\Omega$	-	-16	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits		Unit
							Min	Max	
60 to 61	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{27} (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $V_{IN}=-20V$, $R_L=2.0k\Omega$	15	-	V
62 to 63	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{28} (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $V_{IN}=+20V$, $R_L=2.0k\Omega$	-	-15	V

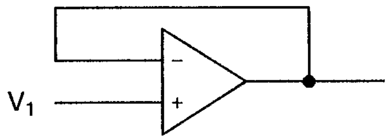
NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Test Conditions (Note 1)	Limits Min	Limits Max	Unit
64 to 65	Slew Rate (Plus)	SR(+)	4002	4(j)	$+V_{CC} = \pm 20V$ $V_{IN} = -5.0V$ to $+5.0V$ square $R_L = 2.0k\Omega$ Note 3	0.2	-	V/µs
66 to 67	Slew Rate (Minus)	SR(−)	4002	4(j)	$+V_{CC} = \pm 20V$ $V_{IN} = -5.0V$ to $+5.0V$ square $R_L = 2.0k\Omega$ Note 3	0.2	-	V/µs
68 to 69	RiseTime	RT	4002	4(j)	$V_{CC} = \pm 20V$, $V_{IN} = 50mV$ $R_L = 2.0k\Omega$ Note 3	-	1.0	µs
70 to 71	Overshoot	OS	4002	4(j)	$V_{CC} = \pm 20V$, $V_{IN} = 50mV$ $R_L = 2.0k\Omega$ Note 3	-	30	%

NOTES

1. Each amplifier shall be tested separately. The amplifier not under test shall be either maintained in a V_{IO} configuration such that the inputs are at the same common mode voltage as the D.U.T., or shall be maintained in the following configuration where V_1 is midway between $+V_{CC}$ and $-V_{CC}$:-



For a.c. parameters the positive input shall be connected to ground.

2. The duration of measurement of I_{OS} shall be $\leq 25ms$.
3. Sample Test Inspection Level = II, AQL = 2.5%.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits		Unit
							Min	Max	
1 to 2	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $V_{IN} = -15V$	-	6.0	mV
3 to 4	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $V_{IN} = 15V$	-	6.0	mV
5 to 6	Input Offset Voltage	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = 0V$	-	6.0	mV
7 to 8	Input Offset Voltage	V_{IO4}	4001	4(a)	E_4 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = 0V$	-	6.0	mV
9 to 10	Input Offset Current	I_{IO1}	4001	4(b)	E_5 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	500	nA
11 to 12	Input Offset Current	I_{IO2}	4001	4(b)	E_6 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	500	nA
13 to 14	Input Offset Current	I_{IO3}	4001	4(b)	E_7 (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA
15 to 16	Input Offset Current	I_{IO4}	4001	4(b)	E_8 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA
17 to 18	Input (Plus) Bias Current	I_{+IB1}	4001	4(c)	E_9 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	1.5	µA
19 to 20	Input (Plus) Bias Current	I_{+IB2}	4001	4(c)	E_{10} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	1.5	µA
21 to 22	Input (Plus) Bias Current	I_{+IB3}	4001	4(c)	E_{11} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA
23 to 24	Input (Plus) Bias Current	I_{+IB4}	4001	4(c)	E_{12} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA
25 to 26	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_{13} (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	1.5	µA
27 to 28	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_{14} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	1.5	µA
29 to 30	Input (Minus) Bias Current	I_{-IB3}	4001	4(d)	E_{15} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA
31 to 32	Input (Minus) Bias Current	I_{-IB4}	4001	4(d)	E_{16} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA

NOTES: See Page 23.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits		Unit
							Min	Max	
33	Power Supply Current Variants 03, 04, 07, 08, 11 and 12	$I_{CC(-)1}$	4005	4(e)	I_{CC1}	$+V_{CC} = +15V$, $-V_{CC} = -15V$	-	5.0	mA
34 to 35	Power Supply Current Variants 01, 02, 05, 06, 09, 10 and 13	$I_{CC(-)2}$	4005	4(e)	I_{CC2}	$+V_{CC} = +15V$, $-V_{CC} = -15V$	-	2.5	mA
36 to 37	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = -15V$ Note 2	−45	−9.0	mA
38 to 39	Short Circuit Output Current (Minus)	$I_{OS(-)}$	3011	4(f)	I_{OS}	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = +15V$ Note 2	9.0	45	mA
40 to 41	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_{17} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = -15V$, $R_L = 2.0k\Omega$	25	-	V/mV
42 to 43	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{18} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = +15V$, $R_L = 2.0k\Omega$	25	-	V/mV
44 to 45	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_{19} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = -2.0V$, $R_L = 2.0k\Omega$	10	-	V/mV
46 to 47	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{20} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = +2.0V$, $R_L = 2.0k\Omega$	10	-	V/mV
48 to 49	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(h)	E_{21} (V)	$+V_{CC} = 10V$, $-V_{CC} = -20V$ $V_{IN} = 0V$	−100	+100	μV/V
50 to 51	Power Supply Rejection Ratio (Minus)	−PSRR	4003	4(h)	E_{22} (V)	$+V_{CC} = 20V$, $-V_{CC} = -10V$ $V_{IN} = 0V$	−100	+100	μV/V
52 to 53	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{23} (V)	$+V_{CC} = 35V$, $-V_{CC} = -5.0V$ $V_{IN} = -15V$	70	-	dB
54 to 55	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{24} (V)	$+V_{CC} = 5.0V$, $-V_{CC} = -35V$ $V_{IN} = 15V$	70	-	dB
56 to 57	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{25} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = -20V$, $R_L = 10k\Omega$	16	-	V
58 to 59	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{26} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = +20V$, $R_L = 10k\Omega$	-	−16	V

NOTES: See Page 23.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits		Unit
							Min	Max	
60 to 61	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{27} (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $V_{IN}=-20V$, $R_L=2.0k\Omega$	15	-	V
62 to 63	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{28} (V)	$+V_{CC}=20V$, $-V_{CC}=-20V$ $V_{IN}=+20V$, $R_L=2.0k\Omega$	-	−15	V

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits		Unit
							Min	Max	
1 to 2	Input Offset Voltage	V_{IO1}	4001	4(a)	E_1 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $V_{IN} = -15V$	-	6.0	mV
3 to 4	Input Offset Voltage	V_{IO2}	4001	4(a)	E_2 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $V_{IN} = 15V$	-	6.0	mV
5 to 6	Input Offset Voltage	V_{IO3}	4001	4(a)	E_3 (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = 0V$	-	6.0	mV
7 to 8	Input Offset Voltage	V_{IO4}	4001	4(a)	E_4 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = 0V$	-	6.0	mV
9 to 10	Input Offset Current	I_{IO1}	4001	4(b)	E_5 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	500	nA
11 to 12	Input Offset Current	I_{IO2}	4001	4(b)	E_6 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	500	nA
13 to 14	Input Offset Current	I_{IO3}	4001	4(b)	E_7 (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA
15 to 16	Input Offset Current	I_{IO4}	4001	4(b)	E_8 (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	500	nA
17 to 18	Input (Plus) Bias Current	I_{+IB1}	4001	4(c)	E_9 (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	1.5	µA
19 to 20	Input (Plus) Bias Current	I_{+IB2}	4001	4(c)	E_{10} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	1.5	µA
21 to 22	Input (Plus) Bias Current	I_{+IB3}	4001	4(c)	E_{11} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA
23 to 24	Input (Plus) Bias Current	I_{+IB4}	4001	4(c)	E_{12} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA
25 to 26	Input (Minus) Bias Current	I_{-IB1}	4001	4(d)	E_{13} (V)	$+V_{CC} = +35V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = -15V$	-	1.5	µA
27 to 28	Input (Minus) Bias Current	I_{-IB2}	4001	4(d)	E_{14} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -35V$ $R_S = 20k\Omega$, $V_{IN} = 15V$	-	1.5	µA
29 to 30	Input (Minus) Bias Current	I_{-IB3}	4001	4(d)	E_{15} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA
31 to 32	Input (Minus) Bias Current	I_{-IB4}	4001	4(d)	E_{16} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $R_S = 20k\Omega$, $V_{IN} = 0V$	-	1.5	µA

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits Min	Limits Max	Unit
33	Power Supply Current Variants 03, 04, 07, 08, 11 and 12	$I_{CC(-)1}$	4005	4(e)	I_{CC1}	$+V_{CC} = +15V$, $-V_{CC} = -15V$	-	7.0	mA
34 to 35	Power Supply Current Variants 01, 02, 05, 06, 09, 10 and 13	$I_{CC(-)2}$	4005	4(e)	I_{CC2}	$+V_{CC} = +15V$, $-V_{CC} = -15V$	-	3.5	mA
36 to 37	Short Circuit Output Current (Plus)	$I_{OS(+)}$	3011	4(f)	I_{OS}	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = -15V$ Note 2	−50	−9.0	mA
38 to 39	Short Circuit Output Current (Minus)	$I_{OS(-)}$	3011	4(f)	I_{OS}	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = +15V$ Note 2	9.0	50	mA
40 to 41	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_{17} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = -15V$, $R_L = 2.0k\Omega$	25	-	V/mV
42 to 43	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{18} (V)	$+V_{CC} = +20V$, $-V_{CC} = -20V$ $V_{IN} = +15V$, $R_L = 2.0k\Omega$	25	-	V/mV
44 to 45	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	E_{19} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = -2.0V$, $R_L = 2.0k\Omega$	10	-	V/mV
46 to 47	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	E_{20} (V)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ $V_{IN} = +2.0V$, $R_L = 2.0k\Omega$	10	-	V/mV
48 to 49	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(h)	E_{21} (V)	$+V_{CC} = 10V$, $-V_{CC} = -20V$ $V_{IN} = 0V$	−100	+100	µV/V
50 to 51	Power Supply Rejection Ratio (Minus)	−PSRR	4003	4(h)	E_{22} (V)	$+V_{CC} = 20V$, $-V_{CC} = -10V$ $V_{IN} = 0V$	−100	+100	µV/V
52 to 53	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{23} (V)	$+V_{CC} = 35V$, $-V_{CC} = -5.0V$ $V_{IN} = -15V$	70	-	dB
54 to 55	Common Mode Rejection Ratio	CMRR	4003	4(i)	E_{24} (V)	$+V_{CC} = 5.0V$, $-V_{CC} = -35V$ $V_{IN} = 15V$	70	-	dB
56 to 57	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{25} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = -20V$, $R_L = 10k\Omega$	16	-	V
58 to 59	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{26} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = +20V$, $R_L = 10k\Omega$	-	−16	V

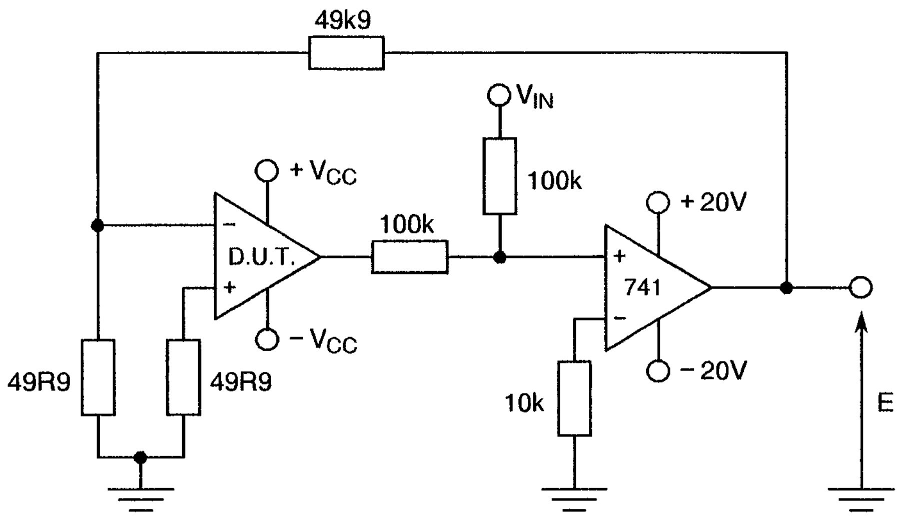
NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, − 55(+ 5 − 0) °C (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD 883	Test Fig.	Meas'd Value	Test Conditions (Note 1)	Limits		Unit
							Min	Max	
60 to 61	Output Voltage Swing (Plus)	$V_{OUT(+)}$	4004	4(g)	E_{27} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = -20V$, $R_L = 2.0k\Omega$	15	-	V
62 to 63	Output Voltage Swing (Minus)	$V_{OUT(-)}$	4004	4(g)	E_{28} (V)	$+V_{CC} = 20V$, $-V_{CC} = -20V$ $V_{IN} = +20V$, $R_L = 2.0k\Omega$	-	−15	V

NOTES: See Page 23.

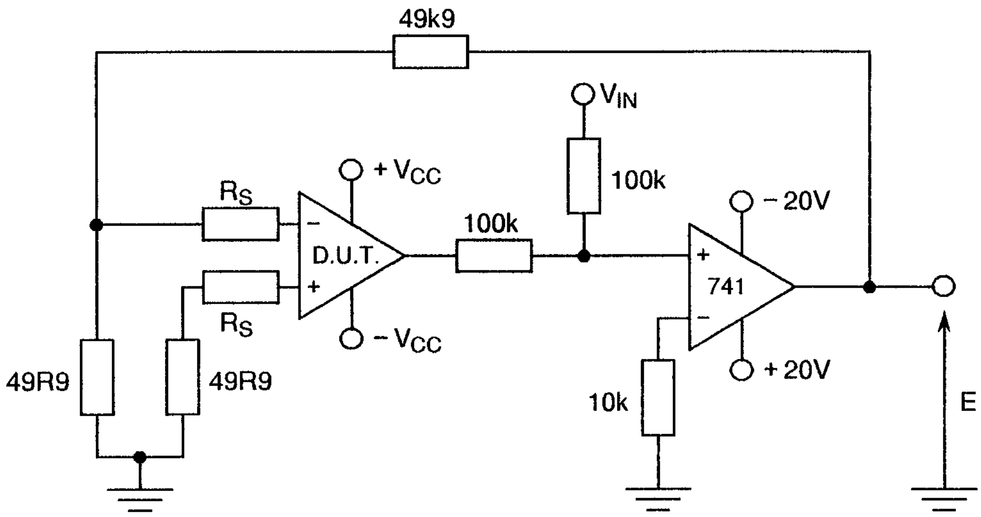
FIGURE 4(a) - INPUT OFFSET VOLTAGE



V_{IO1} (mV) = E_1 (V), V_{IO2} (mV) = E_2 (V), V_{IO3} (mV) = E_3 (V), V_{IO4} (mV) = E_4 (V).

NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(b) - INPUT OFFSET CURRENT

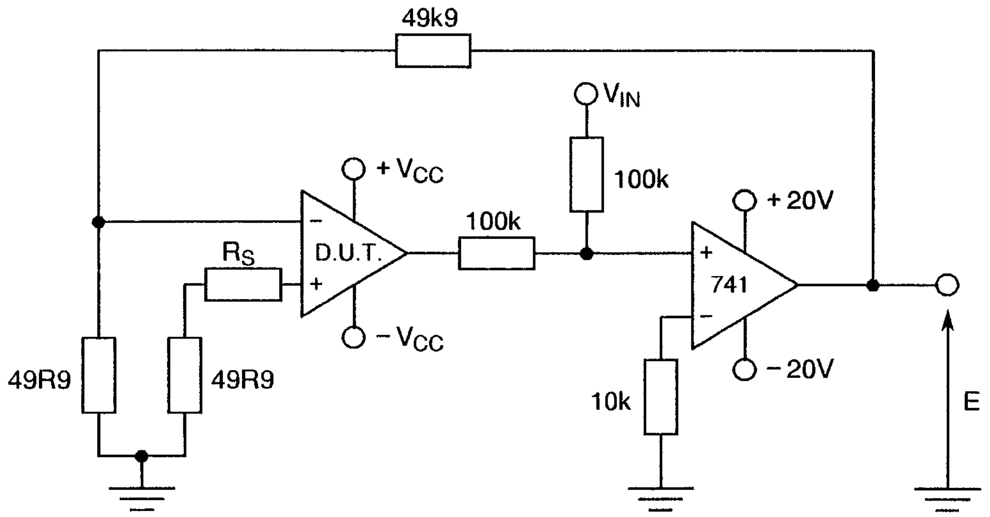


$$I_{IO1}\ (nA) = \frac{(E_1\ (V) - E_5\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{IO2}\ (nA) = \frac{(E_2\ (V) - E_6\ (V))\ 10^6}{R_S\ (k\Omega)}$$

$$I_{IO3}\ (nA) = \frac{(E_3\ (V) - E_7\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{IO4}\ (nA) = \frac{(E_4\ (V) - E_8\ (V))\ 10^6}{R_S\ (k\Omega)}$$

NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(c) - INPUT (PLUS) BIAS CURRENT

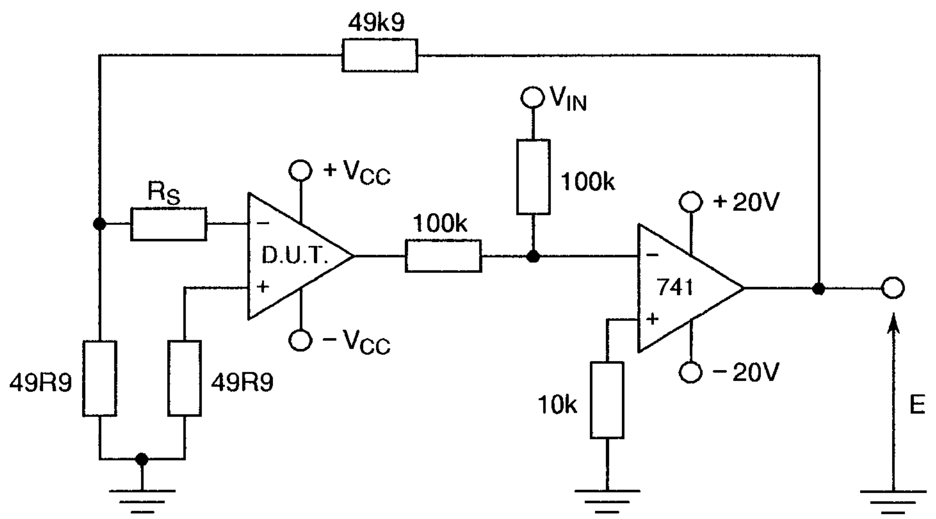


$$I_{+IB1}\ (nA) = \frac{(E_1\ (V) - E_9\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{+IB2}\ (nA) = \frac{(E_2\ (V) - E_{10}\ (V))\ 10^6}{R_S\ (k\Omega)}$$

$$I_{+IB3}\ (nA) = \frac{(E_3\ (V) - E_{11}\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{+IB4}\ (nA) = \frac{(E_4\ (V) - E_{12}\ (V))\ 10^6}{R_S\ (k\Omega)}$$

NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(d) - INPUT (MINUS) BIAS CURRENT

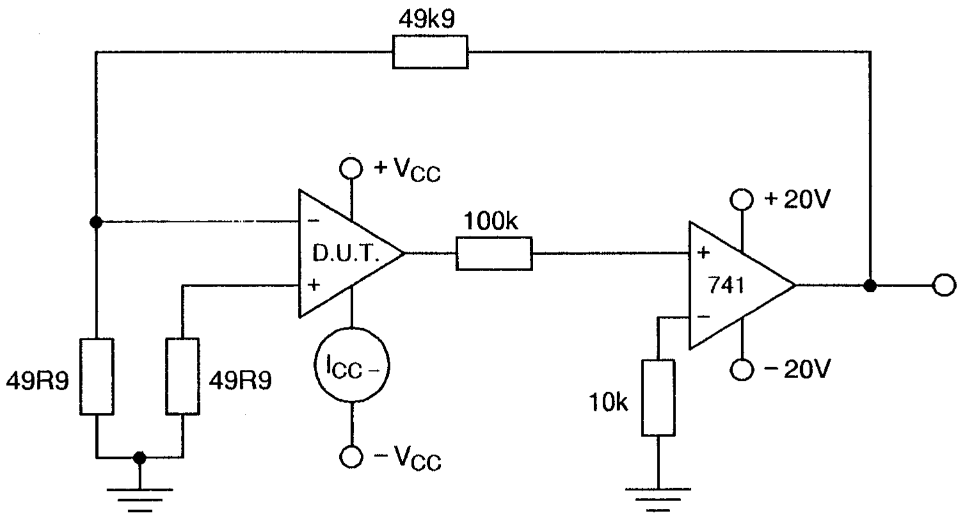


$$I_{-IB1}\ (nA) = \frac{(E_{13}\ (V) - E_1\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{-IB2}\ (nA) = \frac{(E_{14}\ (V) - E_2\ (V))\ 10^6}{R_S\ (k\Omega)}$$

$$I_{-IB3}\ (nA) = \frac{(E_{15}\ (V) - E_3\ (V))\ 10^6}{R_S\ (k\Omega)} \qquad I_{-IB4}\ (nA) = \frac{(E_{16}\ (V) - E_4\ (V))\ 10^6}{R_S\ (k\Omega)}$$

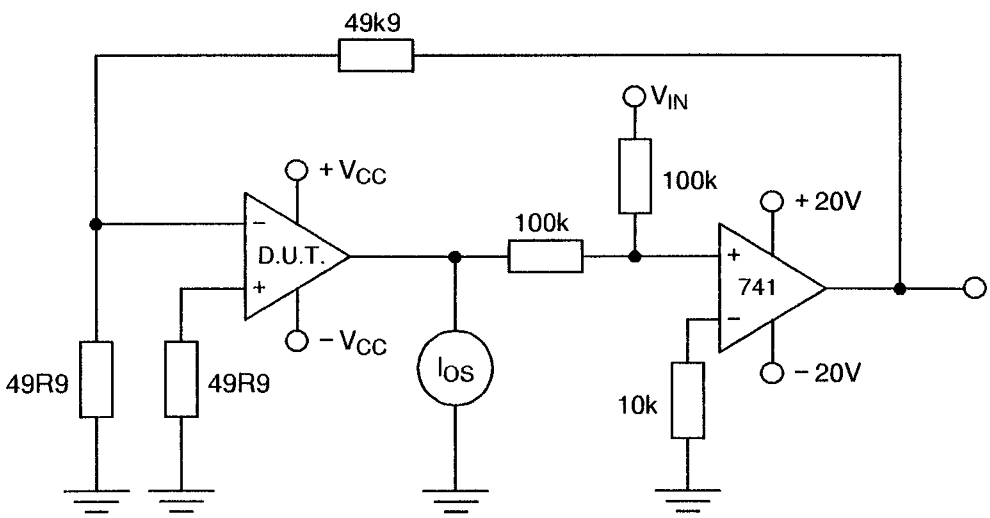
NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(e) - SUPPLY CURRENT



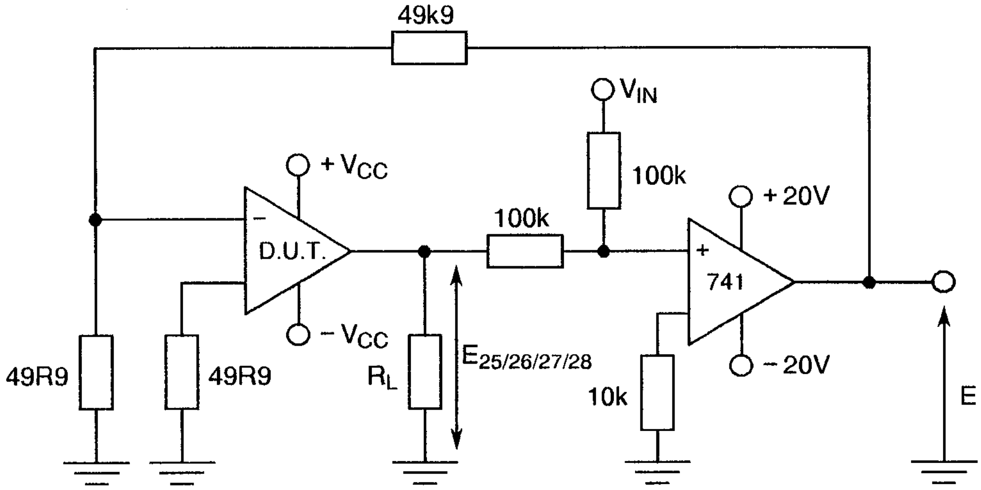
NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(f) - SHORT CIRCUIT OUTPUT CURRENT



NOTES
1. All resistors to be 0.1% tolerance.

FIGURE 4(g) - OUTPUT VOLTAGE SWING
- OPEN LOOP VOLTAGE GAIN



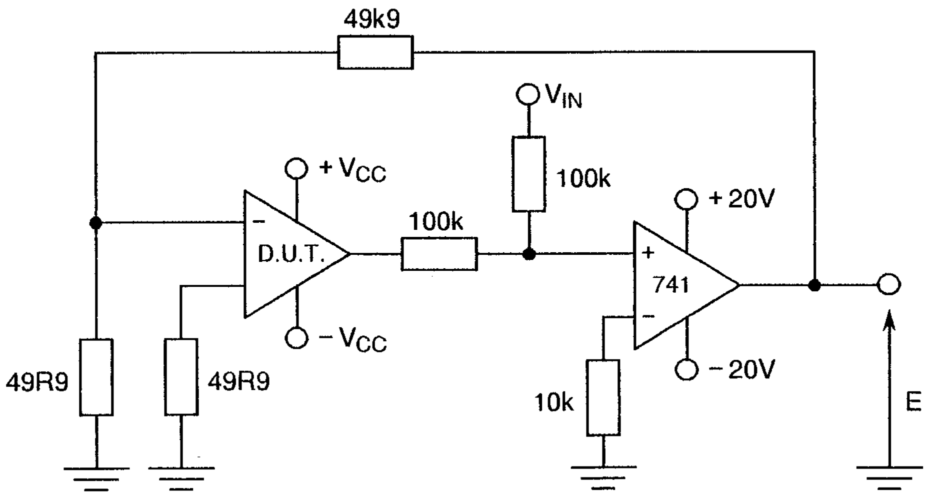
1. $V_{OUT} = (E_{25}, E_{26}, E_{27}, E_{28})$ V

2. $+A_{VS} = \frac{15}{E_3 - E_{17}}$, $+A_{VS} = \frac{2}{E_4 - E_{19}}$

3. $-A_{VS} = \frac{15}{E_{18} - E_3}$, $-A_{VS} = \frac{2}{E_{20} - E_4}$

NOTES
1. E_{25}, E_{26}, E_{27}, E_{28} are in Volts.
2. All resistors to be 0.1% tolerance.

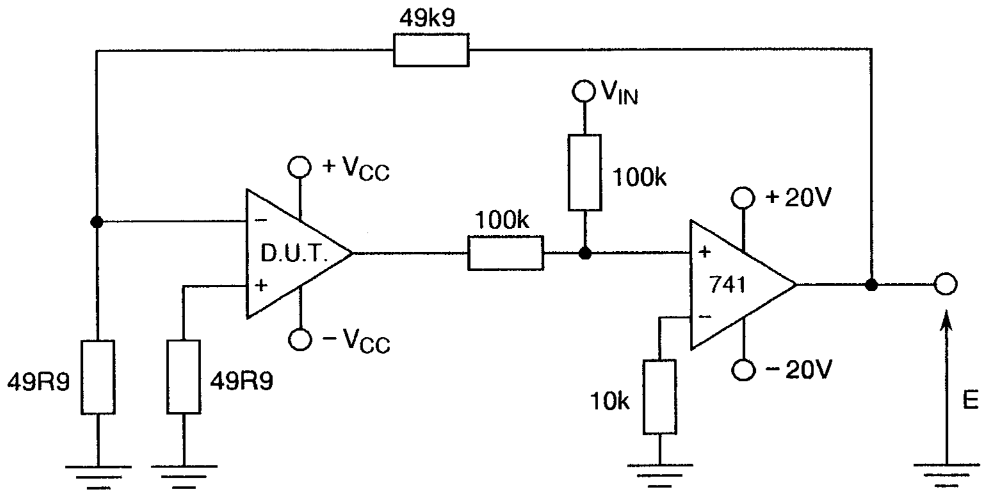
FIGURE 4(h) - POWER SUPPLY REJECTION RATIO



$+PSRR\ (\mu V/V) = (E_3\ (V) - E_{21}\ (V))\ 10^2$, $-PSRR\ (\mu V/V) = (E_3\ (V) - E_{22}\ (V))\ 10^2$

NOTES
1. All resistors to be 0.1% tolerance.
2. E is measured to four digits accuracy.

FIGURE 4(i) - COMMON MODE REJECTION RATIO

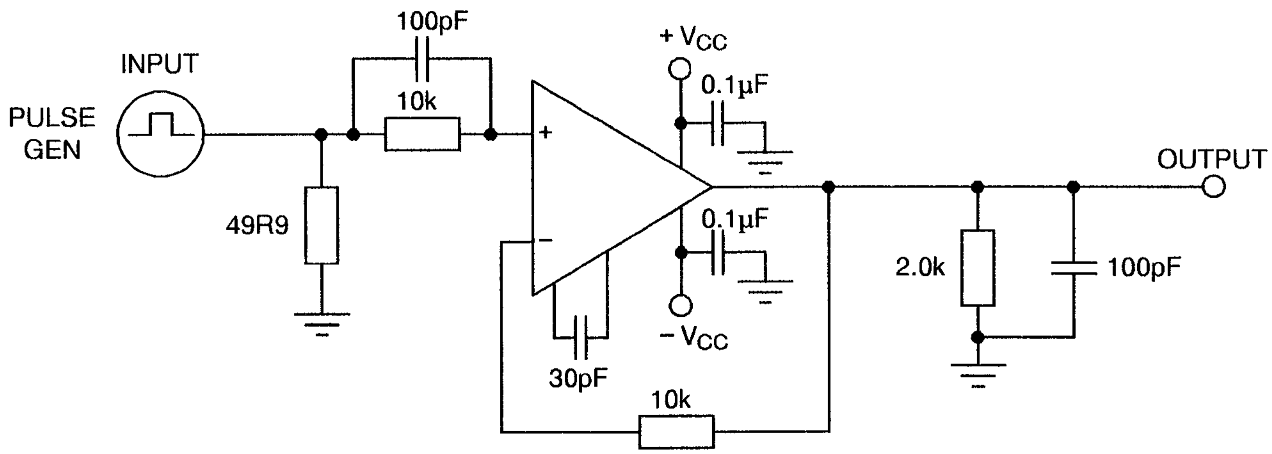


$$CMRR\ (dB) = 20\ LOG\ \frac{30.10^3}{E_{23}\ (V) - E_{24}\ (V)}$$

NOTES

1. Resistors of 49R9Ω at inputs shall be of 0.01% tolerance matched to 0.001%. Remaining resistors shall be of 0.1% tolerance.

FIGURE 4(j) - DYNAMIC TEST MEASUREMENT CIRCUIT



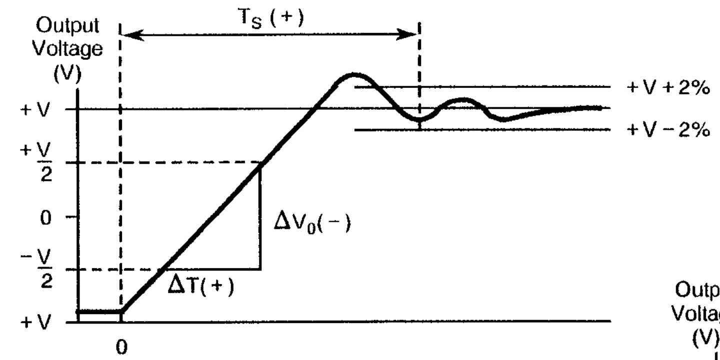
NOTES

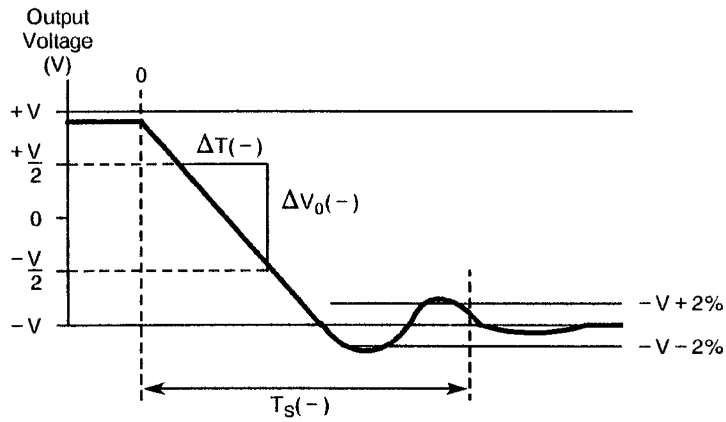
1. Pulse Generator:
   - Rise time ≤ 10ns
   - Repetition rate 1.0kHz (max.)
   - Pulse voltage: −5.0V to +5.0V for slew rate measurement
   - Pulse voltage: 50mV for rise time and overshoot measurement

$$SR = \left| \frac{\Delta V_0}{\Delta T} \right| \text{ (V/μs)}$$

$$RT = t \text{ (μs)}$$

$$OS = \frac{\Delta V}{50} \text{ 100(\%)}$$





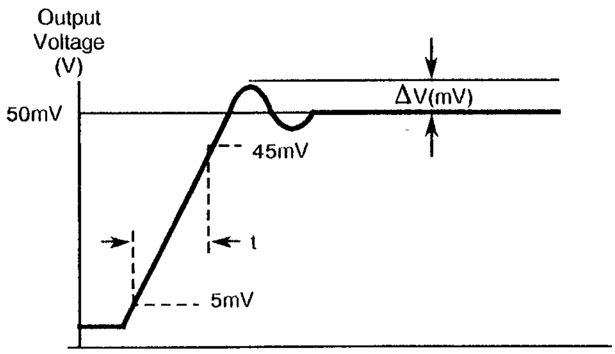


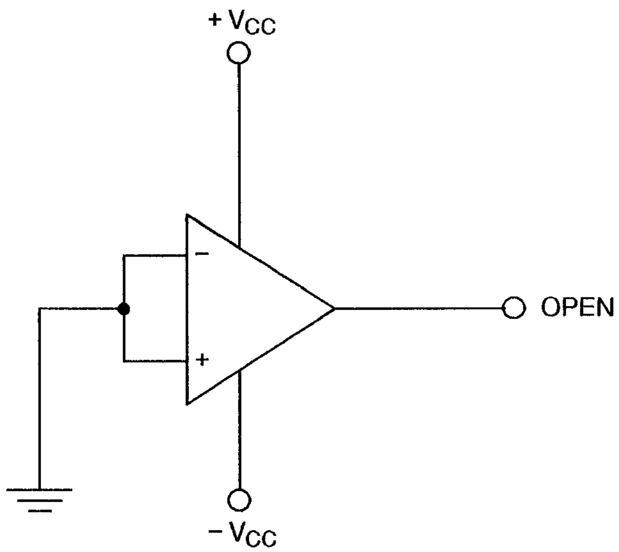
TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
5 to 6	Input Offset Voltage Change	V_{IO3}	As per Table 2	As per Table 2	± 1.0	mV
13 to 14	Input Offset Current Change	I_{IO3}	As per Table 2	As per Table 2	± 20	nA
21 to 22	Input (Plus) Bias Current Change	I_{+IB3}	As per Table 2	As per Table 2	± 50	nA
29 to 30	Input (Minus) Bias Current Change	I_{-IB3}	As per Table 2	As per Table 2	± 50	nA

TABLE 5 - CONDITIONS FOR BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125 ± 5	°C
2	Supply Voltage	V_{CC}	± 20	V

FIGURE 5 - BURN-IN CIRCUIT



4.8 ENVIRONMENTAL AND ENDURANCE TESTS

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
5 to 6	Input Offset Voltage	V_{IO3}	As per Table 2	As per Table 2	-	5.0	mV
13 to 14	Input Offset Current	I_{IO3}	As per Table 2	As per Table 2	-	200	nA
21 to 22	Input (Plus) Bias Current	I_{+IB3}	As per Table 2	As per Table 2	-	500	nA
33	Power Supply Current Variants 03, 04, 07, 08, 11 and 12	$I_{CC(-)1}$	As per Table 2	As per Table 2	-	5.6	mA
34 to 35	Power Supply Current Variants 01, 02, 05, 06, 09, 10 and 13	$I_{CC(-)2}$	As per Table 2	As per Table 2	-	2.8	mA
40 to 41	Open Loop Voltage Gain	$+A_{VS}$	As per Table 2	As per Table 2	50	-	V/mV