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Pages 1 to 69

INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS 8-BIT MICRO-CONTROLLER,

BASED ON TYPE 80C31

ESA/SCC Detail Specification No. 9521/001

space components
coordination group

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APPENDICES (Applicable to specific Manufacturers only)

None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, CMOS 8-Bit Micro-Controller, based on Type 80C31. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE/INSTRUCTION SET

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 500Volts.

1.11 INPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	DIL	2(a)	D2
02	DIL	2(b)	G3

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	−0.5 to +6.5	V	-
2	Input Voltage	V_{IN}	−0.5 to V_{DD} + 0.5	V	Note 1
3	DC Input Current	$\pm I_{IN}$	1.0	mA	-
4	DC Output Current	$\pm I_O$	80	mA	Note 2
5	Device Dissipation	P_D	200	mWdc	Per Package
6	Clock Frequency	f	0 to 12	MHz	-
7	Operating Temperature Range	T_{op}	−55 to +125	°C	-
8	Storage Temperature Range	T_{stg}	−65 to +175	°C	-
9	Soldering Temperature	T_{sol}	+300	°C	Note 3
10	Junction Temperature	T_J	+150	°C	-
11	Thermal Resistance	$R_{TH(J-A)}$	30	°C/W	-

NOTES

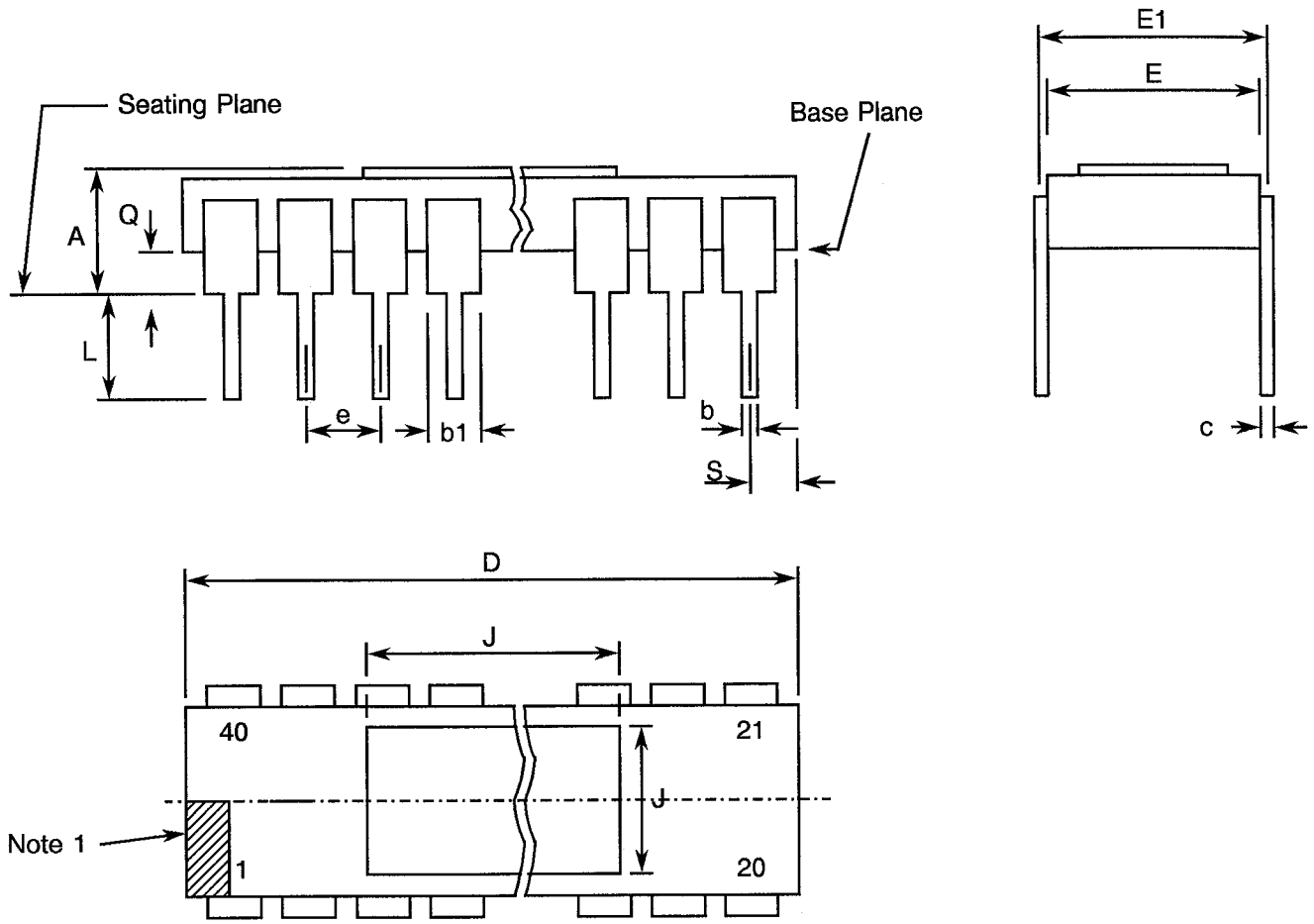
1. V_{DD} + 0.5V should not exceed + 6.5V.
2. The maximum output current of any single output.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 40 PIN

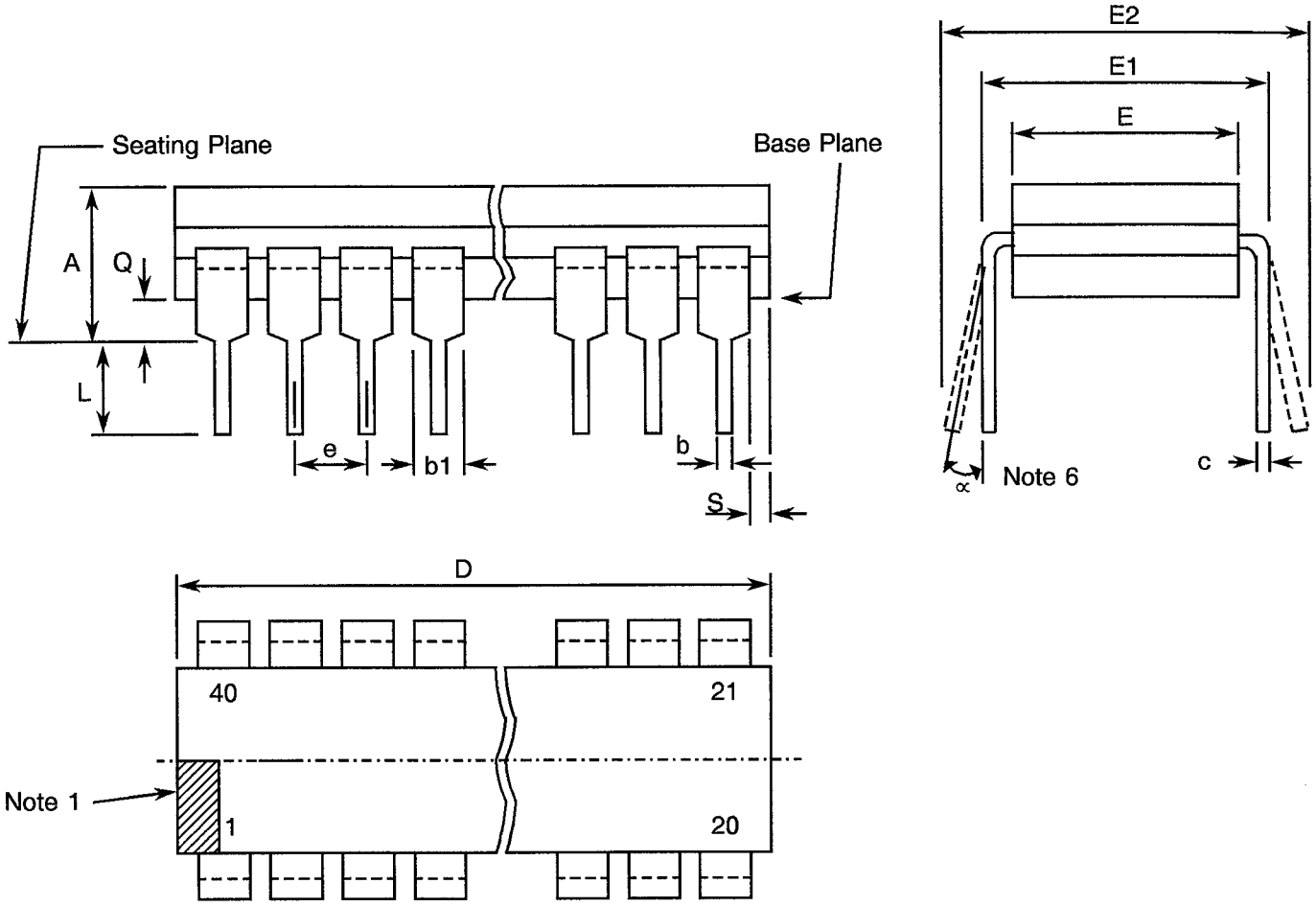


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	2.20	4.80	
b	0.38	0.58	3
b1	0.97	1.52	3
c	0.20	0.38	
D	50.30	51.58	
E	14.74	15.49	
E1	15.12	15.87	
e	2.54 TYP		4
J	10.80 TYP		
L	3.18	4.44	3
Q	0.51	1.77	2
S	0.77	1.65	5

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 40 PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	4.07	5.58	
b	0.38	0.51	
b1	1.15	1.78	
c	0.20	0.38	
D	52.00	53.87	
E	12.95	14.73	
E1	15.41	15.62	
E2	-	17.78	
e	2.54 BSC		4
L	3.17	5.08	3
Q	0.51	1.78	2
S	0.25	-	5
∝	0°	15°	6

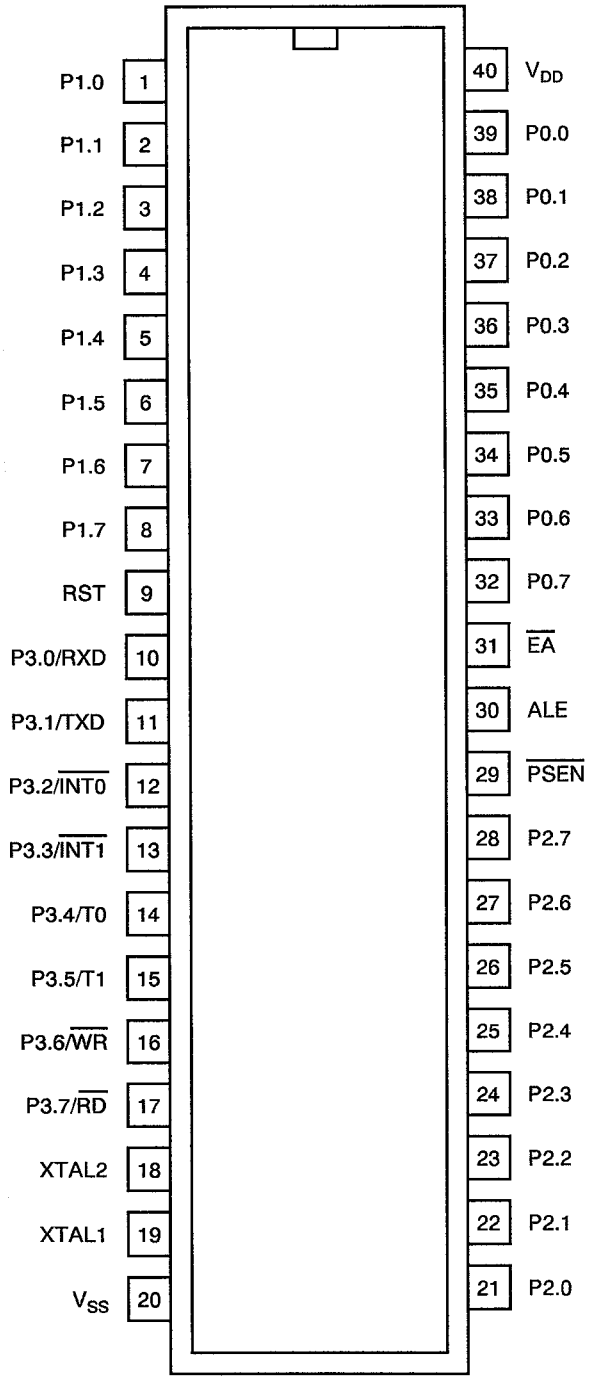
NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(b) INCLUSIVE

1. Index area; a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. All leads or terminals.
4. 38 spaces.
5. All 4 corners.
6. Lead centre when $\propto$ is 0°.

FIGURE 3(a) - PIN ASSIGNMENT



TOP VIEW

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET

INSTRUCTIONS IN HEXADECIMAL ORDER

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
00	1	NOP	
01	2	AJMP	code addr
02	3	LJMP	code addr
03	1	RR	A
04	1	INC	A
05	2	INC	data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	bit addr. code addr
11	2	ACALL	code addr
12	3	LCALL	code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	bit addr. code addr
21	2	AJMP	code addr
22	1	RET	
23	1	RL	A
24	1	ADD	A.data
25	1	ADD	A.data addr
26	1	ADD	A.@R0
27	1	ADD	A.@R1
28	1	ADD	A.R0
29	1	ADD	A.R1
2A	1	ADD	A.R2
2B	1	ADD	A.R3
2C	1	ADD	A.R4

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
2D	1	ADD	A.R5
2E	1	ADD	A.R6
2F	1	ADD	A.R7
30	3	JNB	bit addr. code addr
31	2	ACALL	code addr
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A.#data
35	2	ADDC	A.data addr
36	1	ADDC	A.@R0
37	1	ADDC	A.@R1
38	1	ADDC	A.R0
39	1	ADDC	A.R1
3A	1	ADDC	A.R2
3B	1	ADDC	A.R3
3C	1	ADDC	A.R4
3D	1	ADDC	A.R5
3E	1	ADDC	A.R6
3F	1	ADDC	A.R7
40	2	JC	code addr
41	2	AJMP	code addr
42	2	ORL	data addr.A
43	3	ORL	data addr. #data
44	2	ORL	A.#data
45	2	ORL	A.data addr
46	1	ORL	A.@R0
47	1	ORL	A.@R1
48	1	ORL	A.R0
49	1	ORL	A.R1
4A	1	ORL	A.R2
4B	1	ORL	A.R3
4C	1	ORL	A.R4
4D	1	ORL	A.R5
4E	1	ORL	A.R6
4F	1	ORL	A.R7
50	2	JNC	code addr
51	2	ACALL	code addr
52	2	ANL	code addr.A
53	3	ANL	data addr. #data
54	2	ANL	A.#data
55	2	ANL	A.data addr
56	1	ANL	A.@R0
57	1	ANL	A.@R1
58	1	ANL	A.R0
59	1	ANL	A.R1

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

INSTRUCTIONS IN HEXADECIMAL ORDER (CONTINUED)

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
5A	1	ANL	A.R2
5B	1	ANL	A.R3
5C	1	ANL	A.R4
5D	1	ANL	A.R5
5E	1	ANL	A.R6
5F	1	ANL	A.R7
60	2	JZ	code addr
61	2	AJMP	code addr
62	2	XRL	code addr.A
63	3	XRL	data addr. #data
64	2	XRL	A.#data
65	2	XRL	A.data addr
66	1	XRL	A.@R0
67	1	XRL	A.@R1
68	1	XRL	A.R0
69	1	XRL	A.R1
6A	1	XRL	A.R2
6B	1	XRL	A.R3
6C	1	XRL	A.R4
6D	1	XRL	A.R5
6E	1	XRL	A.R6
6F	1	XRL	A.R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	MOV	C.bit addr
73	1	JMP	@A + DPTR
74	2	MOV	A.#data
75	3	MOV	data addr. #data
76	2	MOV	@R0.#data
77	2	MOV	@R1.#data
78	2	MOV	R0.#data
79	2	MOV	R1.#data
7A	2	MOV	R2.#data
7B	2	MOV	R3.#data
7C	2	MOV	R4.#data
7D	2	MOV	R5.#data
7E	2	MOV	R6.#data
7F	2	MOV	R7.#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C.bit addr
83	1	MOVC	A.@A + PC
84	1	DIV	AB
85	3	MOV	data addr

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
86	2	MOV	data addr.@R0
87	2	MOV	data addr.@R1
88	2	MOV	data addr.R0
89	2	MOV	data addr.R1
8A	2	MOV	data addr.R2
8B	2	MOV	data addr.R3
8C	2	MOV	data addr.R4
8D	2	MOV	data addr.R5
8E	2	MOV	data addr.R6
8F	2	MOV	data addr.R7
90	3	MOV	DPTR.#data
91	2	ACALL	code addr
92	2	MOV	bit addr.C
93	1	MOVC	A.@A + DPTR
94	2	SUBB	A.#data
95	2	SUBB	A.data addr
96	1	SUBB	A.@R0
97	1	SUBB	A.@R1
98	1	SUBB	A.R0
99	1	SUBB	A.R1
9A	1	SUBB	A.R2
9B	1	SUBB	A.R3
9C	1	SUBB	A.R4
9D	1	SUBB	A.R5
9E	1	SUBB	A.R6
9F	1	SUBB	A.R7
A0	2	ORL	C.bit addr
A1	2	AJMP	code addr
A2	2	MOV	C.bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0.data addr
A7	2	MOV	@R1.data addr
A8	2	MOV	R0.data addr
A9	2	MOV	R1.data addr
AA	2	MOV	R2.data addr
AB	2	MOV	R3.data addr
AC	2	MOV	R4.data addr
AD	2	MOV	R5.data addr
AE	2	MOV	R6.data addr
AF	2	MOV	R7.data addr
B0	2	ANL	C.bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A.#data. code addr

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

INSTRUCTIONS IN HEXADECIMAL ORDER (CONTINUED)

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
B5	3	CJNE	A.data addr. code addr
B6	3	CJNE	@R0.#data. code addr
B7	3	CJNE	@R1.#data. code addr
B8	3	CJNE	R0.#data. code addr
B9	3	CJNE	R1.#data. code addr
BA	3	CJNE	R2.#data. code addr
BB	3	CJNE	R3.#data. code addr
BC	3	CJNE	R4.#data. code addr
BD	3	CJNE	R5.#data. code addr
BE	3	CJNE	R6.#data. code addr
BF	3	CJNE	R7.#data. code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A.data addr
C6	1	XCH	A.@R0
C7	1	XCH	A.@R1
C8	1	XCH	A.R0
C9	1	XCH	A.R1
CA	1	XCH	A.R2
CB	1	XCH	A.R3
CC	1	XCH	A.R4
CD	1	XCH	A.R5
CE	1	XCH	A.R6
CF	1	XCH	A.R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
D5	3	DJNZ	data addr. code addr
D6	1	XCHD	A.@R0
D7	1	XCHD	A.@R1
D8	2	DJNZ	R0.code addr
D9	2	DJNZ	R1.code addr
DA	2	DJNZ	R2.code addr
DB	2	DJNZ	R3.code addr
DC	2	DJNZ	R4.code addr
DD	2	DJNZ	R5.code addr
DE	3	DJNZ	R6.code addr
DF	2	DJNZ	R7.code addr
E0	1	MOVX	A.@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A.@R0
E3	1	MOVX	A.@R1
E4	1	CLR	A
E5	2	MOV	A.data addr
E6	1	MOV	A.@R0
E7	1	MOV	A.@R1
E8	1	MOV	A.R0
E9	1	MOV	A.R1
EA	1	MOV	A.R2
EB	1	MOV	A.R3
EC	1	MOV	A.R4
ED	1	MOV	A.R5
EE	1	MOV	A.R6
EF	1	MOV	A.R7
F0	1	MOVX	@DPRT.A
F1	2	ACALL	code addr
F2	1	MOVX	@R0.A
F3	1	MOVX	@R1.A
F4	1	CPL	A
F5	2	MOV	data addr.A
F6	1	MOV	@R0.A
F7	1	MOV	@R1.A
F8	1	MOV	R0.A
F9	1	MOV	R1.A
FA	1	MOV	R2.A
FB	1	MOV	R3.A
FC	1	MOV	R4.A
FD	1	MOV	R5.A
FE	1	MOV	R6.A
FF	1	MOV	R7.A

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

DESCRIPTION OF INSTRUCTIONS

ARITHMETIC OPERATIONS

Mnemonic		Description	Byte	Cyc
ADD	A.Rn	Add register to Accumulator	1	1
ADD	A.direct	Add direct byte to Accumulator	2	1
ADD	A.@Ri	Add indirect RAM to Accumulator	1	1
ADD	A.#data	Add immediate data to Accumulator	2	1
ADDC	A.Rn	Add register to Accumulator with Carry	1	1
ADDC	A.direct	Add direct byte to A with Carry Flag	2	1
ADDC	A.@Ri	Add indirect RAM to A with Carry Flag	1	1
ADDC	A.#data	Add immediate data to A with Carry Flag	2	1
SUBB	A.Rn	Subtract register from A with Borrow	1	1
SUBB	A.direct	Subtract direct byte from A with Borrow	2	1
SUBB	A.@Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB	A.#data	Subtract immediate data from A with Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

LOGIC OPERATIONS

ANL	A.Rn	AND register to Accumulator	1	1
ANL	A.direct	AND direct byte to Accumulator	2	1
ANL	A.@Ri	AND indirect RAM to Accumulator	1	1
ANL	A.#data	AND immediate data to Accumulator	2	1
ANL	direct.A	AND Accumulator to direct byte	2	1
ANL	direct.#data	AND immediate data to direct byte	3	2
ORL	A.Rn	OR register to Accumulator	1	1
ORL	A.direct	OR direct byte to Accumulator	2	1
ORL	A.@Ri	OR indirect RAM to Accumulator	1	1
ORL	A.#data	OR immediate data to Accumulator	2	1
ORL	direct.A	OR Accumulator to direct byte	2	1
ORL	direct.#data	OR immediate data to direct byte	3	2

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

DESCRIPTION OF INSTRUCTIONS (CONTINUED)

LOGIC OPERATIONS (CONT'D)

Mnemonic		Description	Byte	Cyc
XRL	A.Rn	Exclusive-OR register to Accumulator	1	1
XRL	A.direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A.@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A.#data	Exclusive-OR immediate data to A	2	1
XRL	direct.A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct.#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry Flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry Flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

DATA TRANSFER

Mnemonic		Description	Byte	Cyc
MOV	A.Rn	Move register to Accumulator	1	1
MOV	A.direct	Move direct byte to Accumulator	2	1
MOV	A.@Ri	Move indirect RAM to Accumulator	1	1
MOV	A.#data	Move immediate data to Accumulator	2	1
MOV	Rn.A	Move Accumulator to register	1	1
MOV	Rn. direct	Move direct byte to register	2	2
MOV	Rn.#data	Move immediate data to register	2	1
MOV	direct.A	Move Accumulator to direct byte	2	1
MOV	direct.Rn	Move register to direct byte	2	2
MOV	direct.direct	Move direct byte to direct byte	3	2
MOV	direct.@Ri	Move indirect RAM to direct byte	2	2
MOV	direct.#data	Move immediate data to direct byte	3	2
MOV	@Ri.A	Move Accumulator to indirect RAM	1	1
MOV	@Ri.direct	Move direct byte to indirect RAM	2	2
MOV	@Ri.#data	Move immediate data to indirect RAM	2	1
MOV	DPTR.#data 16	Load Data Pointer with a 16-bit constant	3	2
MOVC	A.@A + DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A.@A + PC	Move Code byte relative to PC to A	1	2
MOVX	A.@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A.@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri.A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTRA	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A.Rn	Exchange register with Accumulator	1	1
XCH	A.direct	Exchange direct byte with Accumulator	2	1
XCH	A.@Ri	Exchange indirect RAM with A	1	1
XCHD	A.@Ri	Exchange low-order nibble ind RAM with A	1	1

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

DESCRIPTION OF INSTRUCTIONS (CONTINUED)

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cyc
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	1	1
ANL	C.bit	AND direct bit to Carry flag	2	2
ANL	C./bit	AND complement of direct bit to Carry	2	2
ORL	C.bit	OR direct bit to Carry flag	2	2
ORL	C./bit	OR complement of direct bit to Carry	2	2
MOV	C.bit	Move direct bit to Carry flag	2	1
MOV	bit.C	Move Carry flag to direct bit	2	2

PROGRAMME AND MACHINE CONTROL

Mnemonic		Description	Byte	Cyc
ACALL	addr 11	Absolute Subroutine Call	2	2
LCALL	addr 16	Long Subroutine Call	3	2
RET		Return from Subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit.rel	Jump if direct Bit set	3	2
JNB	bit.rel	Jump if direct Bit not set	3	2
JCB	bit.rel	Jump if direct Bit is set and Clear bit	3	2
CJNE	A.direct.rel	Compare direct to A and Jump if not Equal	3	2
CJNE	A.#data.rel	Compare immed. to A and Jump if not Equal	3	2
CJNE	Rn.#data.rel	Compare immed. to reg and Jump if not Equal	3	2
CJNE	@Ri.#data.rel	Compare immed. to ind and Jump if not Equal	3	2
DJNZ	Rn.rel	Decrement register and Jump if not Zero	2	2
DJNZ	direct.rel	Decrement direct and Jump if not Zero	3	2
NOP		No operation	1	1

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

DESCRIPTION OF INSTRUCTIONS (CONTINUED)

NOTES

1. Notes on data processing modes:-

Rn	-	Working register R0-R7.
direct	-	128 internal RAM Locations, any I/O port control or status register.
@Ri	-	Indirect internal RAM location addressed by register R0 or R1.
#data	-	8-bit constant included in instruction.
#data 16	-	16-bit constant included as bytes 2 and 3 of instruction.
bit	-	128 software flags, any I/O pin, control or status bit.

2. Notes on programme addressing modes:-

addr 16	-	Destination address for LCALL and LJMP may be anywhere within the 64k programme memory address space.
addr 11	-	Destination address for ACALL and AJMP will be within the same 2k page of programme memory as the first byte of the following instruction.
rel	-	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 −128 bytes relative to first byte of the following instruction.

TIMING WAVEFORMS

EXTERNAL PROGRAMME MEMORY READ CYCLE

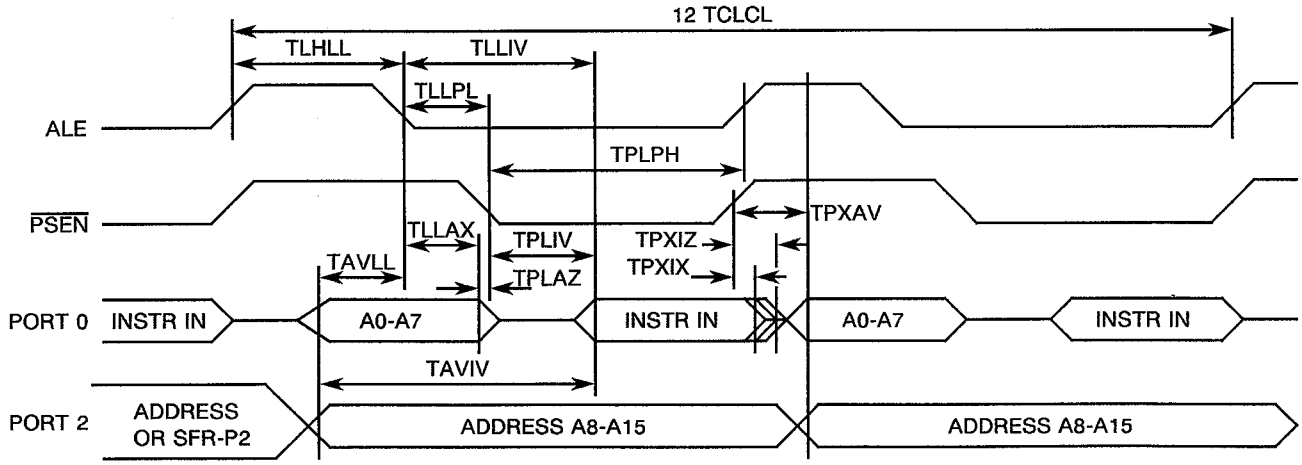
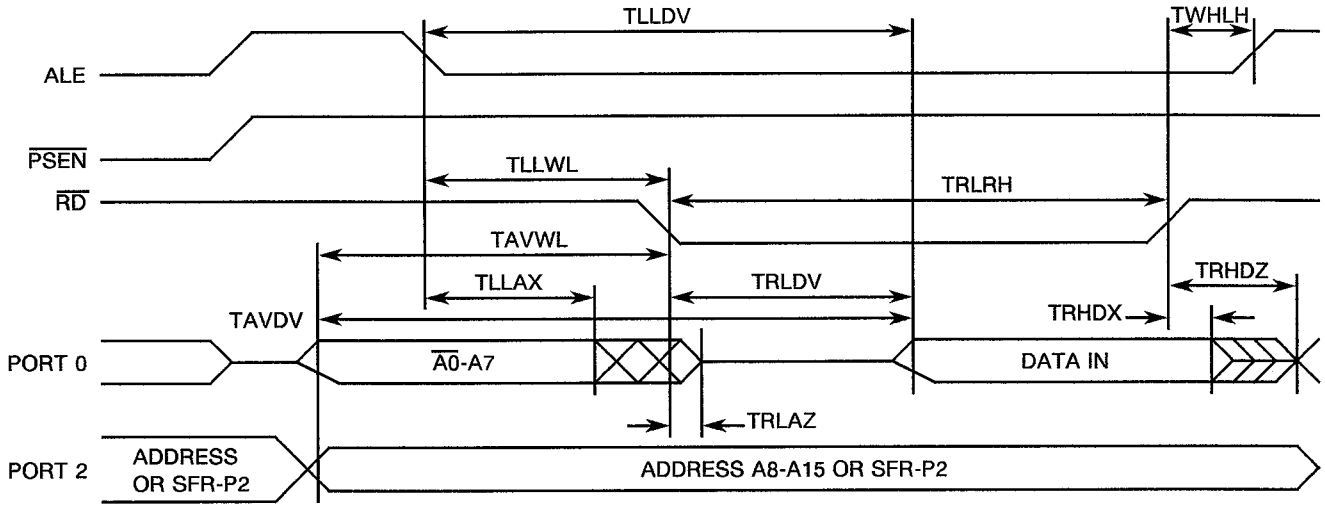


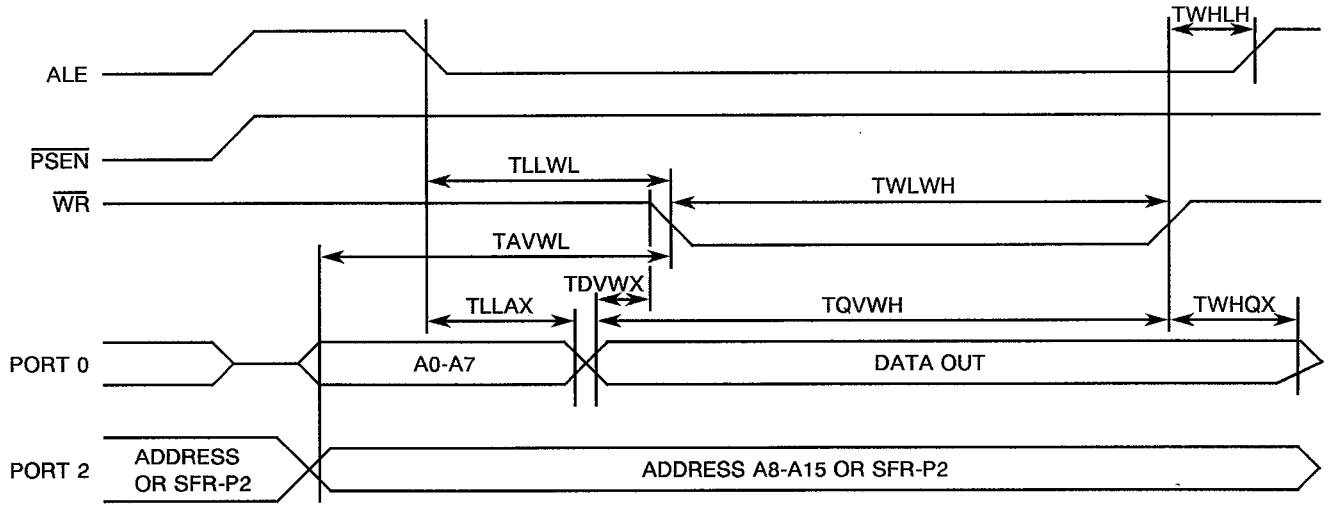
FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK WAVEFORMS

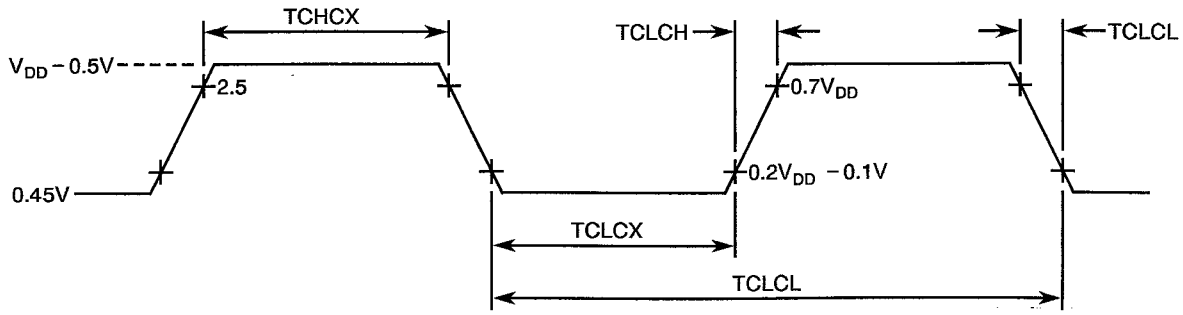
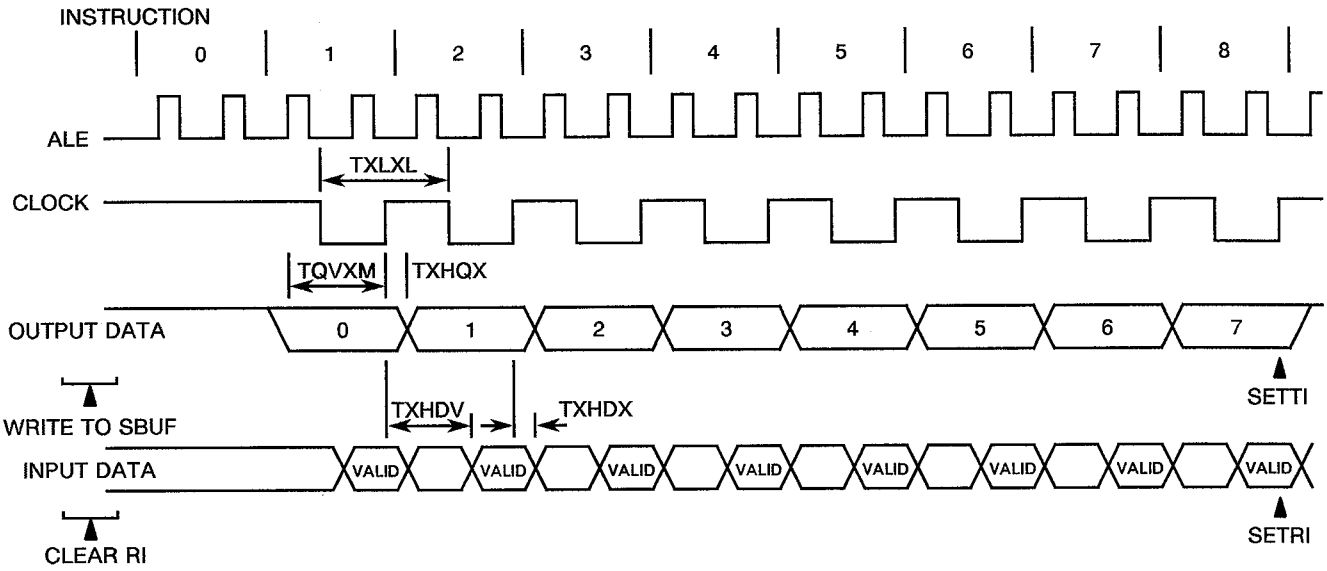


FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

SHIFT REGISTER TIMING WAVEFORMS



SYMBOL	PARAMETER	MIN.	MAX.	UNIT
TXLXL	Serial Port Clock Time	12TCLCL	-	µs
TQVXH	Output Data Setup to Clock Rising Edge	10TCLCL-133	-	ns
TXHQX	Output Data Hold After Clock Rising Edge	2TCLCL-117	-	ns
TXHDX	Input Data Hold After Clock Rising Edge	0	-	ns
TXHDV	Clock Rising Edge to Input Data Valid	-	10TLCL-133	ns

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

INTERNAL CLOCK WAVEFORMS

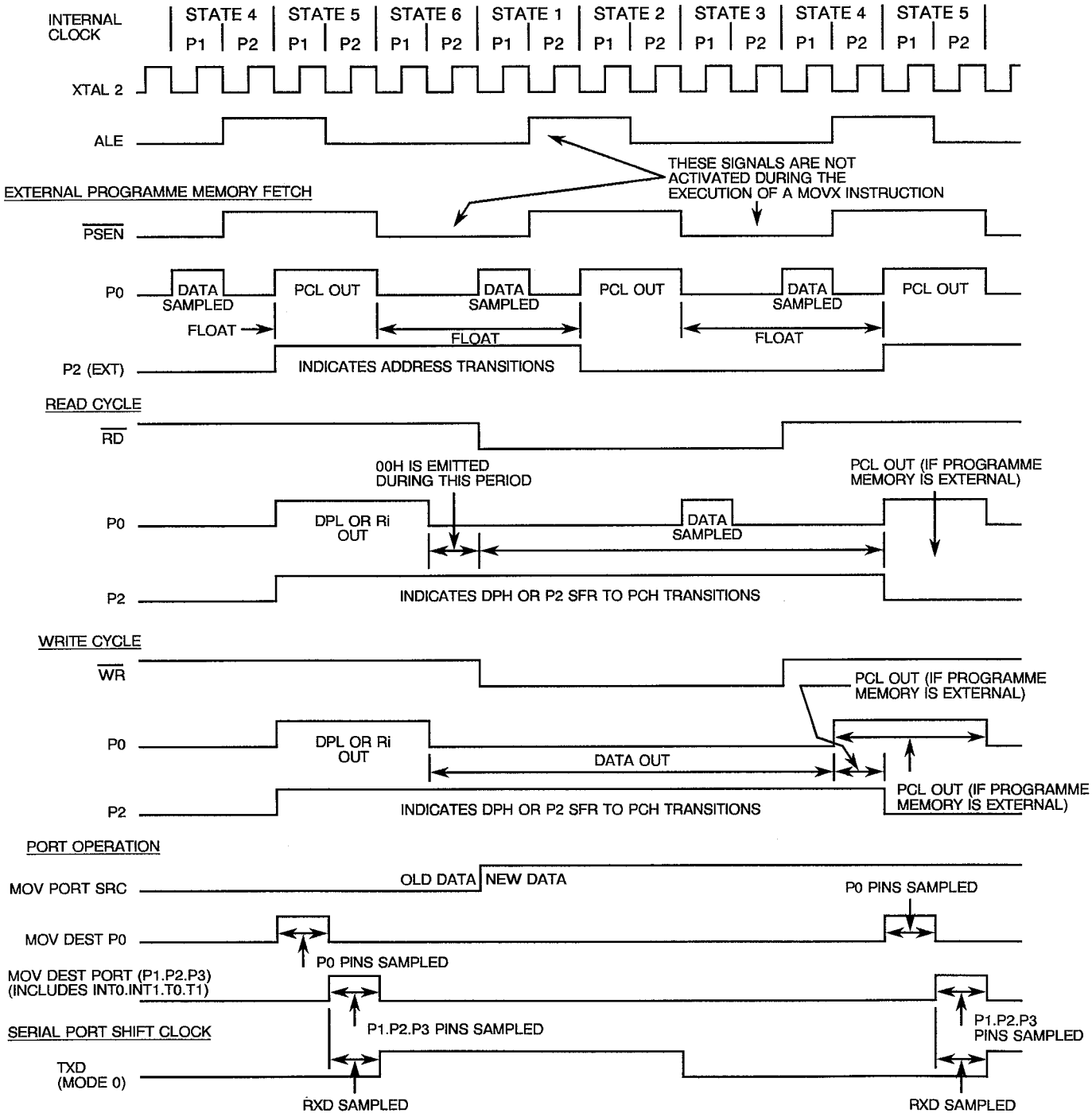


FIGURE 3(c) - CIRCUIT DESCRIPTION

Port 0 - Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external programme and data memory. In this application, it uses strong internal pull-ups when emitting 1's. External pull-ups are required during programme verification. Port 0 can sink eight LS TTL inputs.

Port 1 - Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, Port 1 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 1 also receives the low-order address bytes during programme verification. It can drive CMOS inputs without external pull-ups.

Port 2 - Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external Programme Memory and during accesses to external Data Memory that use 16-bit addresses. In this application, it uses strong internal pull-ups when emitting 1's. During access to external Data Memory that use 8-bit addresses, Port 2 emits the contents of the P2 Special Function Register.

Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs with external pull-ups.

Port 3 - Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pull-ups. It also serves the functions of various special features of the MCS-51 Family, as listed below.

PORT PIN	ALTERNATE FUNCTION	
P3.0	RXD	(Serial Input Port)
P3.1	TXD	(Serial Output Port)
P3.2	INT0	(External Interrupt 0)
P3.4	INT1	(External Interrupt 1)
P3.5	T0	(Timer 0 External Input)
P3.6	T1	(Timer 1 External Input)
P3.7	WR	(External Data Memory Write Strobe)
P3.8	RD	(External Data Memory Read Strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pull-ups.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

RST - A high level on this for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{DD}.

This pin does not receive the power down voltage as in the case for other MCS-51 family members. This function has been transferred to the V_{DD} pin.

ALE - Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 of the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pull-up.

I_{TL} - When an I/O pin on Ports 1, 2 and 3 is used as an input, the external circuit must sink current during the 1 to 0 transition. The maximum sink current is specified as I_{TL}.

IPD - This is the power down I_{DD} current when all output pins are disconnected.

$\overline{PSEN}$ - Program store Enable outputs is the read strobe to external Programme Memory. $\overline{PSEN}$ is activated twice each machine cycle during fetches from external Programme Memory (however, when executing out of external Programme Memory, two activations of $\overline{PSEN}$ are skipped during each access to external Data Memory). $\overline{PSEN}$ is not activated during fetches from internal Programme Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pull-up.

$\overline{EA}$ - When $\overline{EA}$ is held high, the CPU executes out of internal Programme Memory (unless the Programme Counter exceeds OFFFH). When $\overline{EA}$ is held low, the CPU executes only out of external Programme Memory. $\overline{EA}$ must not be floated.

XTAL1 - Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2 - Output of the inverting amplifier that forms the oscillator and input of the internal clock generator. This pin should be floated when an external oscillator is used.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in Figure 3(c)(i). Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 3(c)(ii). There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified must be observed.

FIGURE 3(c)(i) - CRYSTAL OSCILLATOR

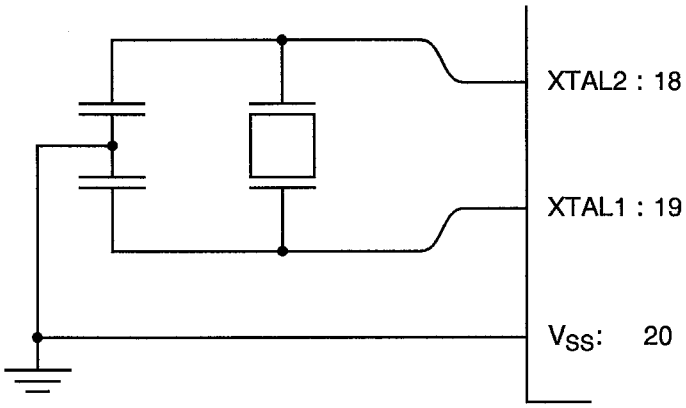


FIGURE 3(c)(ii) - EXTERNAL DRIVE CONFIGURATION

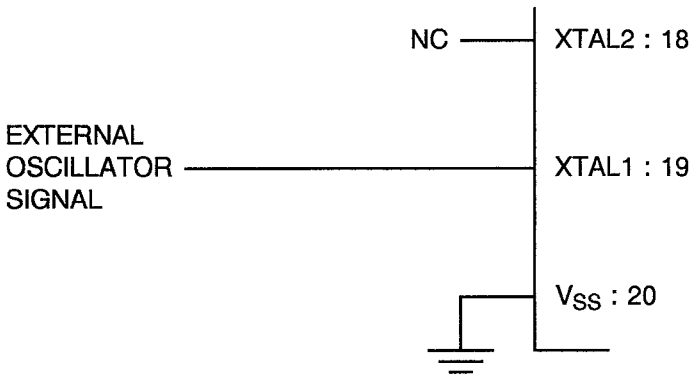
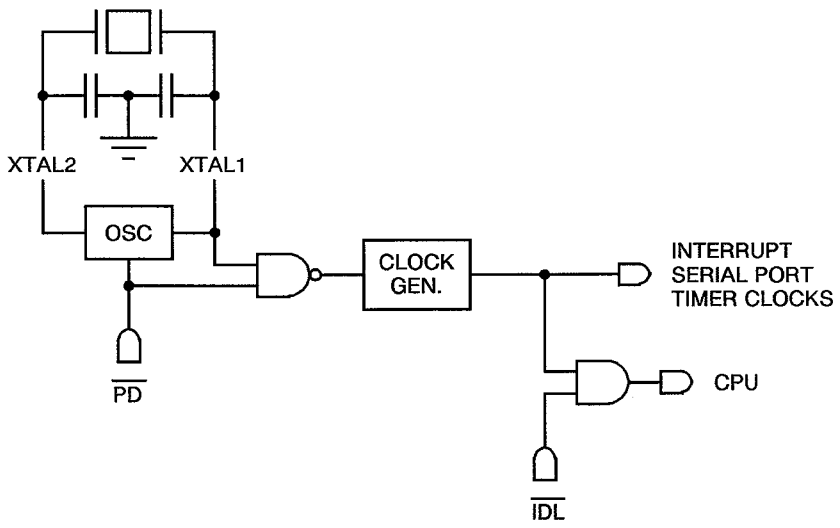


FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

IDLE AND POWER DOWN OPERATION

Figure 3(c)(iii) shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port and timer blocks to continue to function while the clock to the CPU is gated off.

FIGURE 3(c)(iii) - IDLE AND POWER DOWN HARDWARE



These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

PCON: POWER CONTROL REGISTER

(MSB)

SMOD	-	-	-	GF1	GF0	PD	LSD

SYMBOL	POSITION	NAME AND FUNCTION
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
-	PCON.6	(reserved)
-	PCON.5	(reserved)
-	PCON.4	(reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XXX0000).

STATUS OF THE EXTERNAL PINS DURING IDLE AND POWER DOWN MODES

MODE	PROGRAMME MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Port data	Port data	Port data	Port data
Idle	External	1	1	Floating	Port data	Address	Port data
Power down	Internal	0	0	Port data	Port data	Port data	Port data
Power down	External	0	0	Floating	Port data	Port data	Port data

IDLE MODE

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Programme Counter, Programme status Word, Accumulator, RAM and all other registers maintain their data during Idle. The table above describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. Then interrupt is serviced, and following RET1, the next instruction to be executed will be the one following the instruction that wrote a 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

POWER DOWN MODE

The instruction that sets PCON.1 is the last executed prior to entering power down. Once power is down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. A hardware reset initiates the Special Function Registers (see Table above).

In the Power Down mode, V_{DD} may be lowered to minimise circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered and that the voltage is restored before the hardware reset is applied which frees the oscillator.

Reset should not be released until the oscillator has restarted and stabilised +2 cycles. The table above describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external programme memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pull-up.

STOP CLOCK MODE

Due to static design, the MHS80C31SB clock speed can be reduced to 0MHz without any data loss in memory or registers. This mode allows step by step utilisation and permits the reduction in system power consumption by bringing the clock frequency down to any value.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

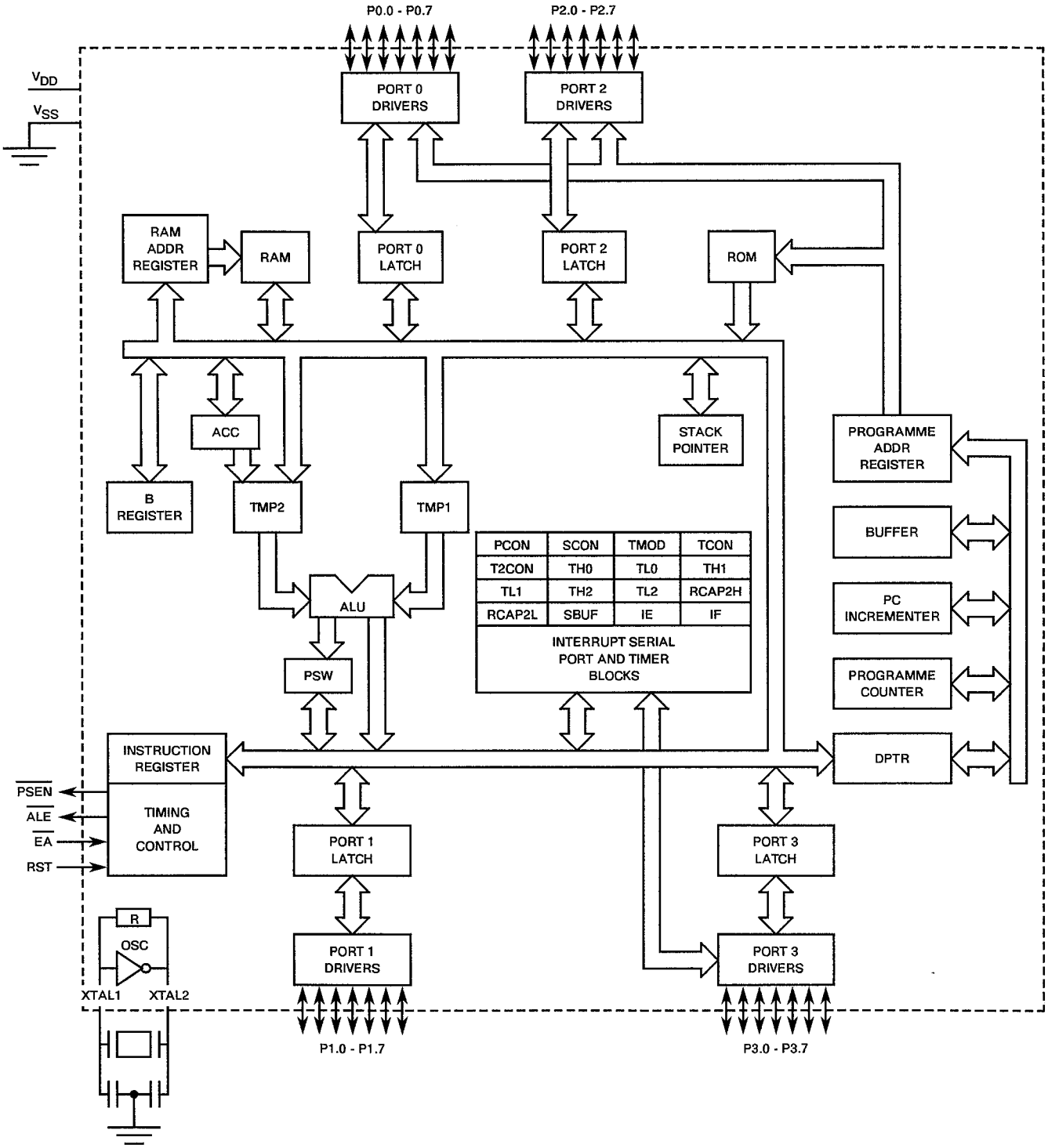
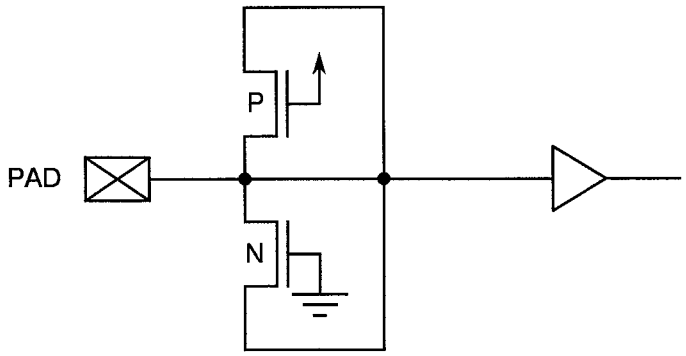
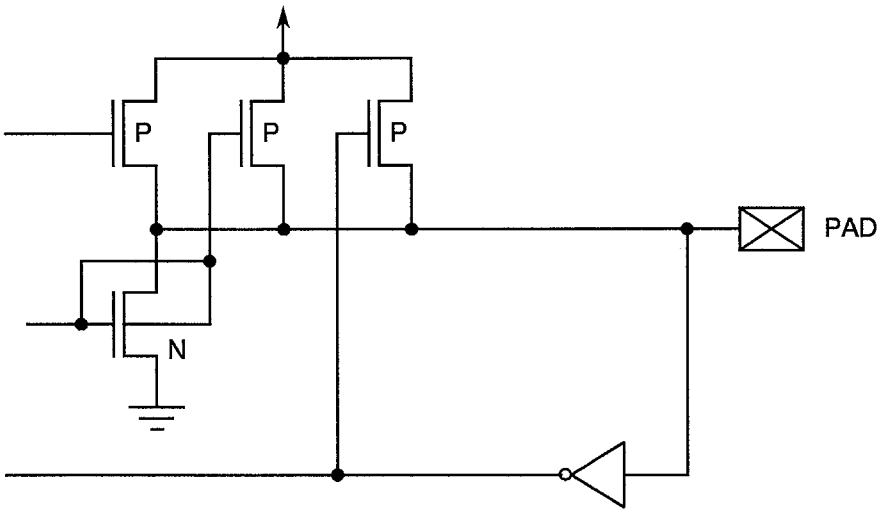


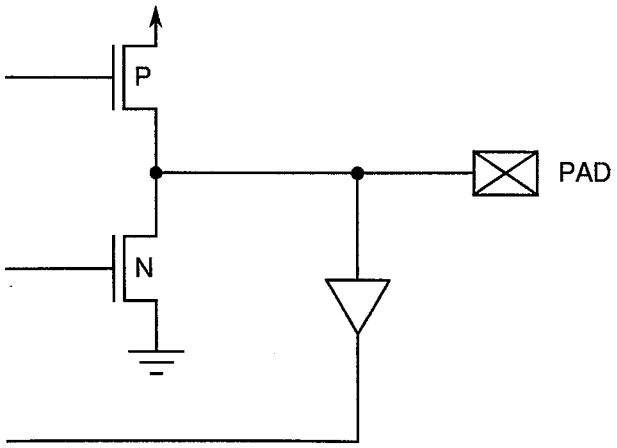
FIGURE 3(e) - INPUT PROTECTION NETWORKS



INPUTS EA, RST, XTAL1



I/O P1, P2, P3



I/O P0, ALE, $\overline{\text{PSEN}}$

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883C, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_{IC} - Input Clamp Voltage.
TCLCL - Clock Cycle Period.
TCLCX - Clock Low Time.
TCHCX - Clock High Time.
TCLCH - Clock Rise Time.
TCHCL - Clock Fall Time.
TLHLL - Ale Pulse Width.
TAVLL - Address Valid to ALE.
TLLAX - Address Hold After ALE.
TLLIV - ALE to Valid Instr. In.
TLLPL - ALE to $\overline{PSEN}$.
TPLPH - $\overline{PSEN}$ Pulse Width.
TPLIV - $\overline{PSEN}$ to Valid Instr. In.
TPXIX - Input Instr. Hold After $\overline{PSEN}$.
TPXIZ - Input Instr. Float After $\overline{PSEN}$.
TPXAV - $\overline{PSEN}$ to Address Valid.
TAVIV - Address to Valid Instr. In.
TPLAZ - $\overline{PSEN}$ Low to Address Float.
TRLRH - $\overline{RD}$ Pulse Width.
TWLWH - $\overline{WR}$ Pulse Width.
TLLAX - Data Address Hold After ALE.
TRLDV - $\overline{RD}$ to Valid Data In.
TRHDX - Data Hold After $\overline{RD}$.
TRHDZ - Data Float After $\overline{RD}$.
TLLDV - ALE to Valid Data In.
TAVDV - Address to Valid Data In.
TLLWL - ALE to $\overline{WR}$ or $\overline{RD}$.
TAVWL - Address to $\overline{WR}$ or $\overline{RD}$.
TQVWX - Data Valid to $\overline{WR}$ Transition.
TQVWH - Data Setup to $\overline{WR}$ High.
TWHQX - Data Hold After $\overline{WR}$.
TRLAZ - $\overline{RD}$ Low to Address Float.
TWHLH - $\overline{RD}$ or $\overline{WR}$ High to ALE High

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during irradiation qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on an irradiation lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), H.T.R.B.: Shall not be performed.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 13 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be glass frit-sealed or brazed.

4.4.2 Lead Material and Finish

The material shall be either Type 'D' with Type '2' finish or Type 'G' with Type '3' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

952100101BF

Detail Specification Number

Type Variant (see Table 1(a))

Testing Level (B or C, as applicable)

Total Dose Irradiation Level (if applicable)

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the Power Burn-in test are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	3(b)	Verify Truth Table without Load. $V_{IL} = 0V$, $V_{IH} = 3.0V$ $V_{OUT} = 1.5V$ $V_{DD} = 4.0V$, $V_{SS} = 0V$ f = 1.0MHz Note 1	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table without Load. $V_{IL} = 0V$, $V_{IH} = 3.0V$ $V_{OUT} = 1.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ f = 1.0MHz Note 1	-	-	-
3	Functional Test 3	-	-	3(b)	Verify Truth Table without Load. $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ $V_{OUT} = 1.5V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ f = 1.0MHz Note 1	-	-	-
4	Functional Test 4	-	-	3(b)	Verify Truth Table without Load. $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ $V_{OUT} = 1.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ f = 1.0MHz Note 1	-	-	-
5	Functional Test 5	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 0V$, $V_{IH} = 3.0V$ $V_{OUT} = 1.5V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ f = 1.0MHz Outputs: 1TTL + 50pF Note 1	-	-	-
6	Functional Test 6	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 0V$, $V_{IH} = 3.0V$ $V_{OUT} = 1.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ f = 1.0MHz Outputs: 1TTL + 50pF Note 1	-	-	-

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
7	Functional Test 7	-	-	3(b)	Verify Truth Table with Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f = 12MHz Outputs: 1TTL + 50pF Note 1	-	-	-
8	Functional Test 8	-	-	3(b)	Verify Truth Table with Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12MHz Outputs: 1TTL + 50pF Note 1	-	-	-
9 to 12	Quiescent Current 1	I_{DD1}	3005	4(a)	V_{DD} = 4.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 1.7 2.7 4.2 6.5	mA
13 to 16	Quiescent Current 2	I_{DD2}	3005	4(a)	V_{DD} = 5.0V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 2.0 3.2 5.5 7.3	mA
17 to 20	Quiescent Current 3	I_{DD3}	3005	4(a)	V_{DD} = 5.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 2.3 3.7 6.7 8.0	mA
21 to 24	Supply Current 1	$I_{DD(S1)}$	3005	4(a)	V_{DD} = 4.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 3.5 6.0 11.5 15	mA
25 to 28	Supply Current 2	$I_{DD(S2)}$	3005	4(a)	V_{DD} = 5.0V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 4.5 7.0 13 18	mA

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS MIN	LIMITS MAX	UNIT
29 to 32	Supply Current 3	$I_{DD(S3)}$	3005	4(a)	V_{DD} = 5.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 5.0 9.0 16 21	mA
33	Power Down Supply Current 1	$I_{DD(PD1)}$	-	4(a)	V_{DD} = 2.0V, V_{SS} = 0V (Pin 40)	-	75	µA
34	Power Down Supply Current 2	$I_{DD(PD2)}$	-	4(a)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 40)	-	75	µA
35 to 42	Input Leakage Current Low Level 1	I_{IL1}	-	4(b)	V_{IN} (Under Test) = 0.45V V_{DD} = 5.5V, V_{SS} = 0V (Pins 32 to 39)	−10	10	µA
43	Input Leakage Current Low Level 2	I_{IL2}	-	4(b)	V_{IN} (Under Test) = 0.45V V_{DD} = 5.5V, V_{SS} = 0V (Pin 31)	−10	10	µA
44 to 51	Input Leakage Current High Level 1	I_{IH1}	-	4(b)	V_{IN} (Under Test) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 32 to 39)	−10	10	µA
52	Input Leakage Current High Level 2	I_{IH2}	-	4(b)	V_{IN} (Under Test) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pin 31)	−10	10	µA
53 to 76	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0.45V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 to 8, 10 to 17, 21 to 28)	−75	-	µA
77 to 100	High to Low Transition Current	I_{IT}	-	4(c)	V_{IN} (Under Test) = 2.0V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 to 8, 10 to 17, 21 to 28)	−750	-	µA
101 to 108	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	I_{OL} = 3.2mA V_{DD} = 4.5V, V_{SS} = 0V (Pins 32 to 39)	-	0.45	V
109 to 132	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	I_{OL} = 1.6mA V_{DD} = 4.5V, V_{SS} = 0V (Pins 1 to 8, 10 to 17, 21 to 28)	-	0.45	V
133 to 134	Output Voltage Low Level 3	V_{OL3}	3007	4(d)	I_{OL} = 3.2mA V_{DD} = 4.5V, V_{SS} = 0V (Pins 29 to 30)	-	0.45	V

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
135 to 142	Output Voltage High Level 1	V_{OH1}	3006	4(e)	$I_{OH} = -400\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 2 (Pins 32 to 39)	2.4	-	V
143 to 166	Output Voltage High Level 2	V_{OH2}	3006	4(e)	$I_{OH} = -60\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 1 to 8, 10 to 17, 21 to 28)	2.4	-	V
167 to 174	Output Voltage High Level 3	V_{OH3}	3006	4(e)	$I_{OH} = -150\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 2 (Pins 32 to 39)	3.375	-	V
175 to 199	Output Voltage High Level 4	V_{OH4}	3006	4(e)	$I_{OH} = -25\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 1 to 8, 10 to 17, 21 to 28)	3.375	-	V
200 to 207	Output Voltage High Level 5	V_{OH5}	3006	4(e)	$I_{OH} = -40\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 2 (Pins 32 to 39)	4.05	-	V
208 to 232	Output Voltage High Level 6	V_{OH6}	3006	4(e)	$I_{OH} = -10\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 1 to 8, 10 to 17, 21 to 28)	4.04	-	V
233 to 234	Output Voltage High Level 7	V_{OH7}	3006	4(e)	$I_{OH} = -400\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 29 to 30)	2.4	-	V
235 to 236	Output Voltage High Level 8	V_{OH8}	3006	4(e)	$I_{OH} = -150\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 29 to 30)	3.375	-	V
237 to 238	Output Voltage High Level 9	V_{OH9}	3006	4(e)	$I_{OH} = -40\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 29 to 30)	4.05	-	V
239 to 276	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(f)	I_{IN} (Under Test) = $100\mu A$ V_{DD} = Open, $V_{SS} = 0V$ (Pins 1 to 19, 21 to 39)	0.2	-	V
277 to 314	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(f)	I_{IN} (Under Test) = $100\mu A$ $V_{DD} = 0V$, V_{SS} = Open (Pins 1 to 19, 21 to 39)	-	−0.2	V
315	Reset Resistor	RRST	-	-	$V_{DD} = 4.5V$ (Pin 9)	50	200	kΩ

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
316 to 357	Input/Output Capacitance		-	4(f)	$V_{IN/OUT}$ (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ f = 1.0MHz Note 3 (Pins 1 to 19, 21 to 39)	-	10	pF
358	ALE Pulse Width	TLHHL-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pin 30)	111	-	ns
359	Address Valid to ALE	TAVLL-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins (32 to 39) to 30)	13	-	ns
360	Address Hold to ALE	TLLAX-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 30 to (32 to 39))	33	-	ns
361	ALE to Valid Inst. In	TLLIV-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 30 to (32 to 39))	213	-	ns
362	ALE to $\overline{PSEN}$	TLLPL-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 30 to 29)	28	-	ns
363	$\overline{PSEN}$ Pulse Width	TPLPH-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pin 29)	190	-	ns
364	$\overline{PSEN}$ to Valid Inst. In	TPLIV-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 29 to (32 to 39))	115	-	ns
365	$\overline{PSEN}$ to In Instr. Hold	TPXIX-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 29 to (32 to 39))	-	0	ns
366	$\overline{PSEN}$ to Address Valid	TPXAV-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 29 to (21 to 28))	75	-	ns

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
367	Address to Valid Inst. In	TAVIV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	265	-	ns
368	$\overline{RD}$ Pulse Width	TRLRH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pin 17)	400	-	ns
369	$\overline{WR}$ Pulse Width	TWLWH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pin 16)	400	-	ns
370	ALE to Data Address Hold	TLLAXR-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	33	-	ns
371	$\overline{RD}$ to Valid Data In	TRLDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	232	-	ns
372	$\overline{RD}$ to Data Hold	TRHDX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
373	$\overline{RD}$ to Data Float	TRHDZ-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	82	-	ns
374	ALE to Valid Data In	TLLDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	496	-	ns
375	Address to Valid Data In	TAVDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	564	-	ns
376	ALE to $\overline{WR}$	TLLWL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to 16)	185	315	ns

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
377	ALE to $\overline{RD}$	TLLRL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to 17)	185	315	ns
378	Address to $\overline{WR}$	TAVWL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	187	-	ns
379	Address to $\overline{RD}$	TAVRL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 17)	187	-	ns
380	Data Valid to $\overline{WR}$	TQVWX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	8.0	-	ns
381	Data Setup to $\overline{WR}$ High	TQVWH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	431	-	ns
382	$\overline{WR}$ to Data Hold	TWHQX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 16 to (32 to 39))	18	-	ns
383	$\overline{RD}$ Low to Address Float	TRLAZ-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
384	$\overline{WR}$ High to ALE High	TWHLH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 16 to 30)	18	184	ns
385	$\overline{RD}$ High to ALE High	TRHLH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to 30)	18	184	ns
386	Serial Port Clock Cycle Time	TXLXL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	999	1001	ns

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
387	Out Data Setup to Clock	TQVXH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	700	-	ns
388	Clock to Out Data Hold	TXHQX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	49	-	ns
389	Clock to In Data Hold	TXHDX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	-	0	ns
390	Clock High to In Data Valid	TXHDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	700	-	ns
391	ALE Pulse Width	TLHLL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 30)	111	-	ns
392	Address Valid to ALE	TAVLL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 30)	13	-	ns
393	Address Hold to ALE	TLLAX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	33	-	ns
394	ALE to Valid Inst. In	TLLIV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	213	-	ns
395	ALE to $\overline{PSEN}$	TLLPL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to 29)	28	-	ns
396	$\overline{PSEN}$ Pulse Width	TPLPH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 29)	190	-	ns
397	$\overline{PSEN}$ to Valid Inst. In	TPLIV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 29 to (32 to 39))	115	-	ns

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
398	$\overline{PSEN}$ to In Inst. Hold	TPXIX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 29 to (32 to 39))	-	0	ns
399	$\overline{PSEN}$ to Address Valid	TPXAV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 29 to (21 to 28))	75	-	ns
400	Address to Valid Inst. In	TAVIV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	265	-	ns
401	$\overline{RD}$ Pulse Width	TRLRH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 17)	400	-	ns
402	$\overline{WR}$ Pulse Width	TWLWH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 16)	400	-	ns
403	ALE to Data Address Hold	TLLAXR-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	33	-	ns
404	$\overline{RD}$ to Valid Data In	TRLDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	232	-	ns
405	$\overline{RD}$ to Data Hold	TRHDX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
406	$\overline{RD}$ to Data Float	TRHDZ-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	82	-	ns
407	ALE to Valid Data In	TLLDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	496	-	ns

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
408	Address to Valid Data In	TAVDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	564	-	ns
409	ALE to $\overline{WR}$	TLLWL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to 16)	185	315	ns
410	ALE to $\overline{RD}$	TLLRL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to 17)	185	315	ns
411	Address to $\overline{WR}$	TAVWL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	187	-	ns
412	Address to $\overline{RD}$	TAVRL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 17)	187	-	ns
413	Data Valid to $\overline{WR}$	TQVWX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	8.0	-	ns
414	Data Setup to $\overline{WR}$ High	TQVWH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	431	-	ns
415	$\overline{WR}$ to Data Hold	TWHQX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 16 to (32 to 39))	18	-	ns
416	$\overline{RD}$ Low to Address Float	TRLAZ-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
417	$\overline{WR}$ High to ALE High	TWHLH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 16 to 30)	18	184	ns

NOTES: See Page 42.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
418	$\overline{RD}$ High to ALE High	TRHLH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to 30)	18	184	ns
419	Serial Port Clock Cycle Time	TXLXL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	999	1001	ns
420	Out Data Setup to Clock	TQVXH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	700	-	ns
421	Clock to Out Data Hold	TXHQX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	49	-	ns
422	Clock to In Data Hold	TXHDX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	-	0	ns
423	Clock High to In Data Valid	TXHDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	700	-	ns

NOTES

1. Functional test includes: instruction set, internal registers, interrupts, timer, serial port, external data, programme counter, ram, idle mode, power-down mode.

   Other parameters (guaranteed):

   V_{IL} min = − 0.5V — V_{IL} max = 0.2V_{DD} − 0.25V (0.85V at 5.5V)
   Except Pin EA: V_{IL} max = 0.2 V_{DD} − 0.45V.

   V_{IH} max = V_{DD} + 0.5V — V_{IH} min = 0.2 V_{DD} + 1.1V (2.0V at 4.5V)
   Except Pins XTAL1, RESET: V_{IH} min = 0.7 V_{DD} + 0.2V.

2. Pull-up resistor = 100kΩ.
3. Guaranteed but not tested.
4. Measurements shall be performed on 100% basis read and record.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 4.0V, V_{SS} = 0V f = 1.0MHz Note 1	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f = 1.0MHz Note 1	-	-	-
3	Functional Test 3	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0.8V, V_{IH} = 2.2V V_{OUT} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f = 1.0MHz Note 1	-	-	-
4	Functional Test 4	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0.8V, V_{IH} = 2.2V V_{OUT} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f = 1.0MHz Note 1	-	-	-
5	Functional Test 5	-	-	3(b)	Verify Truth Table with Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f = 1.0MHz Outputs: 1TTL + 50pF Note 1	-	-	-
6	Functional Test 6	-	-	3(b)	Verify Truth Table with Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f = 1.0MHz Outputs: 1TTL + 50pF Note 1	-	-	-

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS MIN	LIMITS MAX	UNIT
7	Functional Test 7	-	-	3(b)	Verify Truth Table with Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f = 12MHz Outputs: 1TTL + 50pF Note 1	-	-	-
8	Functional Test 8	-	-	3(b)	Verify Truth Table with Load. V_{IL} = 0V, V_{IH} = 3.0V V_{OUT} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12MHz Outputs: 1TTL + 50pF Note 1	-	-	-
9 to 12	Quiescent Current 1	I_{DD1}	3005	4(a)	V_{DD} = 4.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 1.7 2.7 4.2 6.5	mA
13 to 16	Quiescent Current 2	I_{DD2}	3005	4(a)	V_{DD} = 5.0V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 2.0 3.2 5.5 7.3	mA
17 to 20	Quiescent Current 3	I_{DD3}	3005	4(a)	V_{DD} = 5.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 2.3 3.7 6.7 8.0	mA
21 to 24	Supply Current 1	$I_{DD(S1)}$	3005	4(a)	V_{DD} = 4.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 3.5 6.0 11.5 15	mA
25 to 28	Supply Current 2	$I_{DD(S2)}$	3005	4(a)	V_{DD} = 5.0V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 4.5 7.0 13 18	mA

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS MIN	LIMITS MAX	UNIT
29 to 32	Supply Current 3	$I_{DD(S3)}$	3005	4(a)	V_{DD} = 5.5V, V_{SS} = 0V f = 0.5MHz f = 3.5MHz f = 8.0MHz f = 12MHz (Pin 40)	 - - - -	 5.0 9.0 16 21	mA
33	Power Down Supply Current 1	$I_{DD(PD1)}$	-	4(a)	V_{DD} = 2.0V, V_{SS} = 0V (Pin 40)	-	75	µA
34	Power Down Supply Current 2	$I_{DD(PD2)}$	-	4(a)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 40)	-	75	µA
35 to 42	Input Leakage Current Low Level 1	I_{IL1}	-	4(b)	V_{IN} (Under Test) = 0.45V V_{DD} = 5.5V, V_{SS} = 0V (Pins 32 to 39)	−10	10	µA
43	Input Leakage Current Low Level 2	I_{IL2}	-	4(b)	V_{IN} (Under Test) = 0.45V V_{DD} = 5.5V, V_{SS} = 0V (Pin 31)	−10	10	µA
44 to 51	Input Leakage Current High Level 1	I_{IH1}	-	4(b)	V_{IN} (Under Test) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 32 to 39)	−10	10	µA
52	Input Leakage Current High Level 2	I_{IH2}	-	4(b)	V_{IN} (Under Test) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pin 31)	−10	10	µA
53 to 76	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0.45V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 to 8, 10 to 17, 21 to 28)	−75	-	µA
77 to 100	High to Low Transition Current	I_{IT}	-	4(c)	V_{IN} (Under Test) = 2.0V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 to 8, 10 to 17, 21 to 28)	−750	-	µA
101 to 108	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	I_{OL} = 3.2mA V_{DD} = 4.5V, V_{SS} = 0V (Pins 32 to 39)	-	0.45	V
109 to 132	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	I_{OL} = 1.6mA V_{DD} = 4.5V, V_{SS} = 0V (Pins 1 to 8, 10 to 17, 21 to 28)	-	0.45	V
133 to 134	Output Voltage Low Level 3	V_{OL3}	3007	4(d)	I_{OL} = 3.2mA V_{DD} = 4.5V, V_{SS} = 0V (Pins 29 to 30)	-	0.45	V

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
135 to 142	Output Voltage High Level 1	V_{OH1}	3006	4(e)	$I_{OH} = -400\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 2 (Pins 32 to 39)	2.4	-	V
143 to 166	Output Voltage High Level 2	V_{OH2}	3006	4(e)	$I_{OH} = -60\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 1 to 8, 10 to 17, 21 to 28)	2.4	-	V
167 to 174	Output Voltage High Level 3	V_{OH3}	3006	4(e)	$I_{OH} = -150\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 2 (Pins 32 to 39)	3.375	-	V
175 to 199	Output Voltage High Level 4	V_{OH4}	3006	4(e)	$I_{OH} = -25\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 1 to 8, 10 to 17, 21 to 28)	3.375	-	V
200 to 207	Output Voltage High Level 5	V_{OH5}	3006	4(e)	$I_{OH} = -40\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 2 (Pins 32 to 39)	4.05	-	V
208 to 232	Output Voltage High Level 6	V_{OH6}	3006	4(e)	$I_{OH} = -10\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 1 to 8, 10 to 17, 21 to 28)	4.04	-	V
233 to 234	Output Voltage High Level 7	V_{OH7}	3006	4(e)	$I_{OH} = -400\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 29 to 30)	2.4	-	V
235 to 236	Output Voltage High Level 8	V_{OH8}	3006	4(e)	$I_{OH} = -150\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 29 to 30)	3.375	-	V
237 to 238	Output Voltage High Level 9	V_{OH9}	3006	4(e)	$I_{OH} = -40\mu A$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 29 to 30)	4.05	-	V
239 to 276	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(f)	I_{IN} (Under Test) = $100\mu A$ V_{DD} = Open, $V_{SS} = 0V$ (Pins 1 to 19, 21 to 39)	0.2	-	V
277 to 314	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(f)	I_{IN} (Under Test) = $100\mu A$ $V_{DD} = 0V$, V_{SS} = Open (Pins 1 to 19, 21 to 39)	-	-0.2	V
315	Reset Resistor	RRST	-	-	$V_{DD} = 4.5V$ (Pin 9)	50	200	kΩ

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
316 to 357	Input/Output Capacitance		-	4(f)	$V_{IN/OUT}$ (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ f = 1.0MHz Note 3 (Pins 1 to 19, 21 to 39)	-	10	pF
358	ALE Pulse Width	TLHHL-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pin 30)	111	-	ns
359	Address Valid to ALE	TAVLL-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins (32 to 39) to 30)	13	-	ns
360	Address Hold to ALE	TLLAX-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 30 to (32 to 39))	33	-	ns
361	ALE to Valid Inst. In	TLLIV-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 30 to (32 to 39))	213	-	ns
362	ALE to $\overline{PSEN}$	TLLPL-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 30 to 29)	28	-	ns
363	$\overline{PSEN}$ Pulse Width	TPLPH-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pin 29)	190	-	ns
364	$\overline{PSEN}$ to Valid Inst. In	TPLIV-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 29 to (32 to 39))	115	-	ns
365	$\overline{PSEN}$ to In Instr. Hold	TPXIX-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 29 to (32 to 39))	-	0	ns
366	$\overline{PSEN}$ to Address Valid	TPXAV-1	-	4(g)	f = 12MHz $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 4 (Pins 29 to (21 to 28))	75	-	ns

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
367	Address to Valid Inst. In	TAVIV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	265	-	ns
368	$\overline{RD}$ Pulse Width	TRLRH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pin 17)	400	-	ns
369	$\overline{WR}$ Pulse Width	TWLWH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pin 16)	400	-	ns
370	ALE to Data Address Hold	TLLAXR-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	33	-	ns
371	$\overline{RD}$ to Valid Data In	TRLDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	232	-	ns
372	$\overline{RD}$ to Data Hold	TRHDX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
373	$\overline{RD}$ to Data Float	TRHDZ-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	82	-	ns
374	ALE to Valid Data In	TLLDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	496	-	ns
375	Address to Valid Data In	TAVDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	564	-	ns
376	ALE to $\overline{WR}$	TLLWL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to 16)	185	315	ns

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
377	ALE to $\overline{RD}$	TLLRL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 30 to 17)	185	315	ns
378	Address to $\overline{WR}$	TAVWL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	187	-	ns
379	Address to $\overline{RD}$	TAVRL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 17)	187	-	ns
380	Data Valid to $\overline{WR}$	TQVWX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	8.0	-	ns
381	Data Setup to $\overline{WR}$ High	TQVWH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	431	-	ns
382	$\overline{WR}$ to Data Hold	TWHQX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 16 to (32 to 39))	18	-	ns
383	$\overline{RD}$ Low to Address Float	TRLAZ-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
384	$\overline{WR}$ High to ALE High	TWHLH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 16 to 30)	18	184	ns
385	$\overline{RD}$ High to ALE High	TRHLH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 17 to 30)	18	184	ns
386	Serial Port Clock Cycle Time	TXLXL-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	999	1001	ns

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
387	Out Data Setup to Clock	TQVXH-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	700	-	ns
388	Clock to Out Data Hold	TXHQX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	49	-	ns
389	Clock to In Data Hold	TXHDX-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	-	0	ns
390	Clock High to In Data Valid	TXHDV-1	-	4(g)	f = 12MHz V_{DD} = 4.5V, V_{SS} = 0V Note 4	700	-	ns
391	ALE Pulse Width	TLHLL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 30)	111	-	ns
392	Address Valid to ALE	TAVLL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 30)	13	-	ns
393	Address Hold to ALE	TLLAX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	33	-	ns
394	ALE to Valid Inst. In	TLLIV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	213	-	ns
395	ALE to $\overline{PSEN}$	TLLPL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to 29)	28	-	ns
396	$\overline{PSEN}$ Pulse Width	TPLPH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 29)	190	-	ns
397	$\overline{PSEN}$ to Valid Inst. In	TPLIV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 29 to (32 to 39))	115	-	ns

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
398	$\overline{PSEN}$ to In Inst. Hold	TPXIX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 29 to (32 to 39))	-	0	ns
399	$\overline{PSEN}$ to Address Valid	TPXAV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 29 to (21 to 28))	75	-	ns
400	Address to Valid Inst. In	TAVIV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	265	-	ns
401	$\overline{RD}$ Pulse Width	TRLRH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 17)	400	-	ns
402	$\overline{WR}$ Pulse Width	TWLWH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 16)	400	-	ns
403	ALE to Data Address Hold	TLLAXR-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	33	-	ns
404	$\overline{RD}$ to Valid Data In	TRLDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	232	-	ns
405	$\overline{RD}$ to Data Hold	TRHDX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
406	$\overline{RD}$ to Data Float	TRHDZ-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	82	-	ns
407	ALE to Valid Data In	TLLDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to (32 to 39))	496	-	ns

NOTES: See Page 42.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
408	Address to Valid Data In	TAVDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (21 to 28) to (32 to 39))	564	-	ns
409	ALE to $\overline{WR}$	TLLWL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to 16)	185	315	ns
410	ALE to $\overline{RD}$	TLLRL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 30 to 17)	185	315	ns
411	Address to $\overline{WR}$	TAVWL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	187	-	ns
412	Address to $\overline{RD}$	TAVRL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 17)	187	-	ns
413	Data Valid to $\overline{WR}$	TQVWX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	8.0	-	ns
414	Data Setup to $\overline{WR}$ High	TQVWH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins (32 to 39) to 16)	431	-	ns
415	$\overline{WR}$ to Data Hold	TWHQX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 16 to (32 to 39))	18	-	ns
416	$\overline{RD}$ Low to Address Float	TRLAZ-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to (32 to 39))	-	0	ns
417	$\overline{WR}$ High to ALE High	TWHLH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 16 to 30)	18	184	ns

NOTES: See Page 42.

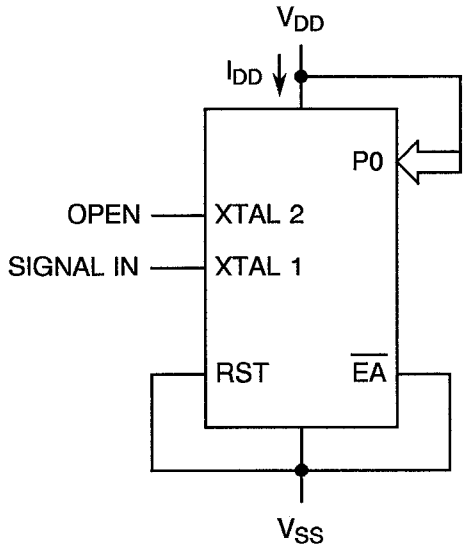
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
418	$\overline{RD}$ High to ALE High	TRHLH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 17 to 30)	18	184	ns
419	Serial Port Clock Cycle Time	TXLXL-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	999	1001	ns
420	Out Data Setup to Clock	TQVXH-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	700	-	ns
421	Clock to Out Data Hold	TXHQX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	49	-	ns
422	Clock to In Data Hold	TXHDX-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	-	0	ns
423	Clock High to In Data Valid	TXHDV-2	-	4(g)	f = 12MHz V_{DD} = 5.5V, V_{SS} = 0V Note 4	700	-	ns

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

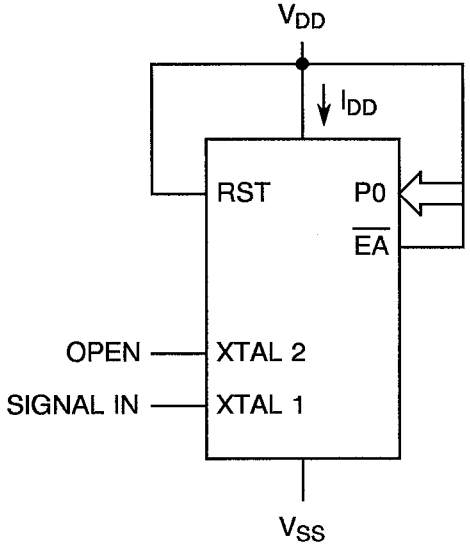
FIGURE 4(a) - SUPPLY CURRENT

FIGURE 4(a)(i) - QUIESCENT CURRENT



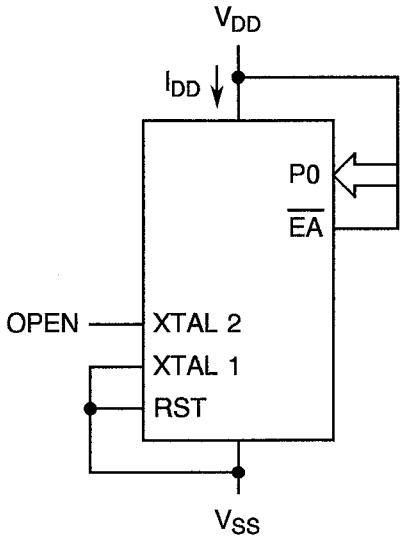
NOTES
1. All remaining pins open.

FIGURE 4(a)(ii) - ACTIVE CURRENT



NOTES
1. All remaining pins open.

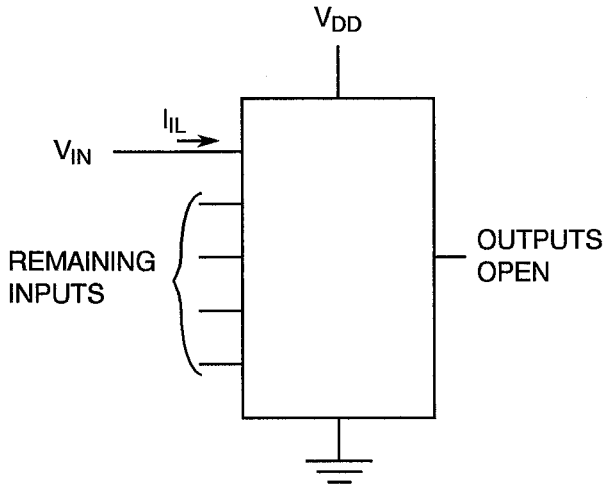
FIGURE 4(a)(iii) - POWER DOWN CURRENT



NOTES
1. All remaining pins open.

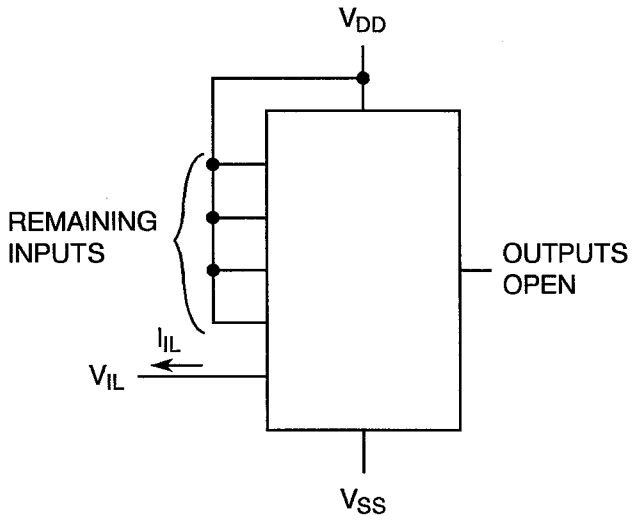
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - INPUT LEAKAGE CURRENT



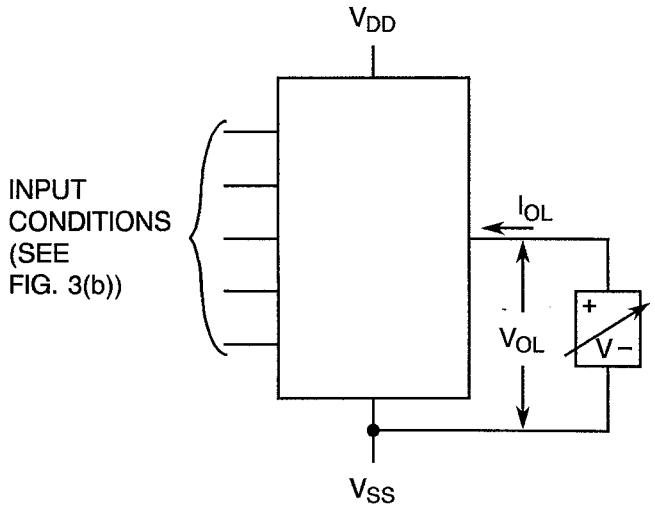
NOTES
1. Each input to be tested separately.

FIGURE 4(c) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately.

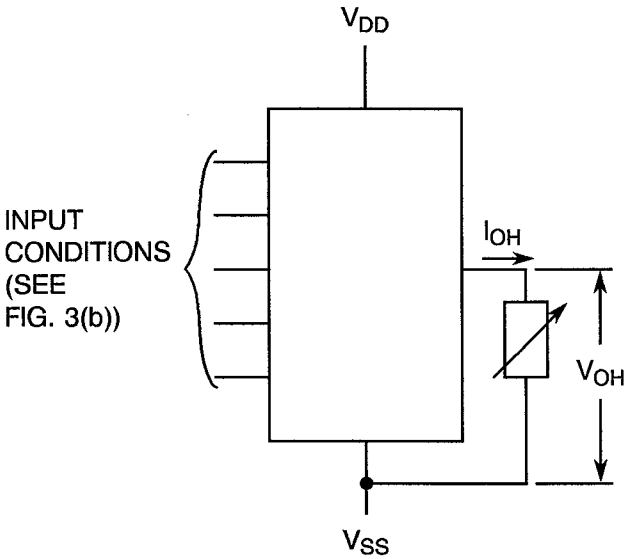
FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



NOTES
1. Each output to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

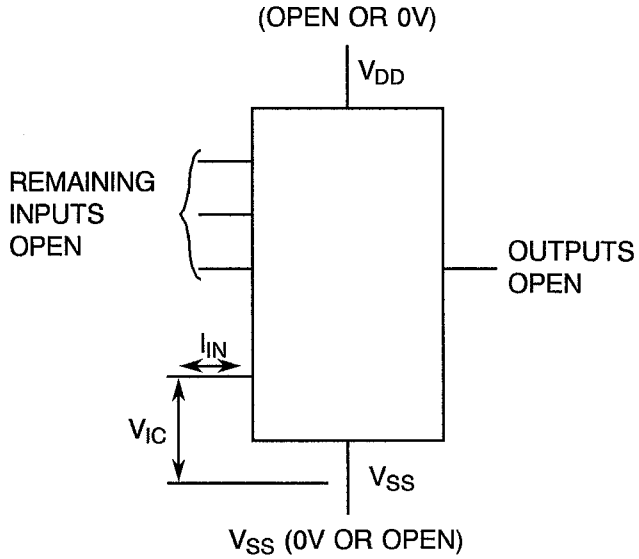
FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



NOTES

1. Each output to be tested separately.

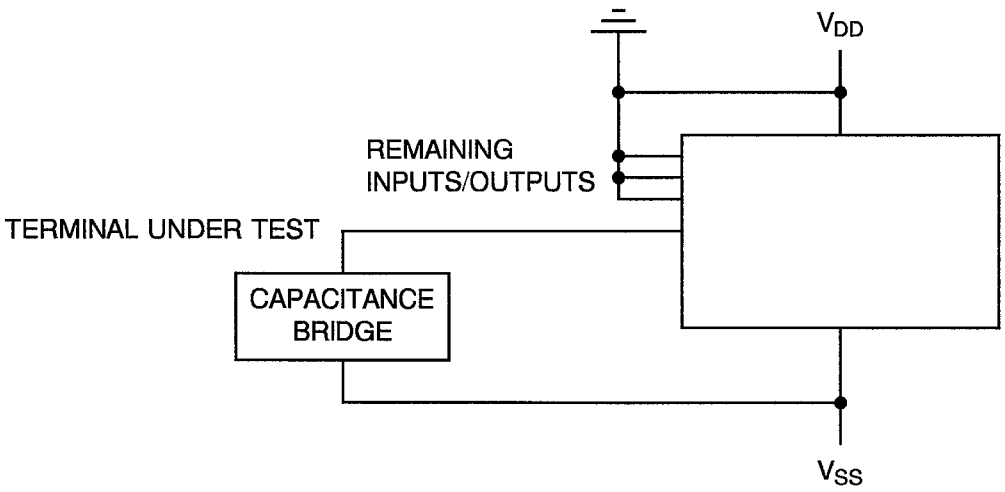
FIGURE 4(f) - INPUT CLAMP VOLTAGE



NOTES

1. Each input to be tested separately.

FIGURE 4(g) - INPUT AND OUTPUT CAPACITANCE



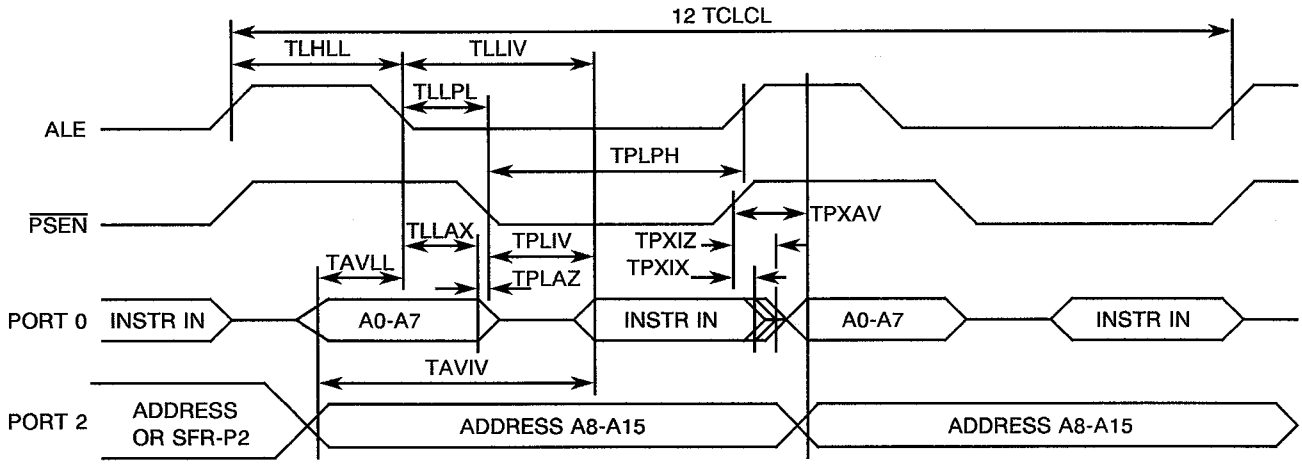
NOTES

1. Test frequency = 1.0MHz.
2. Each input and output is to be tested separately.

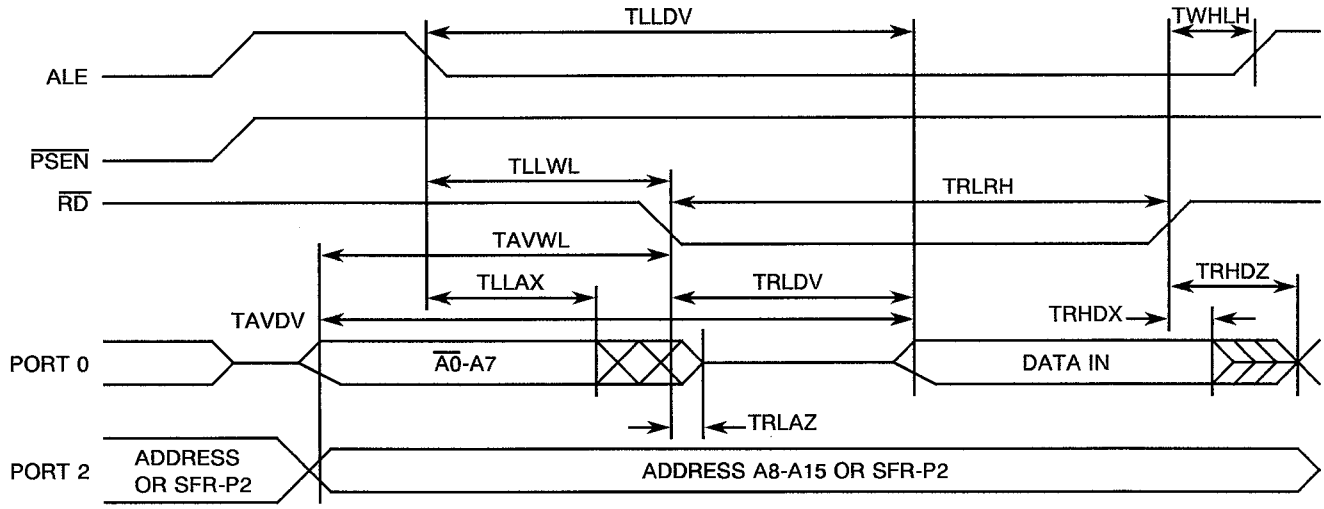
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - PROPAGATION DELAY AND TRANSITION TIME

EXTERNAL PROGRAMME MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

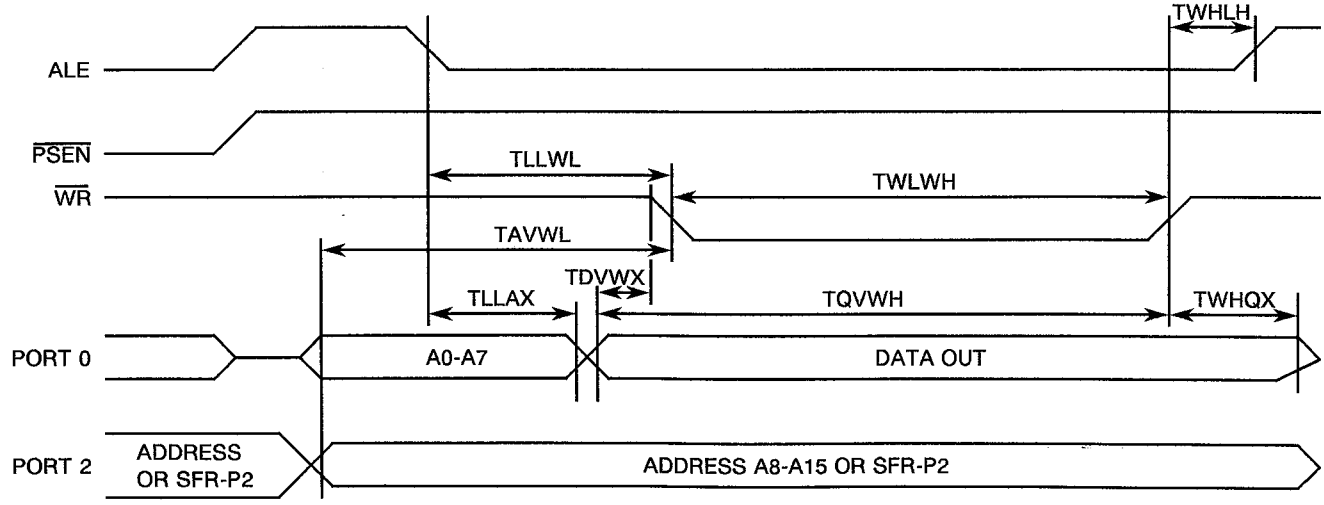
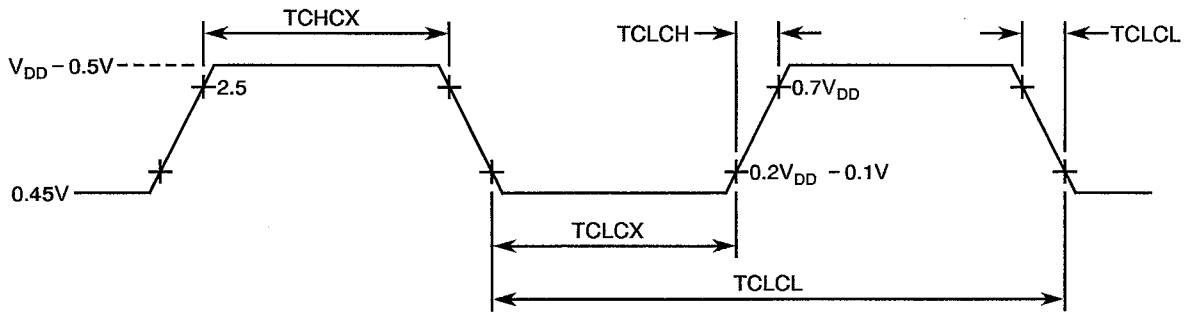


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

EXTERNAL CLOCK WAVEFORMS



SHIFT REGISTER TIMING WAVEFORMS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
TXLXL	Serial Port Clock Time	12TCLCL	-	µs
TQVXH	Output Data Setup to Clock Rising Edge	10TCLCL-133	-	ns
TXHQX	Output Data Hold After Clock Rising Edge	2TCLCL-117	-	ns
TXHDX	Input Data Hold After Clock Rising Edge	0	-	ns
TXHDV	Clock Rising Edge to Input Data Valid	-	10TLCL-133	ns

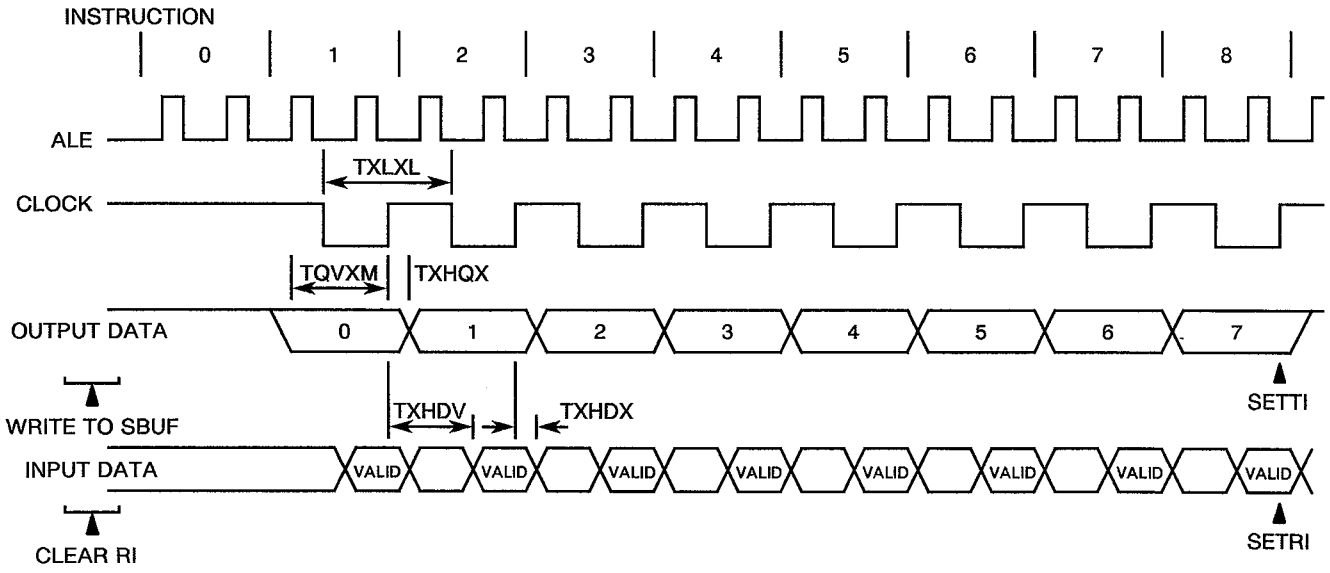


TABLE 4 - PARAMETER DRIFT VALUES

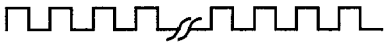
No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
29 to 32	Supply Current 3	$I_{DD(S3)}$	As per Table 2	As per Table 2	±2.0	mA
33	Power Down Supply Current 1	$I_{DD(PD1)}$	As per Table 2	As per Table 2	±8.0	µA
34	Power Down Supply Current 2	$I_{DD(PD2)}$	As per Table 2	As per Table 2	±8.0	µA
35 to 42	Input Leakage Current Low Level 1	I_{IL1}	As per Table 2	As per Table 2	±1.0	µA
43	Input Leakage Current Low Level 2	I_{IL2}	As per Table 2	As per Table 2	±1.0	µA
44 to 51	Input Leakage Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	±1.0	µA
52	Input Leakage Current High Level 2	I_{IH2}	As per Table 2	As per Table 2	±1.0	µA
53 to 76	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±8.0	µA
77 to 100	High to Low Transition Current	I_{IT}	As per Table 2	As per Table 2	±75	µA
101 to 108	Output Voltage Low Level 1	V_{OL1}	As per Table 2	As per Table 2	±0.04	V
109 to 132	Output Voltage Low Level 2	V_{OL2}	As per Table 2	As per Table 2	±0.04	V
133 to 134	Output Voltage Low Level 3	V_{OL3}	As per Table 2	As per Table 2	±0.04	V
135 to 142	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±0.2	V
143 to 166	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	±0.2	V
233 to 234	Output Voltage High Level 7	V_{OH7}	As per Table 2	As per Table 2	±0.2	V

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Inputs/Outputs - (Pins1-2-3-4-5-6-7-8-10-11-12-13-14-15-16-17-21-22-23-24-25-26-27-28-29-30-32-33-34-35-36-37-38-39)	V_{OUT}	Parallel connected	-
3	Input - (Pin 18)	V_{IN}	V_{SS}	V
4	Input - (Pin 19)	V_{IN}	V_{GEN1}	Vac
5	Input - (Pin 9)	V_{IN}	V_{GEN2}	Vac
6	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
7	Pulse Frequency Square Wave	f_{GEN1}	400k ± 20% 50% Duty Cycle	Hz
8	Pulse Square Wave	GEN2	One 60µs positive pulse each 265µs	Vac
9	Positive Supply Voltage (Pin 40)	V_{DD}	+5.5(+0−0.5)	V
10	Negative Supply Voltage (Pin 20)	V_{SS}	0	V

NOTES

1. Input Protection Resistor = Output Load = 1.0kΩ.
2. V_{GEN1}



V_{GEN2}

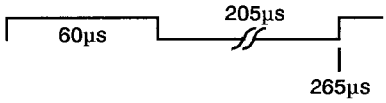
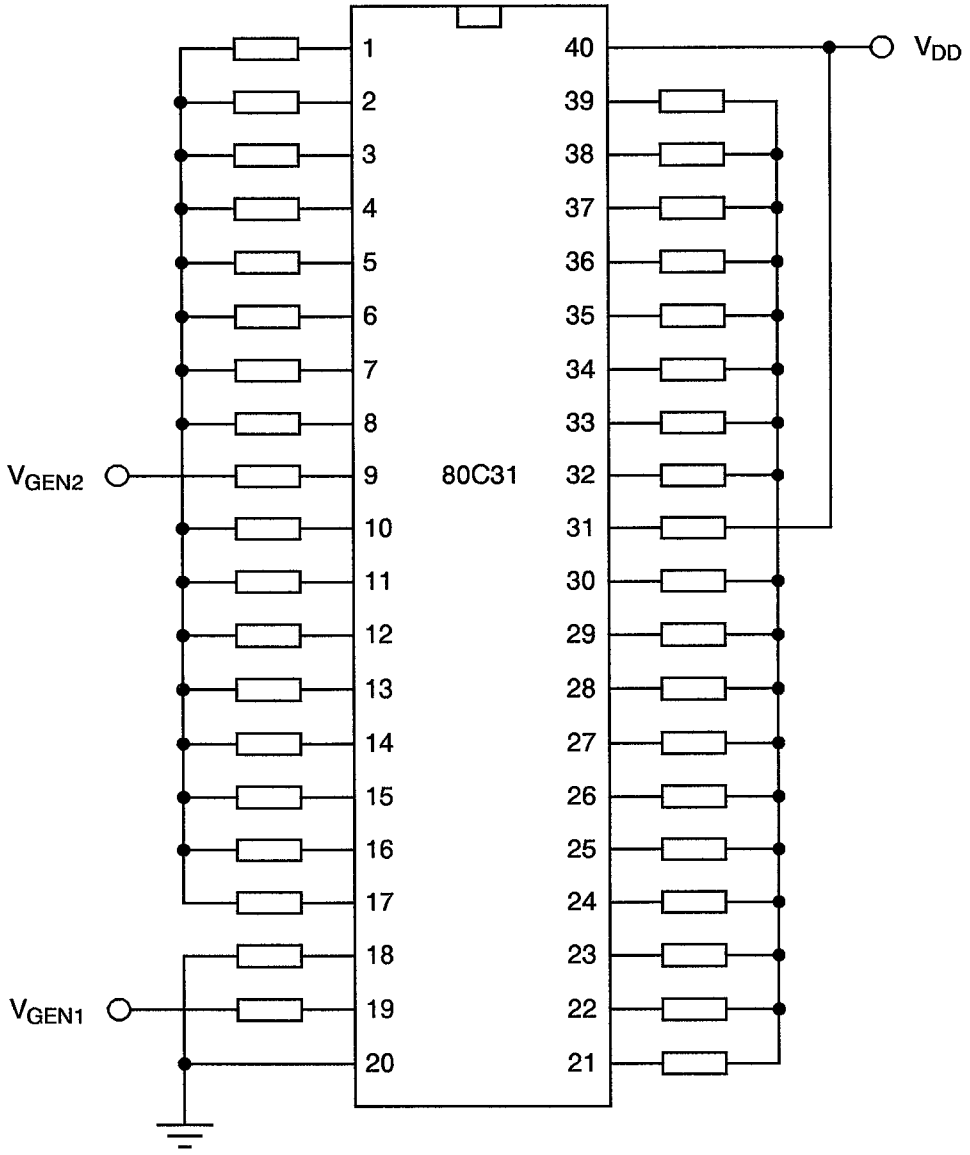


FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5 of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Functional Test 1	-	As per Table 2	As per Table 2	-	-	-
2	Functional Test 2	-	As per Table 2	As per Table 2	-	-	-
3	Functional Test 3	-	As per Table 2	As per Table 2	-	-	-
4	Functional Test 4	-	As per Table 2	As per Table 2	-	-	-
5	Functional Test 5	-	As per Table 2	As per Table 2	-	-	-
6	Functional Test 6	-	As per Table 2	As per Table 2	-	-	-
7	Functional Test 7	-	As per Table 2	As per Table 2	-	-	-
8	Functional Test 8	-	As per Table 2	As per Table 2	-	-	-
9 to 12	Quiescent Current 1	I_{DD1}	As per Table 2	As per Table 2	-	Table 2	mA
13 to 16	Quiescent Current 2	I_{DD2}	As per Table 2	As per Table 2	-	Table 2	mA
17 to 20	Quiescent Current 3	I_{DD3}	As per Table 2	As per Table 2	-	Table 2	mA
21 to 24	Supply Current 1	$I_{DD(S1)}$	As per Table 2	As per Table 2	-	Table 2	mA
25 to 28	Supply Current 2	$I_{DD(S2)}$	As per Table 2	As per Table 2	-	Table 2	mA
29 to 32	Supply Current 3	$I_{DD(S3)}$	As per Table 2	As per Table 2	-	Table 2	mA
33	Power Down Supply Current 1	$I_{DD(PD1)}$	As per Table 2	As per Table 2	-	75	µA
34	Power Down Supply Current 2	$I_{DD(PD2)}$	As per Table 2	As per Table 2	-	75	µA
35 to 42	Input Leakage Current Low Level 1	I_{IL1}	As per Table 2	As per Table 2	−10	10	µA
43	Input Leakage Current Low Level 2	I_{IL2}	As per Table 2	As per Table 2	−10	10	µA
44 to 51	Input Leakage Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	−10	10	µA

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
52	Input Leakage Current High Level 2	I_{IH2}	As per Table 2	As per Table 2	−10	10	µA
53 to 76	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	−10	-	µA
77 to 100	High to Low Transition Current	I_{IT}	As per Table 2	As per Table 2	−750	-	µA
101 to 108	Output Voltage Low Level 1	V_{OL1}	As per Table 2	As per Table 2	-	0.45	V
109 to 132	Output Voltage Low Level 2	V_{OL2}	As per Table 2	As per Table 2	-	0.45	V
133 to 134	Output Voltage Low Level 3	V_{OL3}	As per Table 2	As per Table 2	-	0.45	V
135 to 142	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	2.4	-	V
143 to 166	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	2.4	-	V
167 to 174	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	3.375	-	V
175 to 199	Output Voltage High Level 4	V_{OH4}	As per Table 2	As per Table 2	3.375	-	V
200 to 207	Output Voltage High Level 5	V_{OH5}	As per Table 2	As per Table 2	4.05	-	V
208 to 232	Output Voltage High Level 6	V_{OH6}	As per Table 2	As per Table 2	4.04	-	V
233 to 234	Output Voltage High Level 7	V_{OH7}	As per Table 2	As per Table 2	2.4	-	V
235 to 236	Output Voltage High Level 8	V_{OH8}	As per Table 2	As per Table 2	3.375	-	V

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
237 to 238	Output Voltage High Level 9	V_{OH9}	As per Table 2	As per Table 2	4.05	-	V
239 to 276	Input Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	0.2	-	V
277 to 314	Input Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	−0.2	V
315	Reset Resistor	RRST	As per Table 2	As per Table 2	50	200	kΩ
316 to 357	Input/Output Capacitance		As per Table 2	As per Table 2	-	10	pF
358	ALE Pulse Width	TLHHL-1	As per Table 2	As per Table 2	111	-	ns
359	Address Valid to ALE	TAVLL-1	As per Table 2	As per Table 2	13	-	ns
360	Address Hold to ALE	TLLAX-1	As per Table 2	As per Table 2	33	-	ns
361	ALE to Valid Inst. In	TLLIV-1	As per Table 2	As per Table 2	213	-	ns
362	ALE to $\overline{PSEN}$	TLLPL-1	As per Table 2	As per Table 2	28	-	ns
363	$\overline{PSEN}$ Pulse Width	TPLPH-1	As per Table 2	As per Table 2	190	-	ns
364	$\overline{PSEN}$ to Valid Inst. In	TPLIV-1	As per Table 2	As per Table 2	115	-	ns
365	$\overline{PSEN}$ to In Instr. Hold	TPXIX-1	As per Table 2	As per Table 2	-	0	ns
366	$\overline{PSEN}$ to Address Valid	TPXAV-1	As per Table 2	As per Table 2	75	-	ns
367	Address to Valid Inst. In	TAVIV-1	As per Table 2	As per Table 2	265	-	ns
368	$\overline{RD}$ Pulse Width	TRLRH-1	As per Table 2	As per Table 2	400	-	ns
369	$\overline{WR}$ Pulse Width	TWLWH-1	As per Table 2	As per Table 2	400	-	ns
370	ALE to Data Address Hold	TLLAXR-1	As per Table 2	As per Table 2	33	-	ns
371	$\overline{RD}$ to Valid Data In	TRLDV-1	As per Table 2	As per Table 2	232	-	ns
372	$\overline{RD}$ to Data Hold	TRHDX-1	As per Table 2	As per Table 2	-	0	ns
373	$\overline{RD}$ to Data Float	TRHDZ-1	As per Table 2	As per Table 2	82	-	ns
374	ALE to Valid Data In	TLLDV-1	As per Table 2	As per Table 2	496	-	ns
375	Address to Valid Data In	TAVDV-1	As per Table 2	As per Table 2	564	-	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS (CONT'D)

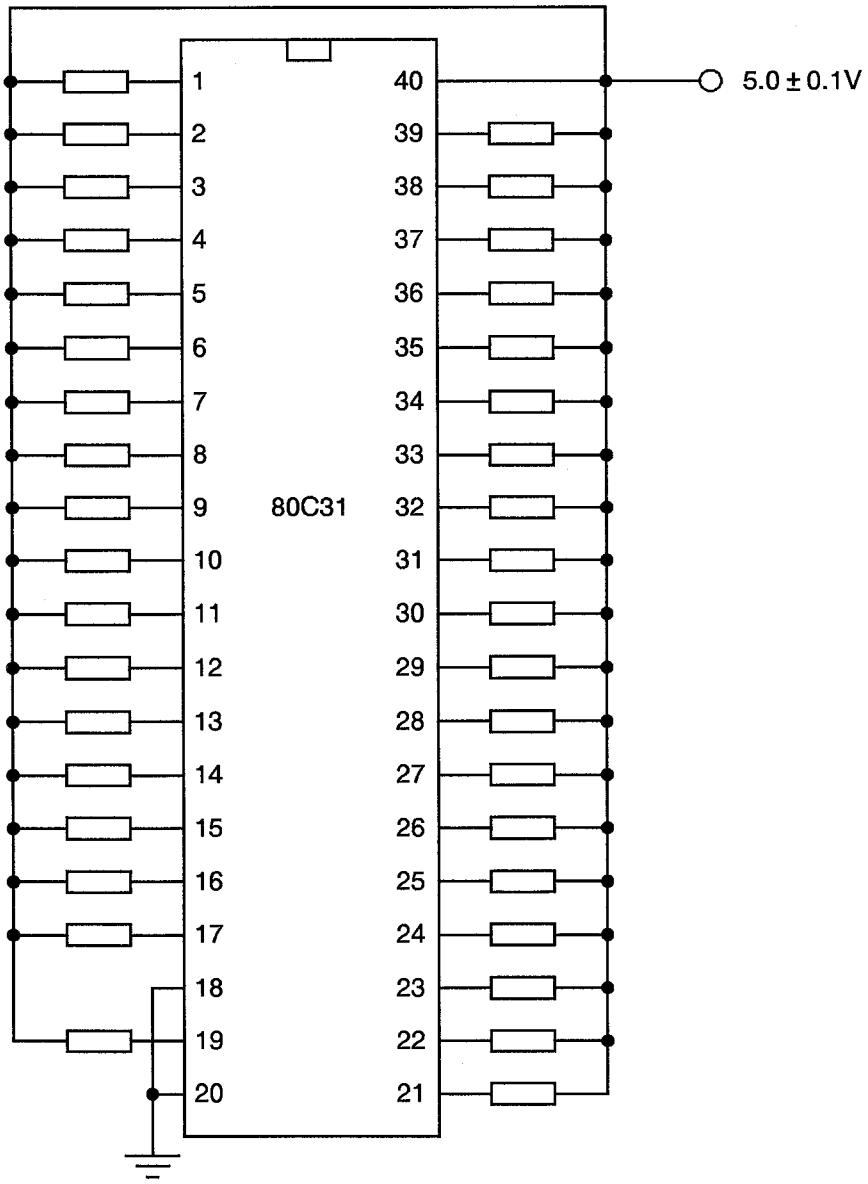
No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX.	
376	ALE to $\overline{WR}$	TLLWL-1	As per Table 2	As per Table 2	185	315	ns
377	ALE to $\overline{RD}$	TLLRL-1	As per Table 2	As per Table 2	185	315	ns
378	Address to $\overline{WR}$	TAVWL-1	As per Table 2	As per Table 2	187	-	ns
379	Address to $\overline{RD}$	TAVRL-1	As per Table 2	As per Table 2	187	-	ns
380	Data Valid to $\overline{WR}$	TQVWX-1	As per Table 2	As per Table 2	8.0	-	ns
381	Data Setup to $\overline{WR}$ High	TQVWH-1	As per Table 2	As per Table 2	431	-	ns
382	$\overline{WR}$ to Data Hold	TWHQX-1	As per Table 2	As per Table 2	18	-	ns
383	$\overline{RD}$ Low to Address Float	TRLAZ-1	As per Table 2	As per Table 2	-	0	ns
384	$\overline{WR}$ High to ALE High	TWHLH-1	As per Table 2	As per Table 2	18	184	ns
385	$\overline{RD}$ High to ALE High	TRHLH-1	As per Table 2	As per Table 2	18	184	ns
386	Serial Port Clock Cycle Time	TXLXL-1	As per Table 2	As per Table 2	999	1001	ns
387	Out Data Setup to Clock	TQVXH-1	As per Table 2	As per Table 2	700	-	ns
388	Clock to Out Data Hold	TXHQX-1	As per Table 2	As per Table 2	49	-	ns
389	Clock to In Data Hold	TXHDX-1	As per Table 2	As per Table 2	-	0	ns
390	Clock High to In Data Valid	TXHDV-1	As per Table 2	As per Table 2	700	-	ns
391	ALE Pulse Width	TLHLL-2	As per Table 2	As per Table 2	111	-	ns
392	Address Valid to ALE	TAVLL-2	As per Table 2	As per Table 2	13	-	ns
393	Address Hold to ALE	TLLAX-2	As per Table 2	As per Table 2	33	-	ns
394	ALE to Valid Inst. In	TLLIV-2	As per Table 2	As per Table 2	213	-	ns
395	ALE to $\overline{PSEN}$	TLLPL-2	As per Table 2	As per Table 2	28	-	ns
396	$\overline{PSEN}$ Pulse Width	TPLPH-2	As per Table 2	As per Table 2	190	-	ns
397	$\overline{PSEN}$ to Valid Inst. In	TPLIV-2	As per Table 2	As per Table 2	115	-	ns
398	$\overline{PSEN}$ to In Inst. Hold	TPXIX-2	As per Table 2	As per Table 2	-	0	ns
399	$\overline{PSEN}$ to Address Valid	TPXAV-2	As per Table 2	As per Table 2	75	-	ns
400	Address to Valid Inst. In	TAVIV-2	As per Table 2	As per Table 2	265	-	ns
401	$\overline{RD}$ Pulse Width	TRLRH-2	As per Table 2	As per Table 2	400	-	ns
402	$\overline{WR}$ Pulse Width	TWLWH-2	As per Table 2	As per Table 2	400	-	ns
403	ALE to Data Address Hold	TLLAXR-2	As per Table 2	As per Table 2	33	-	ns
404	$\overline{RD}$ to Valid Data In	TRLDV-2	As per Table 2	As per Table 2	232	-	ns
405	$\overline{RD}$ to Data Hold	TRHDX-2	As per Table 2	As per Table 2	-	0	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
406	$\overline{RD}$ to Data Float	TRHDZ-2	As per Table 2	As per Table 2	82	-	ns
407	ALE to Valid Data In	TLLDV-2	As per Table 2	As per Table 2	496	-	ns
408	Address to Valid Data In	TAVDV-2	As per Table 2	As per Table 2	564	-	ns
409	ALE to $\overline{WR}$	TLLWL-2	As per Table 2	As per Table 2	185	315	ns
410	ALE to $\overline{RD}$	TLLRL-2	As per Table 2	As per Table 2	185	315	ns
411	Address to $\overline{WR}$	TAVWL-2	As per Table 2	As per Table 2	187	-	ns
412	Address to $\overline{RD}$	TAVRL-2	As per Table 2	As per Table 2	187	-	ns
413	Data Valid to $\overline{WR}$	TQVWX-2	As per Table 2	As per Table 2	8.0	-	ns
414	Data Setup to $\overline{WR}$ High	TQVWH-2	As per Table 2	As per Table 2	431	-	ns
415	$\overline{WR}$ to Data Hold	TWHQX-2	As per Table 2	As per Table 2	18	-	ns
416	$\overline{RD}$ Low to Address Float	TRLAZ-2	As per Table 2	As per Table 2	-	0	ns
417	$\overline{WR}$ High to ALE High	TWHLH-2	As per Table 2	As per Table 2	18	184	ns
418	$\overline{RD}$ High to ALE High	TRHLH-2	As per Table 2	As per Table 2	18	184	ns
419	Serial Port Clock Cycle Time	TXLXL-2	As per Table 2	As per Table 2	999	1001	ns
420	Out Data Setup to Clock	TQVXH-2	As per Table 2	As per Table 2	700	-	ns
421	Clock to Out Data Hold	TXHQX-2	As per Table 2	As per Table 2	49	-	ns
422	Clock to In Data Hold	TXHDX-2	As per Table 2	As per Table 2	-	0	ns
423	Clock High to In Data Valid	TXHDV-2	As per Table 2	As per Table 2	700	-	ns

NOTES: See Page 42.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Input/Output Protection Resistor = 1.0kΩ.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
17 to 20	Quiescent Current 3	I_{DD3}	As per Table 2	As per Table 2	- - - -	8.0 9.0 15 20	mA
21 to 24	Supply Current 1	$I_{DD(S1)}$	As per Table 2	As per Table 2	- - - -	10 14 21.5 30	mA
34	Power Down Supply Current 2	$I_{DD(PD2)}$	As per Table 2	As per Table 2	-	1.0	mA
35 to 42	Input Leakage Current Low Level 1	I_{IL1}	As per Table 2	As per Table 2	−10	10	µA
43	Input Leakage Current Low Level 2	I_{IL2}	As per Table 2	As per Table 2	−10	10	µA
44 to 51	Input Leakage Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	−10	10	µA
52	Input Leakage Current High Level 2	I_{IH2}	As per Table 2	As per Table 2	−10	10	µA
53 to 76	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	−75	-	µA
77 to 100	High to Low Transition Current	I_{IT}	As per Table 2	As per Table 2	−750	-	µA
101 to 108	Output Voltage Low Level 1	V_{OL1}	As per Table 2	As per Table 2	-	0.45	V
109 to 132	Output Voltage Low Level 2	V_{OL2}	As per Table 2	As per Table 2	-	0.45	V
133 to 134	Output Voltage Low Level 3	V_{OL3}	As per Table 2	As per Table 2	-	0.45	V
135 to 142	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	2.4	-	V
143 to 166	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	2.4	-	V
233 to 234	Output Voltage High Level 7	V_{OH7}	As per Table 2	As per Table 2	2.4	-	V

NOTES: See Page 42.