

Pages 1 to 17

TRANSISTORS, POWER, MOSFET, N-CHANNEL, RAD-HARD

BASED ON TYPE BUY10CS12J-01

ESCC Detail Specification No. 5205/028

Issue 1	March 2012
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ISSUE 1

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ISSUE 1

TABLE OF CONTENTS

<u>1.</u>	<u>GENERAL</u>	<u>5</u>
1.1	Scope	5
1.2	Applicable Documents	5
1.3	Terms, Definitions, Abbreviations, Symbols and Units	5
1.4	The ESCC Component Number and Component Type Variants	5
1.4.1	The ESCC Component Number	5
1.4.2	Component Type Variants	5
1.5	Maximum Ratings	6
1.6	Handling Precautions	7
1.7	Physical Dimensions and Terminal Identification	8
1.7.1	Leadless Chip Carrier Package (SMD0.5) - 3 Terminals	8
1.8	Functional Diagram	9
1.9	Materials and Finishes	9
<u>2.</u>	REQUIREMENTS	<u>9</u>
2.1	General	9
2.1.1	Deviations from the Generic Specification	9
2.1.1.1	Deviations from Screening Tests - Chart F3	9
2.1.1.2	Deviations from Qualification and Periodic Testes - Chart F4	10
2.2	Marking	10
2.3	Wafer Lot Acceptance	10
2.4	Electrical Measurements at Room, High and Low Temperatures	10
2.4.1	Room Temperature Electrical Measurements	10
2.4.2	High and Low Temperatures Electrical Measurements	12
2.4.3	Notes to Room, High and Low Temperatures Electrical Measurements	12
2.5	Parameter Drift Values	12
2.6	Intermediate and End-Point Electrical Measurements	13
2.7	High Temperature Reverse Bias Burn-in Conditions	14
2.8	High Temperature Steady-State Gate Bias Burn-in Conditions	14
2.9	Operating Life Conditions	14
2.10	Total Dose Radiation Testing	15
2.10.1	Bias Conditions and Total Dose Level for Total Dose Radiation Testing	15
2.10.2	Electrical Measurements for Total Dose Radiation Testing	15
APPENDIX	('A'	16



1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 <u>APPLICABLE DOCUMENTS</u>

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 5000
- (b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices
- (c) MIL-STD-883, Test Method Standard Microelectronics

1.3 <u>TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS</u>

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 <u>The ESCC Component Number</u>

The ESCC Component Number shall be constituted as follows:

Example: 520502801R

Detail Specification Reference: 5205028Component Type Variant Number: 01

Total Dose Radiation Level Letter: R (as required)

1.4.2 <u>Component Type Variants</u>

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case (Note 1)	Weight max (g)	Total Dose Radiation Level Letter (Note 2)
01	BUY10CS12J-01	SMD0.5	1.1	R [100kRAD(Si)]

NOTES:

- 1. See Physical Dimensions and Terminal Identification.
- 2. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.



1.5 <u>MAXIMUM RATINGS</u>

The maximum ratings shall not be exceeded at any time during use or storage.

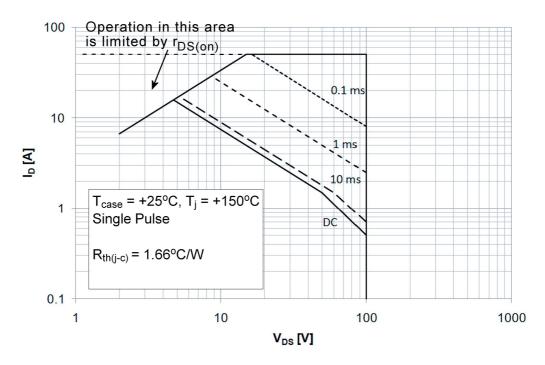
Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Drain-Source Voltage	V _{DS}	100	V	Note 1
Gate-Source Voltage	V_{GS}	±20	V	
Drain Current (Continuous)	I _{DS}	12.4	А	At T _{case} ≤+25°C Notes 1, 2, 3
Drain Current (Continuous)	I _{DS}	8	А	At T _{case} =+100°C Notes 2, 3
Drain Current (Pulsed)	I _{DM}	50	Apk	At T _{case} ≤+25°C Notes 1, 2,
Power Dissipation	P _{tot}	75	W	Note 4
Avalanche Energy (Single Pulse)	E _{AS}	60	mJ	
Operating Temperature Range	T _{op}	-55 to +150	°C	T _{amb}
Storage Temperature Range	T _{stg}	-55 to +150	°C	
Junction Temperature	T _j	+150	°C	
Soldering Temperature	T _{sol}	+250	°C	Note 5
Thermal Resistance, Junction-to-Case	R _{th(j-c)}	1.66	°C/W	

NOTES:

1. Safe Operating Area applies as follows:





- $\rm T_{case}$ is measured on the PCB at the soldering point to the Drain terminal. For $\rm T_{case}$ >+25°C, derate as follows:

$$I_{DS} = \sqrt{\frac{T_{jmax} - T_{case}}{(R_{th(j-c)}) \times (r_{DS(on)}at T_{jmax})}}$$

Where $r_{DS(on)}$ at $T_{jmax} = 490 \text{m}\Omega$

- For $T_{case} > +25$ °C, derate linearly to 0W at $T_{case} = +150$ °C.
- Duration 10 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

HANDLING PRECAUTIONS 1.6

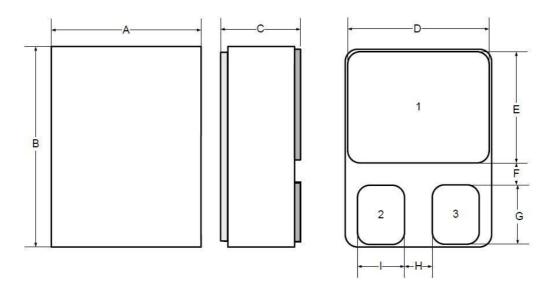
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1000V.



1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 <u>Leadless Chip Carrier Package (SMD0.5) - 3 Terminals</u>



Symbols	Dimensions mm				
	Min	Max			
A	7.35	7.69			
В	9.97	10.41			
С	-	3.3			
D	7.14	7.39			
E	5.59	5.84			
F	0.76	-			
G	2.92	3.18			
Н	0.76	-			
I	2.29	2.54			

NOTES:

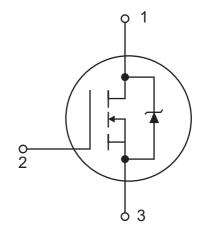
1. Terminal identification: terminal 1 = Drain, terminal 2 = Gate, terminal 3 = Source.



1.8 <u>FUNCTIONAL DIAGRAM</u>

Terminal 1: Drain
Terminal 2: Gate

Terminal 3: Source



NOTES:

1. The case is not connected to any terminal.

1.9 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

- a) Case
 - The case shall be hermetically sealed and have a ceramic/metal body.
- b) Terminals

The terminal material and finish shall be Q14 in accordance with the requirements of ESCC Basic Specification No. 23500.

2. <u>REQUIREMENTS</u>

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

- (a) Verification of Safe Operating Area: The Safe Operating Area shall be verified by performing the Thermal Impedance $(Z_{th(i-s)}) \Delta V_{SD}$ test specified in Room Temperature Electrical Measurements.
- (b) Particle Impact Noise Detection may be performed at any point after Temperature Cycling, prior to Seal.
- (c) Power Burn-in: A high temperature steady-state gate bias test (HTGB) shall be performed instead



of Power Burn-in.

2.1.1.2 Deviations from Qualification and Periodic Testes - Chart F4

(a) Terminal Strength is not applicable.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) The ESCC qualified components symbol (for ESCC qualified components only).
- (b) The ESCC Component Number.
- (c) Traceability information.

2.3 <u>WAFER LOT ACCEPTANCE</u>

A SEM inspection shall be performed as specified in the ESCC Generic Specification.

2.4 <u>ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES</u>

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.4.1 Room Temperature Electrical Measurements

Unless otherwise specified, the measurements shall be performed at T_{amb} =+25 $\pm 3^{o}$ C.

Characteristics	Symbols	MIL-STD-	Test Conditions		nits	Units
		750 Test Method		Min	Max	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	3407	V _{GS} =0V I _D =0.25mA Bias condition C	100		V
Gate-to-Source Threshold Voltage	V _{GS(th)}	3403	V _{DS} ≥V _{GS} I _D =1mA	2	4	V
Gate-to-Source Leakage Current	I _{GSS}	3411	V _{GS} =±20V V _{DS} =0V Bias condition C	-100	+100	nA
Drain Current	I _{DSS}	3413	V _{GS} =0V V _{DS} =80V Bias condition C	-	25	μΑ
Static Drain-to- Source On Resistance	r _{DS(on)}	3421	V _{GS} =10V I _D =8A Note 1	-	130	mΩ



ISSUE 1

Characteristics	Symbols	MIL-STD-	Test Conditions	Lin	nits	Units
		750 Test Method		Min	Max	
Source-to-Drain Diode Forward Voltage	V _{SD}	4011	V _{GS} =0V I _{SD} =12.4A Note 1	-	1.2	V
Thermal Impedance,	Z _{th(j-c)}	3161	Note 2	-	1.14	°C/W
Turn-on Delay Time	t _{d(on)}	3472	V_{GS} =10 V, R_{G} =4.7 Ω V_{DS} =50V, I_{D} =8A Note 3	-	25	ns
Rise Time	t _r	3472	V_{GS} =10 V, R_{G} =4.7 Ω V_{DS} =50V, I_{D} =8A Note 3	-	35	ns
Turn-off Delay Time	t _{d(off)}	3472	V_{GS} =10 V, R _G =4.7 Ω V _{DS} =50V, I _D =8A Note 3	-	35	ns
Fall Time	t _f	3472	V_{GS} =10V, R_{G} =4.7 Ω V_{DS} =50V, I_{D} =8A Note 3	-	20	ns
Reverse Recovery Time	t _{rr}	3473	$V_{DD} \le 50V$, di/dt=100A/ μ s $I_{SD} = 12.4A$ Note 3	-	400	ns
Input Capacitance	C _{iss}	3431	V _{GS} =0V, V _{DS} =100V f=1MHz Note 3	1.3	1.9	nF
Output Capacitance	C _{oss}	3453	V _{GS} =0V, V _{DS} =100V f=1MHz Note 3	90	150	pF
Reverse Transfer Capacitance	C _{rss}	3433	V _{GS} =0V, V _{DS} =100V f=1MHz Note 3	1	6	pF
Total Gate Charge	Qg	3471	V_{GS} =10V, V_{DS} =50V, I_{D} =12.4A Note 3	-	42	nC
Gate-to-Source Charge	Q _{gs}	3471	V_{GS} =10V, V_{DS} =50V, I_{D} =12.4A Note 3	-	15	nC
Gate-to-Drain Charge	Q _{gd}	3471	V_{GS} =10V, V_{DS} =50V, I_{D} =12.4A Note 3	-	15	nC



2.4.2 <u>High and Low Temperatures Electrical Measurements</u>

Characteristics	Symbols	MIL-STD-750	Test Conditions	Lin	nits	Units
		Test Method	Note 4	Min	Max	
Gate-to-Source Threshold Voltage	V _{GS(th)}	3403	T _{amb} =+125(+0-5) ^o C V _{DS} ≥V _{GS} I _D =1mA	1.5	-	V
			T _{amb} =-55(+5-0)°C V _{DS} ≥V _{GS} I _D =1mA	-	5	V
Gate-to-Source Leakage Current	I _{GSS}	3411	T _{amb} =+125(+0-5) ^o C V _{GS} =±20V, V _{DS} =0V Bias condition C	-200	+200	nA
Drain Current	I _{DSS}	3413	T _{amb} =+125(+0-5) ^o C V _{GS} =0V V _{DS} =80V Bias condition C	-	250	μА
Static Drain-to- Source On Resistance	r _{DS(on)}	3421	T _{amb} =+125(+0-5)°C V _{GS} =10V I _D =8A Note 1	-	300	mΩ

2.4.3 Notes to Room, High and Low Temperatures Electrical Measurements

- 1. Pulsed measurement: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- 2. The $Z_{th(j-c)}$ limit is guaranteed by performing a ΔV_{SD} (go-no-go) test. The following test conditions and limits shall apply:
 - V_{DS} = 20V
 - t_M <75μs
 - I_M = 10mA
 - t_H = 25ms
 - I_H = 1.2A
 - V_{SD} = 40mV minimum, 60mV maximum
- Read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively a 100% inspection may be performed.
- Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} =+25 ±3 o C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.



Characteristics	Symbols		Units		
		Drift	Abso	olute	
		Value Δ	Min	Max	
Gate-to-Source Threshold Voltage	V _{GS(th)}	±20%	2	4	V
Gate-to-Source Leakage Current	I _{GSS}	±20 or (1) ±100%	-100	+100	nA
Drain Current	I _{DSS}	±10 or (1) ±100%	-	25	μΑ
Static Drain-to-Source On Resistance (Note 2)	r _{DS(on)}	±20% (3)	-	130	mΩ

NOTES:

- 1. Whichever is greater.
- 2. Measured only prior to HTRB Burn-in and after HTGB Burn-in.
- 3. Referred to the measurement prior to HTRB Burn-in.

2.6 <u>INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS</u>

Unless otherwise specified, the measurements shall be performed at T_{amb} =+25 $\pm 3^{o}$ C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols		Limits		
		Drift	Abs	Absolute	
		Value Δ	Min	Max	
Gate-to-Source Threshold Voltage	V _{GS(th)}	±20%	2	4	V
Gate-to-Source Leakage Current	I _{GSS}	±20 or (1) ±100%	-100	+100	nA
Drain Current	I _{DSS}	±10 or (1) ±100%	-	25	μΑ
Static Drain-to-Source On Resistance	r _{DS(on)}	±20%	-	130	mΩ

NOTES:

1. Whichever is greater.



2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

HTRB Burn-in shall be performed in accordance with MIL-STD-750, Test Method 1042, Test Condition A with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T _{amb}	+150(+0-5)	°C
Drain-to-Source Voltage	V _{DS}	80 (Note 1)	V
Gate-to-Source Voltage	V_{GS}	0	V
Duration	t	240 minimum	hours

NOTES:

1. Voltage may be switched off during cool down.

2.8 HIGH TEMPERATURE STEADY-STATE GATE BIAS BURN-IN CONDITIONS

HTGB Burn-in shall be performed in accordance with MIL-STD-750, Test Method 1042, Test Condition B with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T _{amb}	+150(+0-5)	°C
Drain-to-Source Voltage	V _{DS}	0	V
Gate-to-Source Voltage	V _{GS}	16	V
Duration	t	48 minimum	hours

2.9 OPERATING LIFE CONDITIONS

Operating Life shall consist of High Temperature Reverse Bias in accordance with MIL-STD-750, Test Method 1042, Test Condition A, followed by High Temperature Steady-State Gate Bias in accordance with MIL-STD-750, Test Method 1042, Test Condition B. The test conditions are as follows:

High Temperature Reverse Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T _{amb}	+150(+0-5)	°C
Drain-to-Source Voltage	V _{DS}	80 (Note 1)	V
Gate-to-Source Voltage	V _{GS}	0	V
Duration	t	1000 minimum	Hours

High Temperature Steady-State Gate Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T _{amb}	+150(+0-5)	°C
Drain-to-Source Voltage	V _{DS}	0	V
Gate-to-Source Voltage	V _{GS}	16	V



Characteristics	Symbols	Test Conditions	Units
Duration	t	1000 minimum	hours

NOTES:

1. Voltage may be switched off during cool down.

2.10 <u>TOTAL DOSE RADIATION TESTING</u>

2.10.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

The following bias condition shall be used during irradiation testing:

 $V_{GS} = +15V$

 $V_{DS} = 0V$

The total dose level applied shall be as specified in Component Type Variants herein or in the Purchase Order.

2.10.2 <u>Electrical Measurements for Total Dose Radiation Testing</u>

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at $T_{amb} = 25\pm3^{\circ}C$.

Unless otherwise specified the test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below.

Characteristics	Symbols	Symbols Limits			Units
		Drift Values	Absolute		
		(Δ)	Min	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	±20%	100	-	V
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	+10%, -50%	2	4	V
Gate-to-Source Leakage Current	I _{GSS}	±20	-100	+100	nA
Drain Current	I _{DSS}	_	-	25	μΑ
Static Drain-to-Source On Resistance	r _{DS(on)}	±20%	-	130	mΩ
Source-to-Drain Diode Forward Voltage	V _{SD}	±10%	-	1.2	V





APPENDIX 'A'

AGREED DEVIATIONS FOR INFINEON TECHNOLOGIES (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control (Chart F2)	The 3 component sample Dimension Check need only be performed once on each component package production lot.
Deviations from Screening Tests (Chart F3)	Temperature Cycling shall be performed in accordance with MIL-STD-883, Test Method 1010, Test Condition C, 20 cycles at maximum storage temperature rating specified in the Detail Specification.
	High and Low Temperatures Electrical Measurements may be performed at any point after High Temperature Steady-State Gate Bias Burn-in, prior to Seal, but shall still count towards Check for Lot Failure.
	Radiographic Inspection is not applicable.
	Seal, Fine Leak shall be performed in accordance with MIL-STD-883, Test Method 1014, Test Condition A1 or A2.
	Solderability is not applicable unless otherwise stipulated in the Purchase Order.
Deviations from Qualification and Periodic Tests (Chart F4)	Temperature Cycling shall be performed in accordance with MIL-STD-883, Test Method 1010, Test Condition C, 100 cycles at maximum storage temperature rating specified in the Detail Specification.
	Seal, Fine Leak shall be performed in accordance with MIL-STD-883, Test Method 1014, Test Condition A1 or A2.
Room Temperature Electrical Measurements	The read and record 32 component sample electrical measurements for characteristics $t_{d(on)}$, t_r , $t_{d(off)}$, t_f , t_{rr} , C_{iss} , C_{oss} , C_{rss} , Q_g , Q_{gs} and Q_{gd} need only be performed once on each wafer lot used to supply components to this specification. Any failure shall result in rejection of the wafer lot. The sample measurement may be performed at any time during production.
Marking	For the purposes of marking of the ESCC Component Number on the body of the component, the Variant Number may be marked as a single digit (e.g. 1 for Variant 01). Otherwise the full ESCC Component Number shall be used.
Operating Life Conditions - High Temperature Reverse Bias Conditions	The Drain-to-Source Voltage to be applied during the High Temperature Reverse Bias Operating Life test shall be V _{DS} = 100V.

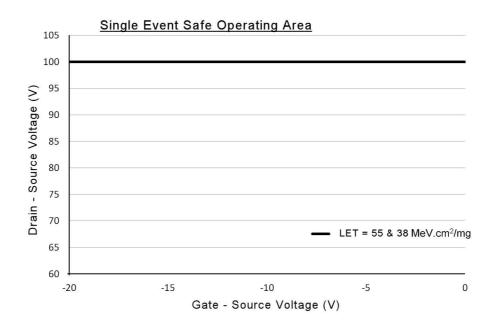


ADDITIONAL DATA - INFINEON TECHNOLOGIES (D)

(a) Derating for Space Application

(i) Single Event Effects Safe Operating Area

These components are susceptible to Single Event Gate Rupture if operated in a space environment unless the following derating is applied:



(ii) Derating of Drain-to-Source Voltage

The generic requirement of ECSS-Q-ST-30-11 to derate Drain-to-source Voltage during use is not applicable to the components specified herein.