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INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS DIGITAL, FIELD PROGRAMMABLE GATE ARRAY, 40000 GATES

BASED ON TYPE AT40KEL040

ESCC Detail Specification No. 9304/008

Issue 2	April 2012

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
697	Specification upissued to incorporate editorial and technical changes per DCR.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930400801R

- Detail Specification Reference: 9304008
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g	Total Dose Radiation Level Letter
01	AT40KEL040	MQFP-F160	G2	7	R [100kRAD (Si)]
02	AT40KEL040	MQFP-F256	D2	14	R [100kRAD (Si)]

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the purchase order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 5.5	V	Note 1
Input Voltage Range	V_{IN}	-0.5 to V_{DD} +0.5	V	Notes 1, 2
Output Voltage Range	V_{OUT}	-0.5 to V_{DD} +0.5	V	Notes 1, 2
Device Power Dissipation	P_D	4	W	
Operating Temperature Range	T_{op}	-55 to +125	^oC	
Storage Temperature	T_{stg}	-65 to +150	^oC	-
Soldering Temperature	T_{sol}	+300	^oC	Note 3
Junction Temperature Max	T_j	+150	^oC	
Thermal Resistance	R_{th}	2	$^oC/W$	

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 3.6V$ with reference to $V_{SS} = 0V$
2. V_{DD} +0.5V shall not exceed 5.5 V.
3. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

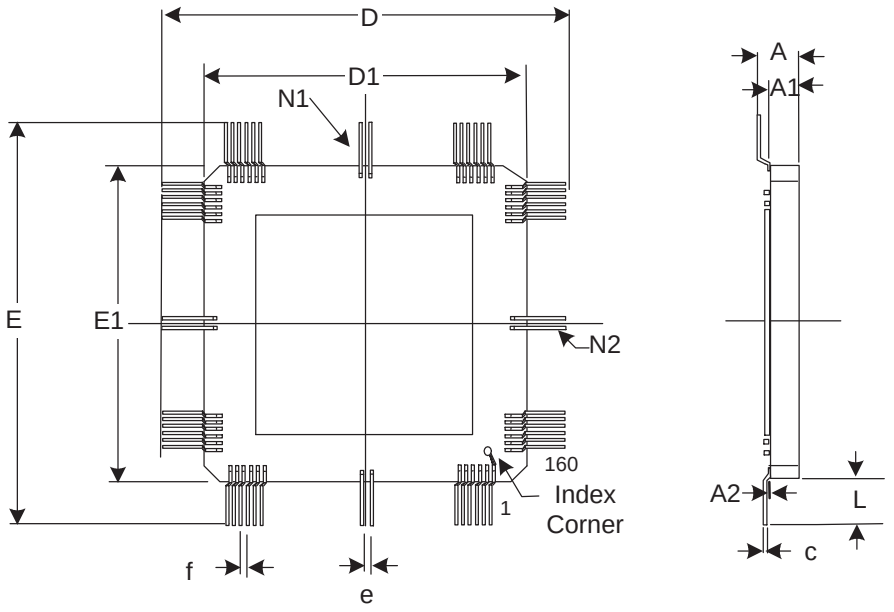
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 3 with Minimum Critical Path Failure Voltage of 4000V per ESCC Basic Specification No. 23800.

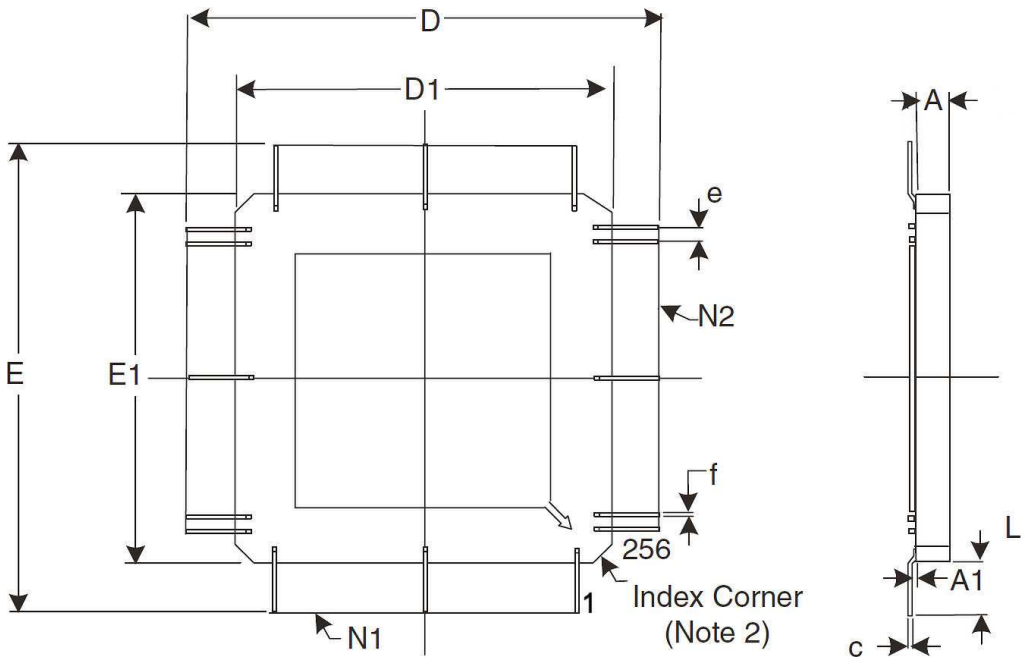
1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Multilayer Ceramic Quad Flat Package (MQFP-F160) - 160 Pins



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.96	2.66	
A1	1.7	2.1	
A2	0.1	0.3	
c	0.1	0.2	
D, E	37.9	39.3	
D1, E1	26.9	27.5	
e	0.65 BSC		
f	0.25	0.35	
L	5.5	5.9	
N1, N2	40		Each side

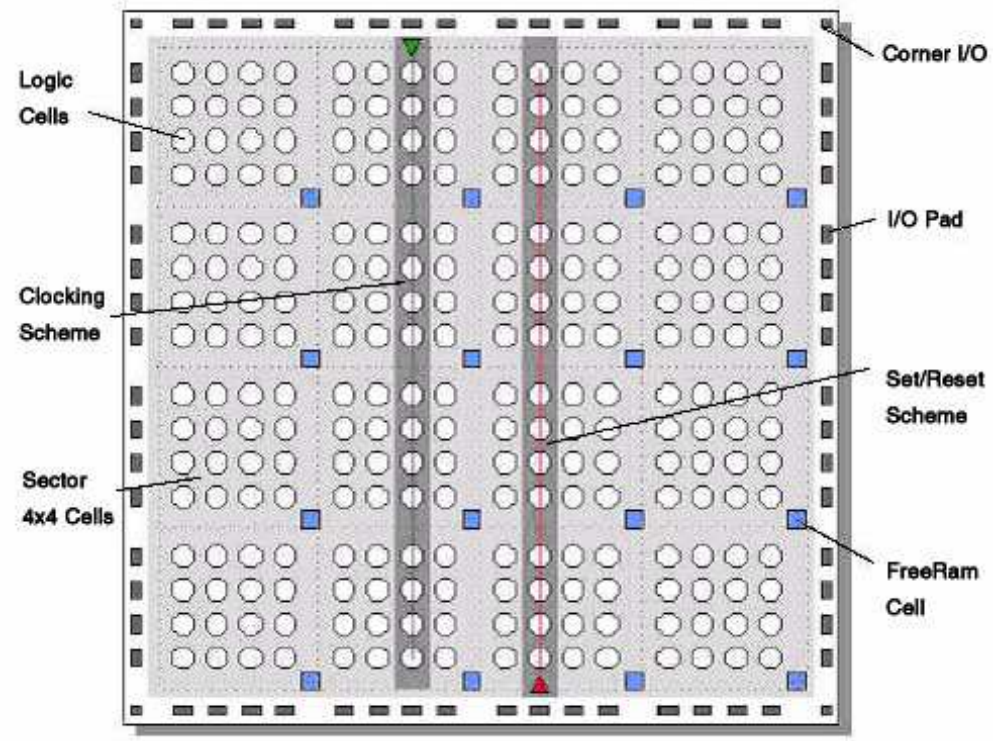
1.7.2 Multilayer Ceramic Quad Flat Package (MQFP-F256) - 256 Pins



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.06	2.56	
A1	0.05	0.36	
c	0.1	0.2	1
D/E	53.23	55.74	
D1/E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1/N2	31.9	32.11	3

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.
3. Each side (64 leads per side); this dimension is derived from 63 x dimension e.

1.8 ARRAY SCHEMATIC



1.9 PIN ASSIGNMENT

Pin	Function	
	MQFP-F160	MQFP-F256
1	V_{DD}	I/O384, GCLK8 (Global Clock), A15 (Address)
2	I/O384, GCLK8 (Global Clock), A15 (Address)	I/O383, A14 (Address)
3	I/O383, A14 (Address)	I/O382
4	I/O382	I/O381
5	I/O381	I/O378
6	I/O372, A13 (Address)	I/O377
7	I/O371, A12 (Address)	V_{SS}
8	I/O370	V_{DD}
9	I/O369	I/O375
10	V_{SS}	I/O374
11	I/O360	I/O372, A13 (Address)
12	I/O359	I/O371, A12 (Address)
13	I/O348, A11 (Address)	I/O370
14	I/O347, A10 (Address)	I/O369
15	I/O344	I/O366
16	I/O343	I/O365
17	I/O338, A9 (Address)	I/O362
18	I/O337, A8 (Address)	I/O360
19	V_{DD}	I/O359
20	V_{SS}	I/O358
21	I/O336, A7 (Address)	I/O356
22	I/O335, A6 (Address)	I/O355
23	I/O330	I/O353
24	I/O329	I/O352
25	I/O328	I/O349
26	I/O326, A5 (Address)	I/O348, A11 (Address)
27	I/O325, A4 (Address)	I/O347, A10 (Address)
28	I/O314	I/O346
29	I/O313	I/O344
30	V_{SS}	I/O343
31	I/O304	I/O338, A9 (Address)
32	I/O303	I/O337, A8 (Address)

Pin	Function	
	MQFP-F160	MQFP-F256
33	I/O298, A3 (Address)	I/O336, A7 (Address)
34	I/O297, CS1 (FPGA Configuration Chip Select), A2 (Address)	I/O335, A6 (Address)
35	I/O292	I/O334
36	I/O291	I/O330
37	I/O290, GCLK7 (Global Clock), A1 (Address)	I/O329
38	I/O289, A0 (Address)	I/O328
39	V_{SS}	I/O326, A5 (Address)
40	TESTCLOCK	I/O325, A4 (Address)
41	V_{DD}	I/O324
42	CCLK (Configuration Clock)	I/O323
43	I/O288, GCLK6 (Global Clock)	I/O321
44	I/O287, D0 (Data)	I/O320
45	I/O286	I/O318
46	I/O285	I/O317
47	I/O278	I/O314
48	I/O277, D1 (Data)	I/O313
49	I/O274	I/O312
50	I/O273	I/O311
51	V_{SS}	I/O308
52	I/O262, FCLK4 (Fast Clock)	I/O307
53	I/O261	I/O304
54	I/O260	I/O303
55	I/O259, D2 (Data)	I/O301
56	I/O246	I/O298, A3 (Address)
57	I/O245	V_{SS}
58	I/O242, CHECK (Configuration Control to Control the Check Function)	V_{DD}
59	I/O241, D3 (Data)	I/O297, CS1 (FPGA Configuration Chip Select), A2 (Address)
60	V_{SS}	I/O291
61	V_{DD}	I/O292
62	I/O240	I/O290, GCLK7 (Global Clock), A1 Address)
63	I/O239, D4 (Data)	I/O289, A0 (Address)

Pin	Function	
	MQFP-F160	MQFP-F256
64	I/O236	TESTCLOCK
65	I/O235	CCLK (Configuration Clock)
66	I/O222, CS0 (FPGA Configuration Chip Select)	I/O288, GCLK6 (Global Clock)
67	I/O221, D5 (Data)	I/O287, D0 (Data)
68	I/O220	I/O286
69	I/O219, FCLK3 (Fast Clock)	I/O285
70	V_{SS}	I/O282
71	I/O208	V_{SS}
72	I/O207	V_{DD}
73	I/O206	I/O278
74	I/O205, D6 (Data)	I/O277, D1 (Data)
75	I/O196	I/O276
76	I/O195	I/O274
77	I/O194, GCLK5 (Global Clock)	I/O273
78	I/O93, D7 (Data)	I/O272
79	RESETN	I/O270
80	V_{DD}	I/O269
81	CON (FPGA Configuration Start and Status)	I/O267
82	V_{SS}	I/O266
83	I/O192, GCLK4 (Global Clock)	I/O262, FCLK4 (Fast Clock)
84	I/O191, D8 (Data)	I/O261
85	I/O190	I/O260
86	I/O189	I/O259, D2 (Data)
87	I/O184, D9 (Data)	I/O258
88	I/O183, D10 (Data)	I/O257
89	I/O180	I/O254
90	I/O179	I/O253
91	V_{SS}	I/O252
92	I/O168	I/O251
93	I/O167	I/O248
94	I/O166, D11 (Data)	I/O246
95	I/O165, D12 (Data)	I/O245
96	I/O152	I/O242, CHECK (Configuration Control to Control the Check Function)

Pin	Function	
	MQFP-F160	MQFP-F256
97	I/O151	I/O241, D3 (Data)
98	I/O146, D13 (Data)	I/O240
99	I/O145, D14 (Data)	I/O239, D4 (data)
100	V_{SS}	I/O236
101	V_{DD}	I/O235
102	I/O144, INIT (Power-on-reset or Configuration Download)	I/O234
103	I/O143, D15 (Data)	I/O232
104	I/O138	I/O230
105	I/O137	I/O228
106	I/O124	I/O227
107	I/O123	I/O225
108	I/O122	I/O224
109	I/O121	I/O222, CS0 (FPGA Configuration Chip Select)
110	V_{SS}	I/O221, D5 (Data)
111	I/O110	I/O220
112	I/O109	I/O219, FCLK3 (Fast Clock)
113	I/O102, LDC (Low During Configuration)	I/O216
114	I/O101	I/O215
115	I/O100	I/O212
116	I/O99	I/O208
117	I/O98, HDC (High During Configuration)	I/O207
118	I/O97, GCLK3 (Global Clock)	I/O206
119	M2 (Mode)	I/O205, D6 (Data)
120	V_{DD}	I/O204
121	M0 (Mode)	V_{SS}
122	V_{SS}	V_{DD}
123	M1 (Mode)	I/O203
124	I/O96, GCLK2 (Global Clock)	I/O196
125	I/O95, OTS (Input to Immediately Tri-state all User I/O)	I/O195
126	I/O94	I/O194, GCLK5 (Global Clock)
127	I/O93	I/O193, D7 (Data)

Pin	Function	
	MQFP-F160	MQFP-F256
128	I/O90	RESETN
129	I/O89	CON (FPGA Configuration Start and Status)
130	I/O84	I/O192, GCLK4 (Global Clock)
131	I/O83	I/O191, D8 (Data)
132	V_{SS}	I/O190
133	I/O72, FCLK2 (Fast Clock)	I/O189
134	I/O71	I/O186
135	I/O70	V_{SS}
136	I/O69	V_{DD}
137	I/O54	I/O184, D9 (Data)
138	I/O53	I/O183, D10 (Data)
139	I/O50	I/O181
140	I/O49	I/O180
141	V_{DD}	I/O179
142	V_{SS}	I/O177
143	I/O48, A23 (Address)	I/O174
144	I/O47, A22 (Address)	I/O173
145	I/O44	I/O171
146	I/O43	I/O168
147	I/O28, A21 (Address)	I/O167
148	I/O27, A20 (Address)	I/O166, D11 (Data)
149	I/O26	I/O165, D12 (Data)
150	I/O25, FCLK1 (Fast Clock)	I/O163
151	V_{SS}	I/O162
152	I/O16	I/O161
153	I/O15	I/O158
154	I/O6, A19 (Address)	I/O157
155	I/O5, A18 (Address)	I/O156
156	I/O4	I/O152
157	I/O3	I/O151
158	I/O2, A17 (Address)	I/O150
159	I/O1, GCLK1 (Global Clock), A16 (Address)	I/O149
160	V_{SS}	I/O146, D13 (Data)

Pin	Function	
	MQFP-F160	MQFP-F256
161	-	I/O145, D14 (Data)
162	-	I/O144, INIT (Power-on-reset or Configuration Download
163	-	I/O143, D15 (Data)
164	-	I/O141
165	-	I/O138
166	-	I/O137
167	-	I/O136
168	-	I/O134
169	-	I/O132
170	-	I/O131
171	-	I/O129
172	-	I/O128
173	-	I/O124
174	-	I/O123
175	-	I/O122
176	-	I/O121
177	-	I/O120
178	-	I/O119
179	-	I/O116
180	-	I/O115
181	-	I/O113
182	-	I/O110
183	-	I/O109
184	-	I/O101
185	-	V_{SS}
186	-	V_{DD}
187	-	I/O102, LDC (Low During Configuration)
188	-	I/O99
189	-	I/O100
190	-	I/O98, HDC (High During Configuration)
191	-	I/O97, GCLK3 (Global Clock)
192	-	M2 (Mode)
193	-	M0 (Mode)

Pin	Function	
	MQFP-F160	MQFP-F256
194	-	M1 (Mode)
195	-	I/O96, GCLK2 (Global Clock)
196	-	I/O95, OTS (Input to Immediately Tri-state all User I/O)
197	-	I/O94
198	-	I/O93
199	-	V_{SS}
200	-	V_{DD}
201	-	I/O90
202	-	I/O89
203	-	I/O86
204	-	I/O85
205	-	I/O84
206	-	I/O83
207	-	I/O80
208	-	I/O79
209	-	I/O77
210	-	I/O76
211	-	I/O72, FCLK2 (Fast Clock)
212	-	I/O71
213	-	I/O70
214	-	I/O69
215	-	I/O67
216	-	I/O66
217	-	I/O63
218	-	I/O62
219	-	I/O60
220	-	I/O59
221	-	I/O57
222	-	I/O56
223	-	I/O54
224	-	I/O53
225	-	I/O50
226	-	I/O49
227	-	I/O48, A23 (Address)

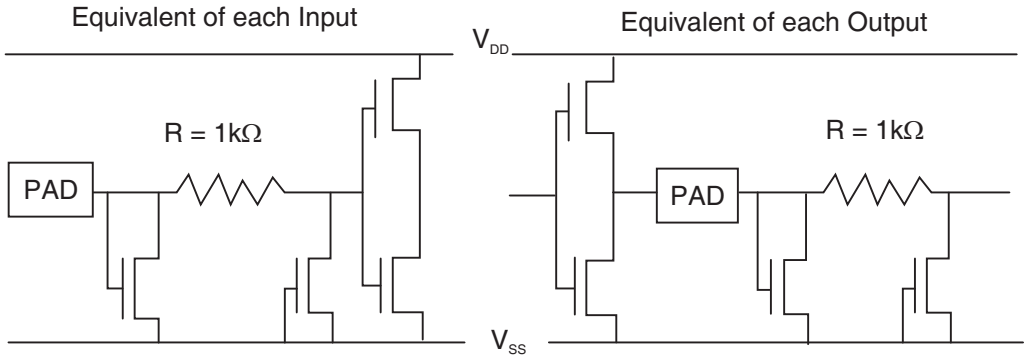
Pin	Function	
	MQFP-F160	MQFP-F256
228	-	I/O47, A22 (Address)
229	-	I/O44
230	-	I/O43
231	-	I/O41
232	-	I/O39
233	-	I/O36
234	-	I/O35
235	-	I/O34
236	-	I/O33
237	-	I/O30
238	-	I/O29
239	-	I/O28, A21 (Address)
240	-	I/O27, A20 (Address)
241	-	I/O26
242	-	I/O25, FCLK1 (Fast Clock)
243	-	I/O21
244	-	I/O20
245	-	I/O18
246	-	I/O16
247	-	I/O15
248	-	I/O13
249	-	V_{SS}
250	-	V_{DD}
251	-	I/O6, A19 (Address)
252	-	I/O5, A18 (Address)
253	-	I/O4
254	-	I/O3
255	-	I/O2, A17 (Address)
256	-	I/O1, GCLK1 (Global Clock), A16 (Address)

NOTES:

Pin Name	Type
A0-23	Inputs
CCLK	Input
CHECK	Input

Pin Name	Type
CON	Input
CS0-1	Inputs
D0-15	Inputs
FCLK1-4	Inputs
GCLK1-8	Inputs
HDC	Input
INIT	Input
I/O	Inputs/Outputs
LDC	Input
M0-2	Inputs
OTS	Input
RESETN	Input
TESTCLOCK	Input

1.10 PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Functional Test 1 Nominal Inputs	-	3014	Note 1, 3	-	-	-
Functional Test 2 Worst Case Inputs	-	3014	Note 1, 3	-	-	-
Functional Test 3 Worst Case Outputs	-	3014	Note 1, 3	-	-	-
Low Level Input Current	I_{IL}	3009	V_{IN}=0V, V_{DD}=3.6V, V_{SS}=0V	-	-5	µA
Low Level Input Current with Pull Up	I_{ILPU}	3009	V_{IN}=0V, V_{DD}=3.6V, V_{SS}=0V	-	-300	µA
High Level Input Current	I_{IH}	3010	V_{IN}=3.6V V_{DD}=3.6V, V_{SS}=0V	-	5	µA
High Level Input Current with Pull Down	I_{IHPD}	3010	V_{IN}=3.6V V_{DD}=3.6V, V_{SS}=0V	-	300	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
High Impedance Output Leakage Current, Low Level	I_{OZL}	3020	V_{OUT} =0V, V_{DD}=3.6V, V_{SS}=0V	-	-5	µA
High Impedance Output Leakage Current, Low Level with Pull Up	I_{OZLPU}	3020	V_{OUT} =0V, V_{DD}=3.6V, V_{SS}=0V	-	-300	µA
High Impedance Output Leakage Current, High Level	I_{OZH}	3021	V_{OUT} =3.6V V_{DD}=3.6V, V_{SS}=0V	-	5	µA
High Impedance Output Leakage Current, High Level with Pull Down	I_{OZHPD}	3021	V_{OUT} =3.6V V_{DD}=3.6V, V_{SS}=0V	-	300	µA
Low Level Output Voltage 1	V_{OL1}	3007	I_{OL}=4mA V_{DD}=3V, V_{SS}=0V	-	400	mV
Low Level Output Voltage 2	V_{OL2}	3007	I_{OL}=12mA V_{DD}=3V, V_{SS}=0V	-	400	mV
Low Level Output Voltage 3	V_{OL3}	3007	I_{OL}=16mA V_{DD}=3V, V_{SS}=0V	-	400	mV
High Level Output Voltage 1	V_{OH1}	3006	I_{OL}=-4mA V_{DD}=3V, V_{SS}=0V	2.4	-	V
High Level Output Voltage 2	V_{OH2}	3006	I_{OL}=-12mA V_{DD}=3V, V_{SS}=0V	2.4	-	V
High Level Output Voltage 3	V_{OH3}	3006	I_{OL}=-16mA V_{DD}=3V, V_{SS}=0V	2.4	-	V
Stand-by Supply Current	I_{DDSB}	3005	Unprogrammed V_{DD}=3.6V, V_{SS}=0V	-	5	mA
Input Capacitance	C_{IN}	3012	V_{IN}=V_{DD}=V_{SS}=0V Note 2	-	10	pF
Propagation Delay Low to High Look-up Table Inverter (Lut inverter /)	TP1	3003	V_{DD}=3V, V_{SS}=0V	-	3	ns
Propagation Delay High to Low Look-up Table Inverter (Lut inverter \)	TP2	3003	V_{DD}=3V, V_{SS}=0V	-	3	ns
Propagation Delay Low to High Look-up Table Buffer (Lut buffer /)	TP3	3003	V_{DD}=3V, V_{SS}=0V	-	3	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Propagation Delay High to Low Look-up Table Buffer (Lut buffer \)	TP4	3003	V_{DD}=3V, V_{SS}=0V	-	3	ns
Propagation Delay A14 to A0 (CLK to Q)	TP5	3003	V_{DD}=3V, V_{SS}=0V	-	10	ns
Propagation Delay A15 to A0 (Set to Q)	TP6	3003	V_{DD}=3V, V_{SS}=0V	-	11	ns
Propagation Delay A15 to A0 (Reset to Q)	TP7	3003	V_{DD}=3V, V_{SS}=0V	-	13	ns

NOTES:

1. Devices are functionally tested using a serial scan test method. Devices are first 100% functionally tested, then benchmark design/timing patterns are programmed into the devices and then characterised to determine the compliance of the parameters.
2. Parameter guaranteed but not tested.
3. Condition for $V_{IL} \leq 0.3V_{DD}$ for CMOS and $\leq 0.8V$ for TTL.
   Condition for $V_{IH} \geq 0.7V_{DD}$ for CMOS and $\geq 2V$ for TTL.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5) ^{o}C and T_{amb}=- 55(+5-0)^{o}C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 $\pm$3^{o}C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	±0.5	-	-5	µA
High Level Input Current	I_{IH}	±0.5	-	5	µA
High Impedance Output Leakage Current, Low Level	I_{OZL}	±0.5	-	-5	µA
High Impedance Output Leakage Current, High Level	I_{OZH}	±0.5	-	5	µA
Low Level Output Voltage 1	V_{OL1}	±0.1	-	0.4	V
Low Level Output Voltage 2	V_{OL2}	±0.1	-	0.4	V
Low Level Output Voltage 3	V_{OL3}	±0.1	-	0.4	V
High Level Output Voltage 1	V_{OH1}	±0.1	2.4	-	V
High Level Output Voltage 2	V_{OH2}	±0.1	2.4	-	V
High Level Output Voltage 3	V_{OH3}	±0.1	2.4	-	V
Stand-by Supply Current	I_{DDSB}	±0.5	-	5	mA

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	℃
Positive Supply Voltage	V_{DD}	3.7	V
Negative Supply Voltage	V_{SS}	0	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	200	kHz

NOTES:

1. During Burn-in and Operating Life, the devices shall be programmed with a reset and configuration pattern.
2. Test set-up shall be maintained within the manufacturer's PID.
3. Input and I/O Protection Resistor = 1kΩ

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continous bias shall be applied during irradiation testing as specified below. The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ± 3	℃
Positive Supply Voltage	V_{DD}	3.6	V
Negative Supply Voltage	V_{SS}	0	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	1	Hz

NOTES:

1. During Total Dose Radiation Testing the device shall be programmed with a logical pattern.
2. Test set-up shall be maintained within the manufacturer's PID.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall successfully meet the Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at T_{amb} = 22±3 ^{o}C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.