



**INTEGRATED CIRCUITS, SILICON MONOLITHIC,  
QUAD BIPOLAR VOLTAGE COMPARATOR,  
BASED ON TYPES LM139 AND LM139A  
ESCC Detail Specification No. 9103/004**

**ISSUE 1  
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ESA/SCC Detail Specification No. 9103/004**



**space components  
coordination group**

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 2	March 1995	<i>P. Anom...</i>	<i>[Signature]</i>





**DOCUMENTATION CHANGE NOTICE**

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all modifications defined in Revisions 'A', 'B', 'C' and 'D' to Issue 1 and the following DCR's:- Cover Page		None
		DCN		None
		Table 1(a)	: Lead Material column heading amended : For Variants 01 to 06, "(a)" added to Figure	221144 221144
			: Variants 07 to 10 added	221144
		Table 1(b)	: Nos. 1, 3, 4, 6 and 7, Symbol amended : No. 5, Characteristics amended. Ratings and Notes added for Variants 07 to 10	221144 221144
			: No. 6, Note reference amended	221144
			: No. 7, "T <sub>amb</sub> " added to Remarks	221144
			: No. 9, existing temperature referenced to FP and DIP, new temperature added for CCP and Note 3 reference amended to "5"	221144
			: Note 1 amended	221144
			: Notes 2 and 3 renumbered as "4" and "5" and new Notes 2 and 3 added	221144
			: New Note 5, text deleted and new text added	221144
			: New Note 6 added	221144
		Figure 1	: Title amended and Undertitle added : Existing slope allocated to Variants 01 to 06 and new slopes added	221144 221144
		Figure 2(a)	: Title amended and Sub-title added : Imperial dimensions deleted	221144 221144
			: Notes moved and standardised	221144
		Figures 2(b), 2(c)	: Added	221144
		Figure 2	: Notes consolidated onto 1 page	221144
		Figure 3(a)	: Title added to existing drawing : New Title and drawing added	221144 221144
			: Pin assignment added	221144
		Figure 3(d)	: Pin functions added	23724
		Para. 3	: "I <sub>O</sub> ", "I <sub>I</sub> " and "V <sub>S</sub> " abbreviations amended : "V <sub>T</sub> " abbreviation added	221144 221144
		Para. 4.3.2	: Text amended	221144
		Para. 4.4.2	: Text amended	221144
		Para. 4.5.1	: Text deleted and new text added	23724
		Para. 4.5.2	: Text amended	221144
		Para. 4.5.5	: Deleted in toto	23724
		Para. 4.7.2	: Renumbered to "4.7.3" and text amended : New Para. added	221144 221144
		Para. 4.7.3	: Renumbered to "4.7.5" and text amended	221144
		Para. 4.7.4	: New Para. added	221144
		Table 2	: Note 5 amended	221144
		Table 5(a)	: Entry added	221144
		Table 5	: Renumbered to "5(b)" and Title amended	221144
		Figure 5(a)	: Entry added	221144
		Figure 5	: Renumbered to "5(b)" and Title amended	221144
		Para. 4.8.2	: Second sentence added	221144
		Para's. 4.8.4 & 4.8.5	: In second sentence, 5 changed to "5(b)"	221144





**DOCUMENTATION CHANGE NOTICE**

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		Para. 4.8.6 Table 6	: Second sentence amended : Note amended	23724 221144

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**APPENDICES (Applicable to specific Manufacturers only)**

None.

**1. GENERAL****1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, Quad Bipolar Voltage Comparator, based on Types LM139 and LM139A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

**1.2 COMPONENT TYPE VARIANTS**

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

**1.3 MAXIMUM RATINGS**

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

**1.4 PARAMETER DERATING INFORMATION**

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

**1.5 PHYSICAL DIMENSIONS**

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

**1.6 PIN ASSIGNMENT**

As per Figure 3(a).

**1.7 TRUTH TABLE (FIGURE 3(b))**

Not applicable.

**1.8 CIRCUIT SCHEMATIC**

As per Figure 3(c).

**1.9 FUNCTIONAL DIAGRAM**

As per Figure 3(d).





**TABLE 1(a) - TYPE VARIANTS**

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	LM139	D.I.L.	2(a)	D2
02	LM139	D.I.L.	2(a)	D3 or D4
03	LM139A	D.I.L.	2(a)	D2
04	LM139A	D.I.L.	2(a)	D3 or D4
05	LM139	D.I.L.	2(a)	G4
06	LM139A	D.I.L.	2(a)	G4
07	LM139	FLAT	2(b)	G4
08	LM139A	FLAT	2(b)	G4
09	LM139	CHIP CARRIER	2(c)	2
10	LM139A	CHIP CARRIER	2(c)	2

**TABLE 1(b) - MAXIMUM RATINGS**

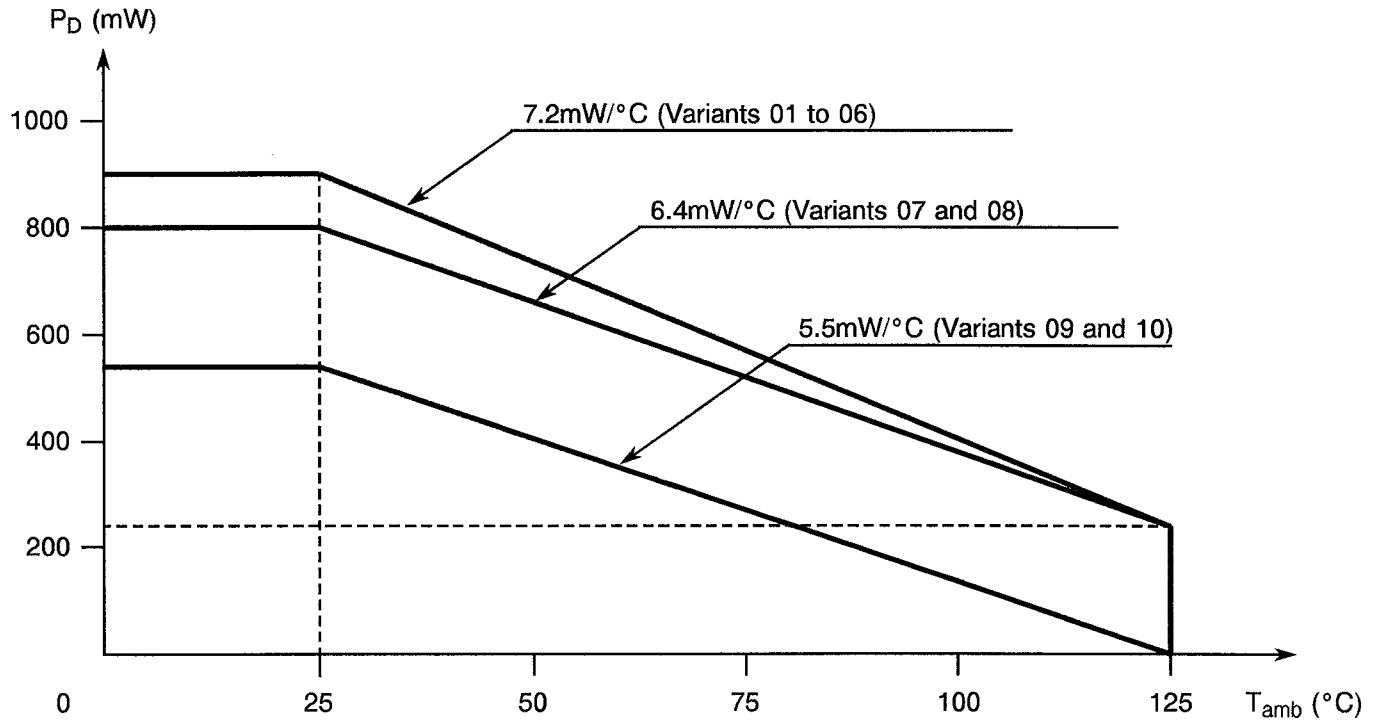
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage Range	$V_{CC}$	32 or $\pm 16$	V	-
2	Differential Input Voltage Range	$V_{ID}$	30	V	-
3	Output Sink Current	$I_{OUT}$	35	mA	-
4	Input Voltage Range	$V_{IN}$	- 0.3 to +30	V	-
5	Power Dissipation Variants 01 to 06 Variants 07 and 08 Variants 09 and 10 Variants 09 and 10	$P_D$	900 800 550 300	mW	Note 1 Note 1 Note 2 Note 3
6	Output Short Circuit Duration	$I_{OS(t)}$	Indefinite	-	Note 4
7	Operating Temperature Range	$T_{op}$	- 55 to +125	$^{\circ}C$	$T_{amb}$
8	Storage Temperature Range	$T_{stg}$	- 55 to +150	$^{\circ}C$	-
9	Soldering Temperature For FP and DIP For CCP	$T_{sol}$	+ 300 + 245	$^{\circ}C$	Note 5 Note 6

**NOTES**

1. At  $T_{amb} = +25^{\circ}C$ . For derating at  $T_{amb} > +25^{\circ}C$ , see Figure 1.
2. At  $T_{amb} = +25^{\circ}C$  when mounted on a ceramic substrate of dimensions  $15 \times 15 \times 0.6mm$ . For derating at  $T_{amb} > +25^{\circ}C$ , see Figure 1.
3. At  $T_{amb} = +25^{\circ}C$  without substrate.
4. No protection exists for short circuits to the positive supply. Short circuits from the output to  $V_{IN+}$  can cause excessive heating and eventual destruction.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
6. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.



**FIGURE 1 - PARAMETER DERATING INFORMATION**

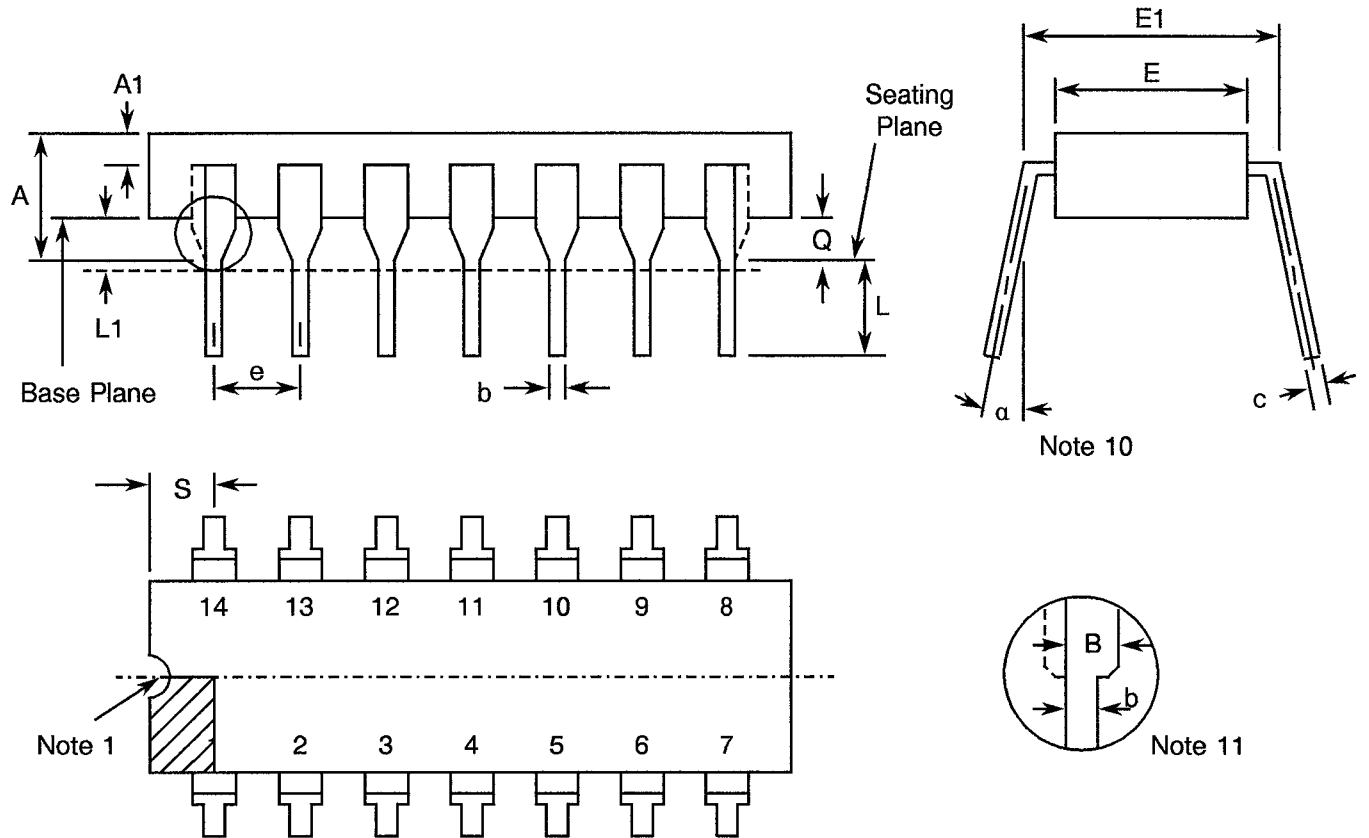


Power Dissipation versus Temperature



**FIGURE 2 - PHYSICAL DIMENSIONS**

**FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 14 PIN**



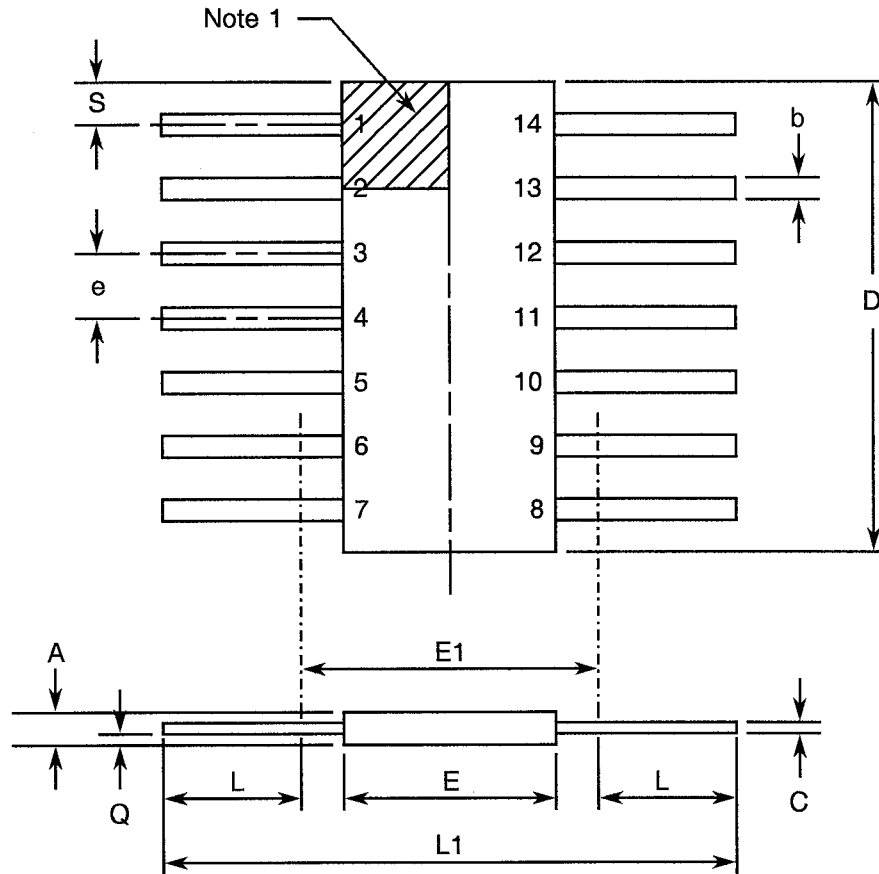
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
A1	-	2.03	
b	0.381	0.508	8
B	-	1.77	
c	0.204	0.304	8
e	2.54 TYPICAL		6, 9
E	6.30 TYPICAL		
E1	7.62	8.25	
L	2.5	3.9	8
L1	-	0.76	12
Q	0.51	-	3
S	Note 13	Note 13	7
a	0°	15°	10

**NOTES:** See Page 12.



**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

**FIGURE 2(b) - FLAT PACKAGE, 14-PIN**



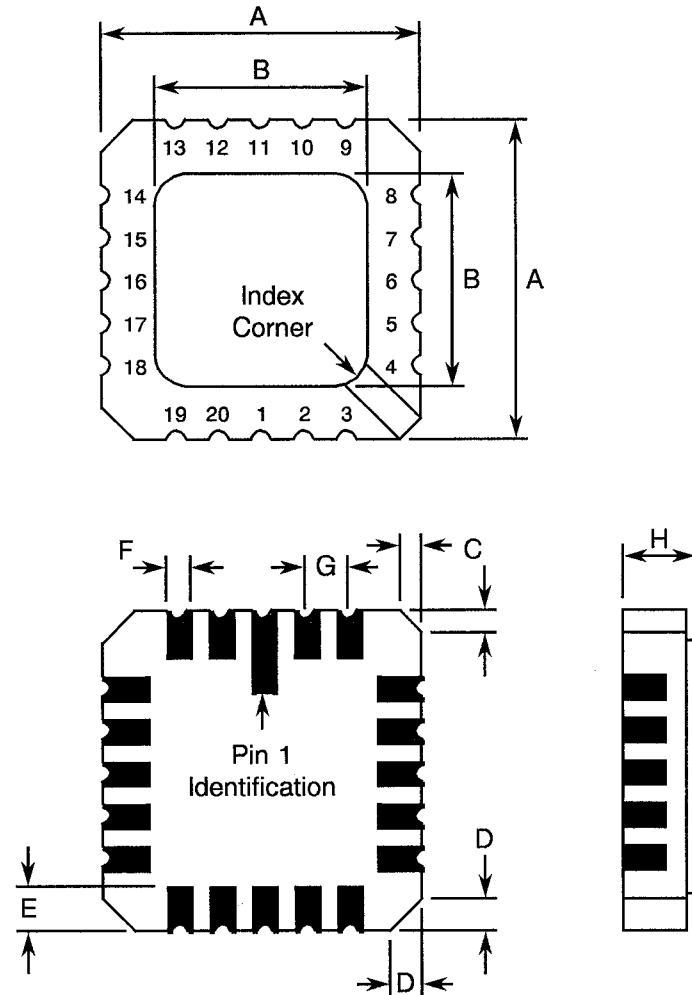
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.53	2.15	
b	0.36	0.48	8
C	0.11	0.17	8
D	9.42	9.90	4
E	6.23	6.60	
E1	7.00 TYPICAL		4
e	1.27 TYPICAL		5, 9
L	6.10	9.14	8
L1	18.93	25.38	
Q	0.51	1.02	2
S	-	1.14	7

**NOTES:** See Page 12.



**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

**FIGURE 2(c) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE), 20-TERMINAL**



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	8.69	9.09	
B	7.80	9.09	
C	0.25	0.51	14
D	0.89	1.14	15
E	1.14	1.40	8
F	0.56	0.71	8
G	1.27 TYPICAL		5, 9
H	1.63	2.54	

**NOTES:** See Page 12.

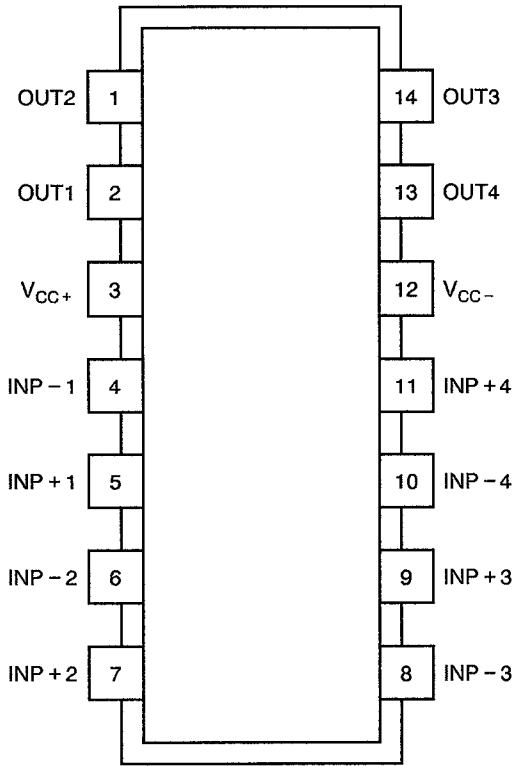
**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)****NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE**

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(c).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within  $\pm 0.13\text{mm}$  of its true longitudinal position relative to Pins 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within  $\pm 0.25\text{mm}$  of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 12 spaces for flat and dual-in-line packages.  
16 spaces for chip carrier packages.
10. Lead centre when  $\alpha$  is  $0^\circ$ .
11. The lead profile is not required for the transition from B to b.  
The outline of the end pins in the case of F.105A may differ from that of the others.
12. The spacing between leads is measured within the area of L1.
13. Case F.105 : S between  $e/2$  and e ( $1.27\text{mm} < Z < 2.54\text{mm}$ ).  
Case F.105A : S less than  $e/2$  ( $S < 1.27\text{mm}$ ).
14. Index corner only - 2 dimensions.
15. 3 non-index corners - 6 dimensions.



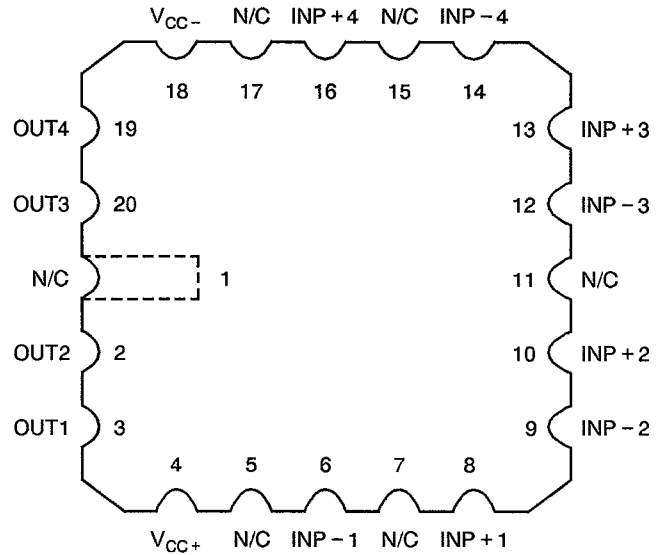
**FIGURE 3(a) - PIN ASSIGNMENT**

DUAL-IN-LINE AND FLAT PACKAGE



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CHIP CARRIER PIN OUTS	2	3	4	6	8	9	10	12	13	14	16	18	19	20

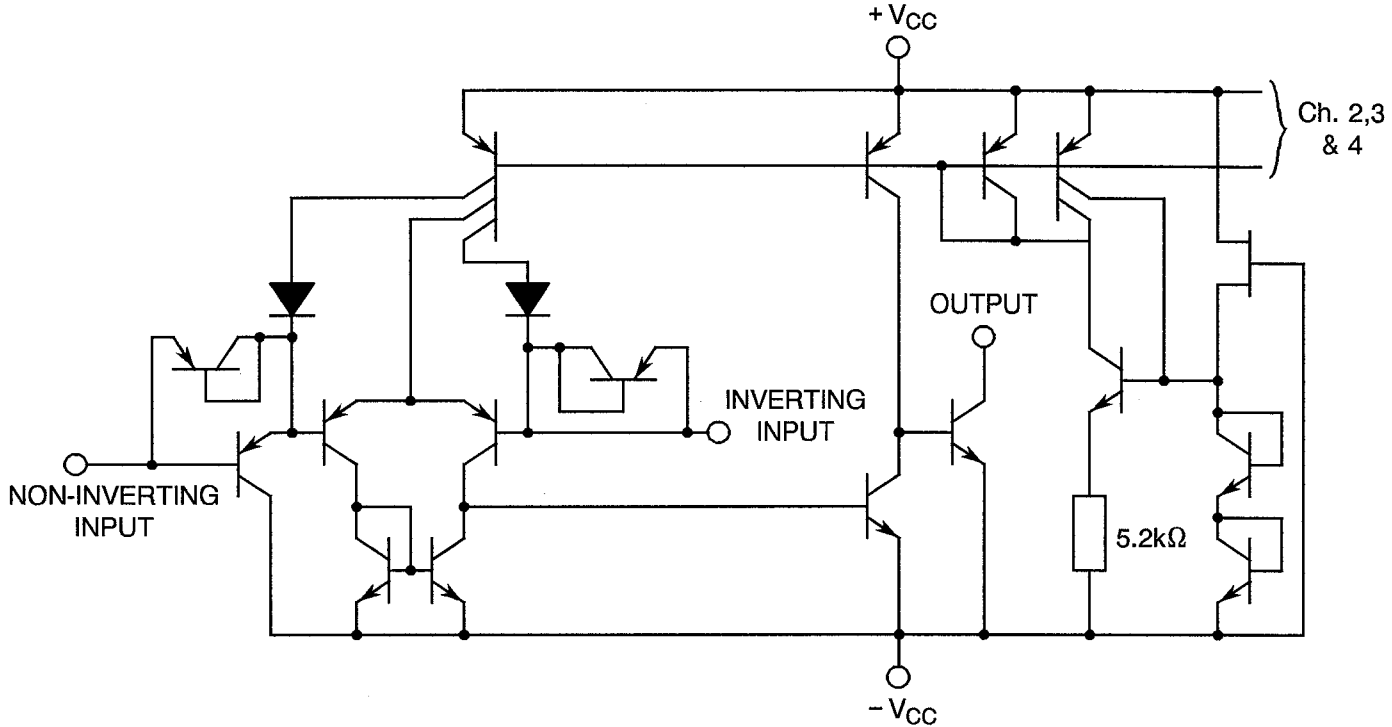
**FIGURE 3(b) - TRUTH TABLE**

Not applicable.

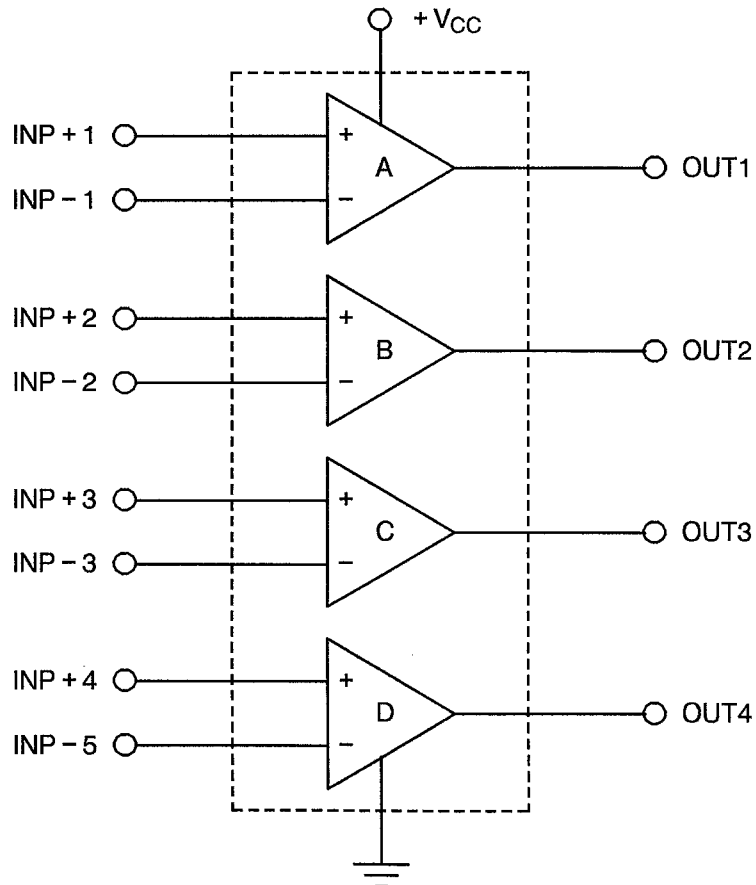




**FIGURE 3(c) - CIRCUIT SCHEMATIC**



**FIGURE 3(d) - FUNCTIONAL DIAGRAM**



**2. APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

**3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

- $V_T$  = Test Voltage.
- $I_{OS(t)}$  = Output Short Circuit Duration.
- $I_{CC}$  = Supply Current.
- $V_{CC}$  = Supply Voltage of the device under test.

**4. REQUIREMENTS****4.1 GENERAL**

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

**4.2 DEVIATIONS FROM GENERIC SPECIFICATION****4.2.1 Deviations from Special In-process Controls**

None.

**4.2.2 Deviations from Final Production Tests (Chart II)**

None.

**4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)**

- (a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

**4.2.4 Deviations from Qualification Tests (Chart IV)**

None.

**4.2.5 Deviations from Lot Acceptance Tests (Chart V)**

None.



#### 4.3 MECHANICAL REQUIREMENTS

##### 4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

##### 4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.0 grammes for the dual-in-line package, 1.0 grammes for the flat package and 0.6 grammes for the chip carrier package.

#### 4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

##### 4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

##### 4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the lead material shall be Type 'D' or Type 'G' with either Type '2', Type '3 or 4' or Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be Type '2' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

#### 4.5 MARKING

##### 4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

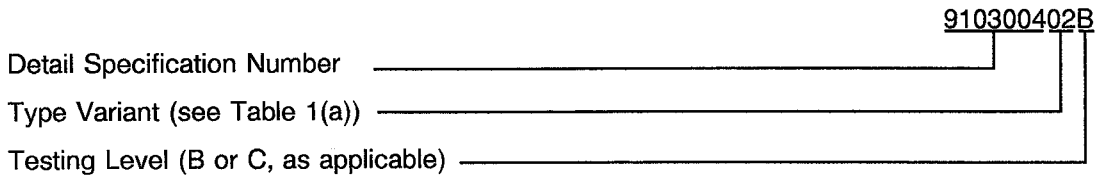
##### 4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined in Figure 2(c).



4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3(a) and 3(b). The measurements shall be performed at  $T_{amb} = +125(+0-5)$  and  $-55(+5-0)$  °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C. The parameter drift values ( $\Delta$ ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in (Table 5(a))

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in (Figure 5(a))

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
1 to 4	Input Offset Voltage 1	$V_{IO1}$	4001	4(a)	$E_1$	+ $V_{CC} = 30V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_L = 30V$ $V_T = 15V$	-	5.0 (2.0)	mV
5 to 8	Input Offset Voltage 2	$V_{IO2}$	4001	4(a)	$E_2$	+ $V_{CC} = 2.0V$ - $V_{CC} = -28V$ $V_{IN+} = 0V$ $V_L = 2.0V$ $V_T = -13V$	-	5.0 (2.0)	mV
9 to 12	Input Offset Voltage 3	$V_{IO3}$	4001	4(a)	$E_3$	+ $V_{CC} = 5.0V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_L = 5.0V$ $V_T = 1.4V$	-	5.0 (2.0)	mV
13 to 16	Input Offset Voltage 4	$V_{IO4}$	4001	4(a)	$E_4$	+ $V_{CC} = 2.0V$ - $V_{CC} = -3.0V$ $V_{IN+} = 0V$ $V_L = 2.0V$ $V_T = -1.6V$	-	5.0 (2.0)	mV
17 to 20	Input Bias Current +1	$I_{B1+}$	4001	4(b)	$E_5+$	+ $V_{CC} = 30V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ )	-	100	nA
21 to 24	Input Bias Current +2	$I_{B2+}$	4001	4(b)	$E_6+$	+ $V_{CC} = 2.0V$ - $V_{CC} = -28V$ $V_{IN+} = 0V$ $V_{IN-} = 100mA$ ( $V_{IN-} = -100mV$ )	-	100	nA
25 to 28	Input Bias Current +3	$I_{B3+}$	4001	4(b)	$E_7+$	+ $V_{CC} = 5.0V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ )	-	100	nA
29 to 32	Input Bias Current +4	$I_{B4+}$	4001	4(b)	$E_8+$	+ $V_{CC} = 2.0V$ - $V_{CC} = -3.0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ )	-	100	nA

**NOTES:** See Page 22.



**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
33 to 36	Input Bias Current - 1	$I_{B1-}$	4001	4(b)	$E_5 -$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
37 to 40	Input Bias Current - 2	$I_{B2-}$	4001	4(b)	$E_6 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
41 to 44	Input Bias Current - 3	$I_{B3-}$	4001	4(b)	$E_7 -$	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
45 to 48	Input Bias Current - 4	$I_{B4-}$	4001	4(b)	$E_8 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
49 to 52	Input Offset Current 1	$I_{IO1}$	4001	4(c)	$E_5 +$  $E_5 -$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 100mV (V <sub>IN-</sub> = -100mV)  +V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	25	nA
53 to 56	Input Offset Current 2	$I_{IO2}$	4001	4(c)	$E_6 +$  $E_6 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN-</sub> = 100mV V <sub>IN+</sub> = 0V (V <sub>IN-</sub> = -100mV)  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	25	nA

**NOTES:** See Page 22.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
57 to 60	Input Offset Current 3	$I_{IO3}$	4001	4(c)	$E_7 +$  $E_7 -$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ ) $+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 100mV$ $V_{IN-} = 0V$ ( $V_{IN+} = -100mV$ )	-	25	nA
61 to 64	Input Offset Current 4	$I_{IO4}$	4001	4(c)	$E_8 +$  $E_8 -$	$+V_{CC} = 2.0V$ $-V_{CC} = -3.0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ ) $+V_{CC} = 2.0V$ $-V_{CC} = -3.0V$ $V_{IN+} = 100mV$ $V_{IN-} = 0V$ ( $V_{IN+} = -100mV$ )	-	25	nA
65 to 68	Output Leakage Current	$I_{OL}$	4001	4(d)	$E_9$	$+V_{CC} = 0V$ $-V_{CC} = -30V$ $V_{IN+} = -29V$ $V_{IN-} = -30V$ $V_O = 0V$	-	1.0	$\mu A$
69 to 72	Input Leakage Current	$+I_{IL}$	-	4(e)	$E_{10}$	$+V_{CC} = 2.0V$ $-V_{CC} = -34V$ $V_{IN+} = 0V$ $V_{IN-} = -34V$	-	1.0	$\mu A$
73 to 76	Input Leakage Current	$-I_{IL}$	-	4(e)	$E_{11}$	$+V_{CC} = 2.0V$ $-V_{CC} = -34V$ $V_{IN+} = -34V$ $V_{IN-} = 0V$	-	1.0	$\mu A$
77	Supply Current 1	$I_{CC1}$	-	4(f)	$E_{12}$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN-} = 0V$ $V_D = -1.5V$	-	2.0	mA
78	Supply Current 2	$I_{CC2}$	-	4(f)	$E_{13}$	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN-} = 0V$ $V_D = -1.5V$	-	3.0	mA

**NOTES:** See Page 22.



**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
79 to 82	Saturation Voltage 1	$V_{OL1}$	-	4(g)	E <sub>14</sub>	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 1.0V I(V <sub>O</sub> ) = 4.0mA	-	400	mV
83 to 86	Saturation Voltage 2	$V_{OL2}$	-	4(g)	E <sub>15</sub>	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 1.0V I(V <sub>O</sub> ) = 8.0mA	-	1.5	V
87 to 90	Voltage Gain	$A_{VS}$	4004	4(h)	E <sub>16</sub>  E <sub>17</sub>	+V <sub>CC</sub> = 15V -V <sub>CC</sub> = 0V V <sub>L</sub> = 15V V <sub>T</sub> = 1.0V  +V <sub>CC</sub> = 15V -V <sub>CC</sub> = 0V V <sub>L</sub> = 15V V <sub>T</sub> = 11V	50	-	V/mV
91 to 94	Common Mode Rejection Ratio 1	$C_{MR1}$	4003	4(i)	E <sub>3</sub>  E <sub>4</sub>	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 5.0V V <sub>T</sub> = 1.4V  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -1.6V	70	-	dB
95 to 98	Common Mode Rejection Ratio 2	$C_{MR2}$	4003	4(i)	E <sub>1</sub>  E <sub>2</sub>	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 30V V <sub>T</sub> = 15V Note 3  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -13V Note 3	76	-	dB

**NOTES:** See Page 22.



**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS		UNIT
							MIN	MAX	
99 to 102	Response Time (Low to High) 1	$t_{rLH1}$	-	4(j)	E <sub>18</sub>	+V <sub>CC</sub> = 5.0V V <sub>IN</sub> = 100mV R <sub>L</sub> = 5.1k $\Omega$ V <sub>OD</sub> = 5.0mV Note 4	-	5.0	$\mu$ s
103 to 106	Response Time (Low to High) 2	$t_{rLH2}$	-	4(j)	E <sub>19</sub>	+V <sub>CC</sub> = 5.0V V <sub>IN</sub> = 100mV R <sub>L</sub> = 5.1k $\Omega$ V <sub>OD</sub> = 50mV Note 4	-	0.8	$\mu$ s
107 to 110	Response Time (High to Low) 1	$t_{rHL1}$	-	4(j)	E <sub>20</sub>	+V <sub>CC</sub> = 5.0V V <sub>IN</sub> = 100mV R <sub>L</sub> = 5.1k $\Omega$ V <sub>OD</sub> = 5.0mV Note 4	-	2.5	$\mu$ s
111 to 114	Response Time (High to Low) 2	$t_{rHL2}$	-	4(j)	E <sub>21</sub>	+V <sub>CC</sub> = 5.0V V <sub>IN</sub> = 100mV R <sub>L</sub> = 5.1k $\Omega$ V <sub>OD</sub> = 50mV Note 4	-	0.8	$\mu$ s

**NOTES**

- Adjust the signal generator so that V<sub>IN</sub> is a 100mV pulse train with a 10 $\mu$ s pulse width at 50kHz, t<sub>r</sub> and t<sub>f</sub> < 10ns and Z<sub>O</sub> = 50 $\Omega$ .
- All resistor tolerances are  $\pm$ 1% and all capacitor tolerances are  $\pm$ 10%.
- C<sub>MR1</sub> and C<sub>MR2</sub> shall be calculated using data from input offset voltage measurements.
- Measurements performed on a sample basis LTPD7 or less.
- Limits without parenthesis are for all Variants. However, if parenthesised Limits are contained in a Limits Box, the Limits without parenthesis are for Variants 01, 02, 05, 07 and 09 and the Limits with parenthesis are for Variants 03, 04, 06, 08 and 10.

**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
1 to 4	Input Offset Voltage 1	$V_{IO1}$	4001	4(a)	$E_1$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 30V V <sub>T</sub> = 15V	-	7.0 (4.0)	mV
5 to 8	Input Offset Voltage 2	$V_{IO2}$	4001	4(a)	$E_2$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -13V	-	7.0 (4.0)	mV
9 to 12	Input Offset Voltage 3	$V_{IO3}$	4001	4(a)	$E_3$	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 5.0V V <sub>T</sub> = 1.4V	-	7.0 (4.0)	mV
13 to 16	Input Offset Voltage 4	$V_{IO4}$	4001	4(a)	$E_4$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -1.6V	-	7.0 (4.0)	mV
17 to 20	Input Bias Current +1	$I_{B1+}$	4001	4(b)	$E_5+$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 100mV (V <sub>IN-</sub> = -100mV)	-	100	nA
21 to 24	Input Bias Current +2	$I_{B2+}$	4001	4(b)	$E_6+$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 100mA (V <sub>IN-</sub> = -100mV)	-	100	nA
25 to 28	Input Bias Current +3	$I_{B3+}$	4001	4(b)	$E_7+$	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 100mV (V <sub>IN-</sub> = -100mV)	-	100	nA
29 to 32	Input Bias Current +4	$I_{B4+}$	4001	4(b)	$E_8+$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 100mV (V <sub>IN-</sub> = -100mV)	-	100	nA

**NOTES:** See Page 22.



**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
33 to 36	Input Bias Current - 1	$I_{B1-}$	4001	4(b)	$E_5 -$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
37 to 40	Input Bias Current - 2	$I_{B2-}$	4001	4(b)	$E_6 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
41 to 44	Input Bias Current - 3	$I_{B3-}$	4001	4(b)	$E_7 -$	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
45 to 48	Input Bias Current - 4	$I_{B4-}$	4001	4(b)	$E_8 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	100	nA
49 to 52	Input Offset Current 1	$I_{IO1}$	4001	4(c)	$E_5 +$  $E_5 -$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 100mV (V <sub>IN-</sub> = -100mV)  +V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	25	nA
53 to 56	Input Offset Current 2	$I_{IO2}$	4001	4(c)	$E_6 +$  $E_6 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN-</sub> = 100mV V <sub>IN+</sub> = 0V (V <sub>IN-</sub> = -100mV)  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	25	nA

**NOTES:** See Page 22.



**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
57 to 60	Input Offset Current 3	$I_{IO3}$	4001	4(c)	$E_7 +$  $E_7 -$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ ) $+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 100mV$ $V_{IN-} = 0V$ ( $V_{IN+} = -100mV$ )	-	25	nA
61 to 64	Input Offset Current 4	$I_{IO4}$	4001	4(c)	$E_8 +$  $E_8 -$	$+V_{CC} = 2.0V$ $-V_{CC} = -3.0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ ) $+V_{CC} = 2.0V$ $-V_{CC} = -3.0V$ $V_{IN+} = 100mV$ $V_{IN-} = 0V$ ( $V_{IN+} = -100mV$ )	-	25	nA
65 to 68	Output Leakage Current	$I_{OL}$	4001	4(d)	$E_9$	$+V_{CC} = 0V$ $-V_{CC} = -30V$ $V_{IN+} = -29V$ $V_{IN-} = -30V$ $V_O = 0V$	-	1.0	$\mu A$
69 to 72	Input Leakage Current	$+I_{IL}$	-	4(e)	$E_{10}$	$+V_{CC} = 2.0V$ $-V_{CC} = -34V$ $V_{IN+} = 0V$ $V_{IN-} = -34V$	-	1.0	$\mu A$
73 to 76	Input Leakage Current	$-I_{IL}$	-	4(e)	$E_{11}$	$+V_{CC} = 2.0V$ $-V_{CC} = -34V$ $V_{IN+} = -34V$ $V_{IN-} = 0V$	-	1.0	$\mu A$
77	Supply Current 1	$I_{CC1}$	-	4(f)	$E_{12}$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN-} = 0V$ $V_D = -1.5V$	-	2.0	mA
78	Supply Current 2	$I_{CC2}$	-	4(f)	$E_{13}$	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN-} = 0V$ $V_D = -1.5V$	-	3.0	mA

**NOTES:** See Page 22.



**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
79 to 82	Saturation Voltage 1	$V_{OL1}$	-	4(g)	E <sub>14</sub>	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 1.0V I(V <sub>O</sub> ) = 4.0mA	-	700	mV
83 to 86	Saturation Voltage 2	$V_{OL2}$	-	4(g)	E <sub>15</sub>	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 1.0V I(V <sub>O</sub> ) = 8.0mA	-	2.0	V
87 to 90	Voltage Gain	$A_{VS}$	4004	4(h)	E <sub>16</sub>  E <sub>17</sub>	+V <sub>CC</sub> = 15V -V <sub>CC</sub> = 0V V <sub>L</sub> = 15V V <sub>T</sub> = 1.0V  +V <sub>CC</sub> = 15V -V <sub>CC</sub> = 0V V <sub>L</sub> = 15V V <sub>T</sub> = 11V	15	-	V/mV
91 to 94	Common Mode Rejection Ratio 1	$C_{MR1}$	4003	4(i)	E <sub>3</sub>  E <sub>4</sub>	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 5.0V V <sub>T</sub> = 1.4V  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -1.6V	70	-	dB
95 to 98	Common Mode Rejection Ratio 2	$C_{MR2}$	4003	4(i)	E <sub>1</sub>  E <sub>2</sub>	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 30V V <sub>T</sub> = 15V Note 3  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -13V Note 3	76	-	dB

**NOTES:** See Page 22.



**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
1 to 4	Input Offset Voltage 1	$V_{IO1}$	4001	4(a)	$E_1$	+ $V_{CC} = 30V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_L = 30V$ $V_T = 15V$	-	7.0 (4.0)	mV
5 to 8	Input Offset Voltage 2	$V_{IO2}$	4001	4(a)	$E_2$	+ $V_{CC} = 2.0V$ - $V_{CC} = -28V$ $V_{IN+} = 0V$ $V_L = 2.0V$ $V_T = -13V$	-	7.0 (4.0)	mV
9 to 12	Input Offset Voltage 3	$V_{IO3}$	4001	4(a)	$E_3$	+ $V_{CC} = 5.0V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_L = 5.0V$ $V_T = 1.4V$	-	7.0 (4.0)	mV
13 to 16	Input Offset Voltage 4	$V_{IO4}$	4001	4(a)	$E_4$	+ $V_{CC} = 2.0V$ - $V_{CC} = -3.0V$ $V_{IN+} = 0V$ $V_L = 2.0V$ $V_T = -1.6V$	-	7.0 (4.0)	mV
17 to 20	Input Bias Current +1	$I_{B1+}$	4001	4(b)	$E_5+$	+ $V_{CC} = 30V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ )	-	200	nA
21 to 24	Input Bias Current +2	$I_{B2+}$	4001	4(b)	$E_6+$	+ $V_{CC} = 2.0V$ - $V_{CC} = -28V$ $V_{IN+} = 0V$ $V_{IN-} = 100mA$ ( $V_{IN-} = -100mV$ )	-	200	nA
25 to 28	Input Bias Current +3	$I_{B3+}$	4001	4(b)	$E_7+$	+ $V_{CC} = 5.0V$ - $V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ )	-	200	nA
29 to 32	Input Bias Current +4	$I_{B4+}$	4001	4(b)	$E_8+$	+ $V_{CC} = 2.0V$ - $V_{CC} = -3.0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ )	-	200	nA

**NOTES:** See Page 22.



**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
33 to 36	Input Bias Current - 1	$I_{B1-}$	4001	4(b)	$E_5 -$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	200	nA
37 to 40	Input Bias Current - 2	$I_{B2-}$	4001	4(b)	$E_6 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	200	nA
41 to 44	Input Bias Current - 3	$I_{B3-}$	4001	4(b)	$E_7 -$	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	200	nA
45 to 48	Input Bias Current - 4	$I_{B4-}$	4001	4(b)	$E_8 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	200	nA
49 to 52	Input Offset Current 1	$I_{IO1}$	4001	4(c)	$E_5 +$  $E_5 -$	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>IN-</sub> = 100mV (V <sub>IN-</sub> = -100mV)  +V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	75	nA
53 to 56	Input Offset Current 2	$I_{IO2}$	4001	4(c)	$E_6 +$  $E_6 -$	+V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN-</sub> = 100mV V <sub>IN+</sub> = 0V (V <sub>IN-</sub> = -100mV)  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 100mV V <sub>IN-</sub> = 0V (V <sub>IN+</sub> = -100mV)	-	75	nA

**NOTES:** See Page 22.



**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE (CONT'D)**

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
57 to 60	Input Offset Current 3	$I_{IO3}$	4001	4(c)	$E_7+$  $E_7-$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ ) $+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 100mV$ $V_{IN-} = 0V$ ( $V_{IN+} = -100mV$ )	-	75	nA
61 to 64	Input Offset Current 4	$I_{IO4}$	4001	4(c)	$E_8+$  $E_8-$	$+V_{CC} = 2.0V$ $-V_{CC} = -3.0V$ $V_{IN+} = 0V$ $V_{IN-} = 100mV$ ( $V_{IN-} = -100mV$ ) $+V_{CC} = 2.0V$ $-V_{CC} = -3.0V$ $V_{IN+} = 100mV$ $V_{IN-} = 0V$ ( $V_{IN+} = -100mV$ )	-	75	nA
65 to 68	Output Leakage Current	$I_{OL}$	4001	4(d)	$E_9$	$+V_{CC} = 0V$ $-V_{CC} = -30V$ $V_{IN+} = -29V$ $V_{IN-} = -30V$ $V_O = 0V$	-	1.0	$\mu A$
77	Supply Current 1	$I_{CC1}$	-	4(f)	$E_{12}$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN-} = 0V$ $V_D = -1.5V$	-	3.0	mA
78	Supply Current 2	$I_{CC2}$	-	4(f)	$E_{13}$	$+V_{CC} = 30V$ $-V_{CC} = 0V$ $V_{IN-} = 0V$ $V_D = -1.5V$	-	4.0	mA
79 to 82	Saturation Voltage 1	$V_{OL1}$	-	4(g)	$E_{14}$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 1.0V$ $I(V_O) = 4.0mA$	-	100	mV
83 to 86	Saturation Voltage 2	$V_{OL2}$	-	4(g)	$E_{15}$	$+V_{CC} = 5.0V$ $-V_{CC} = 0V$ $V_{IN+} = 0V$ $V_{IN-} = 1.0V$ $I(V_O) = 8.0mA$	-	2.0	V

**NOTES:** See Page 22.





**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE (CONT'D)**

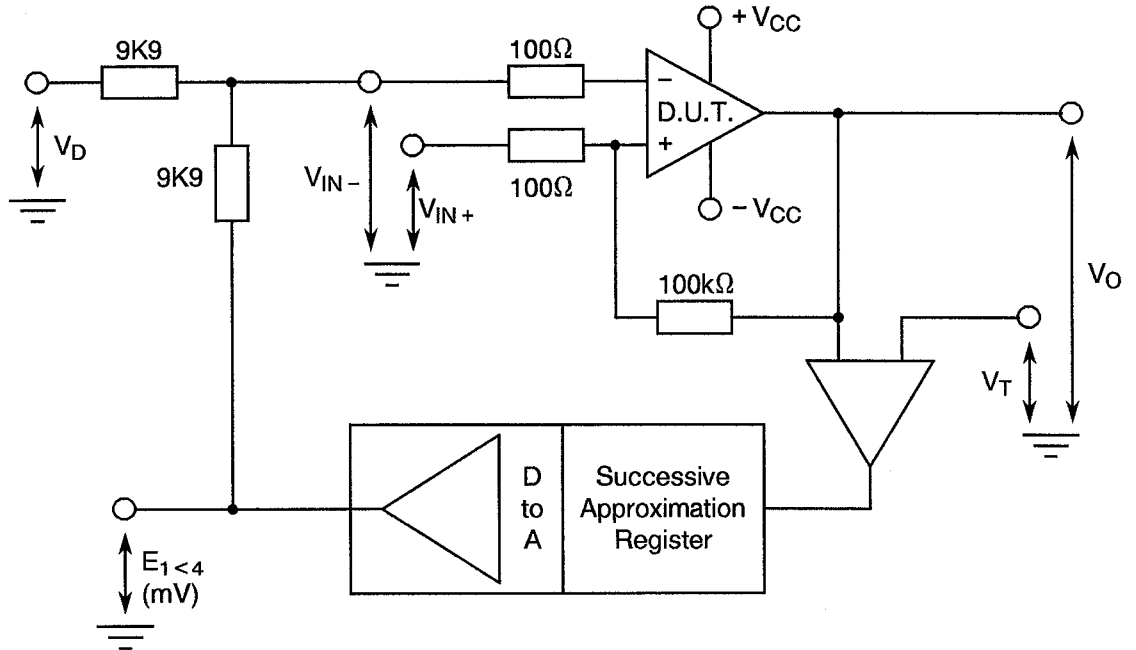
No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	MEAS. VALUE	TEST CONDITIONS (NOTES 1 AND 2)	LIMITS (NOTE 5)		UNIT
							MIN	MAX	
87 to 90	Voltage Gain	$A_{VS}$	4004	4(h)	E <sub>16</sub>  E <sub>17</sub>	+V <sub>CC</sub> = 15V -V <sub>CC</sub> = 0V V <sub>L</sub> = 15V V <sub>T</sub> = 1.0V  +V <sub>CC</sub> = 15V -V <sub>CC</sub> = 0V V <sub>L</sub> = 15V V <sub>T</sub> = 11V	15	-	V/mV
91 to 94	Common Mode Rejection Ratio 1	C <sub>MR1</sub>	4003	4(i)	E <sub>3</sub>  E <sub>4</sub>	+V <sub>CC</sub> = 5.0V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 5.0V V <sub>T</sub> = 1.4V  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -3.0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -1.6V	70	-	dB
95 to 98	Common Mode Rejection Ratio 2	C <sub>MR2</sub>	4003	4(i)	E <sub>1</sub>  E <sub>2</sub>	+V <sub>CC</sub> = 30V -V <sub>CC</sub> = 0V V <sub>IN+</sub> = 0V V <sub>L</sub> = 30V V <sub>T</sub> = 15V Note 3  +V <sub>CC</sub> = 2.0V -V <sub>CC</sub> = -28V V <sub>IN+</sub> = 0V V <sub>L</sub> = 2.0V V <sub>T</sub> = -13V Note 3	76	-	dB

**NOTES:** See Page 22.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS**

**FIGURE 4(a) - INPUT OFFSET VOLTAGE**



**NOTES**

1. This test circuit must be multiplied by 4.

2. Equation:-

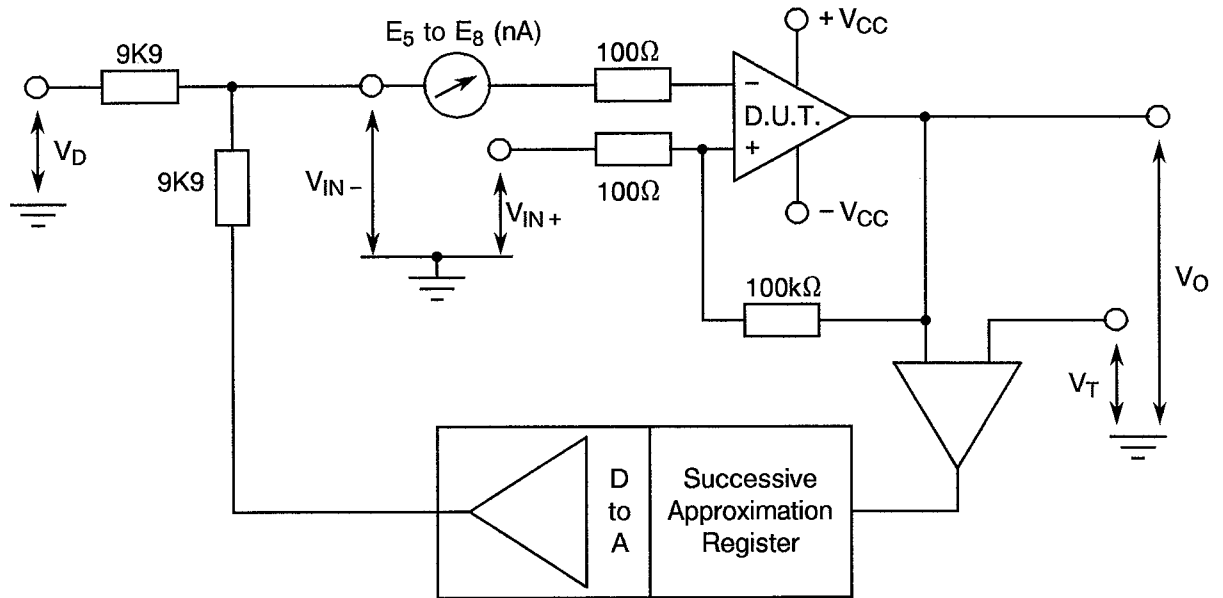
$$V_{IO_n} = \frac{E_n}{100} \text{ (mV)}$$

3. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - INPUT BIAS CURRENT



**NOTES**

1. This test circuit must be multiplied by 4.

2. Equation:-

$$I_{Bn \pm} = I_{\alpha n} + I_{\beta n}. \text{ See Note 4}$$

$$\text{where } I_{\alpha n} + E_{n(+)} = \frac{(100 + V_{IO n})}{200}, \text{ see Note 3}$$

$$\text{and where } I_{\beta n} + E_{n(-)} = \frac{(100 + V_{IO n})}{200}$$

$$E_{n \pm} = I_{Bn} = \frac{I_{Bn+} + I_{Bn-}}{2} \text{ (nA)}$$

3.  $V_{IO n}$  is one of measured values  $E_1$  to  $E_4$ .

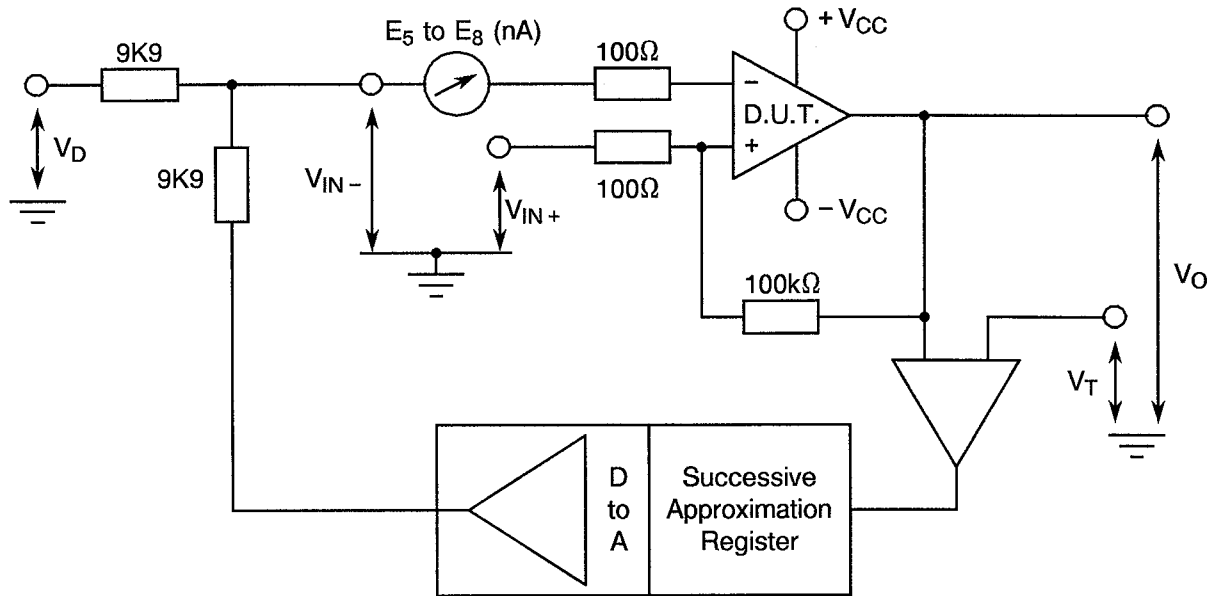
4. Perform this calculation for  $I_{Bn+}$  and  $I_{Bn-}$ . The circuit shown is for  $I_{Bn-}$  measurement. To re-configure for  $I_{Bn+}$  measurement transfer the ammeter to the  $V_{IN+}$  terminal.

5. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(c) - INPUT OFFSET CURRENT**



**NOTES**

1. This test circuit must be multiplied by 4.
2. Equation:-

$$E_n = I_{On} = I_{Bn+} - I_{Bn-}$$

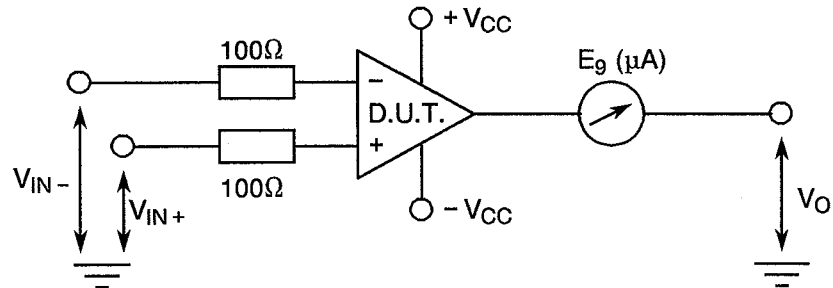
where  $I_{Bn\pm}$  is one of calculated values  $E_5$  to  $E_8$ .

3. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

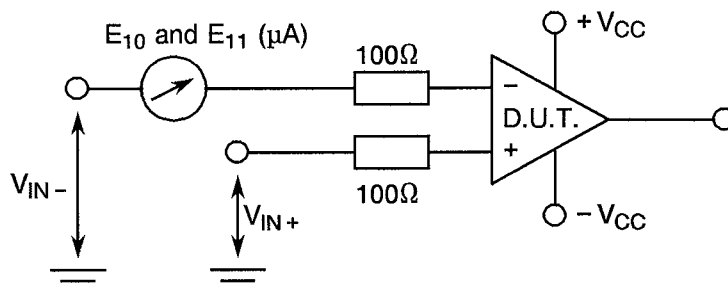
**FIGURE 4(d) - OUTPUT LEAKAGE CURRENT**



**NOTES**

1. This test circuit must be multiplied by 4.
2. Comparators not under test shall have their inputs connected to ground via 10kΩ resistors.

**FIGURE 4(e) - INPUT LEAKAGE CURRENT**



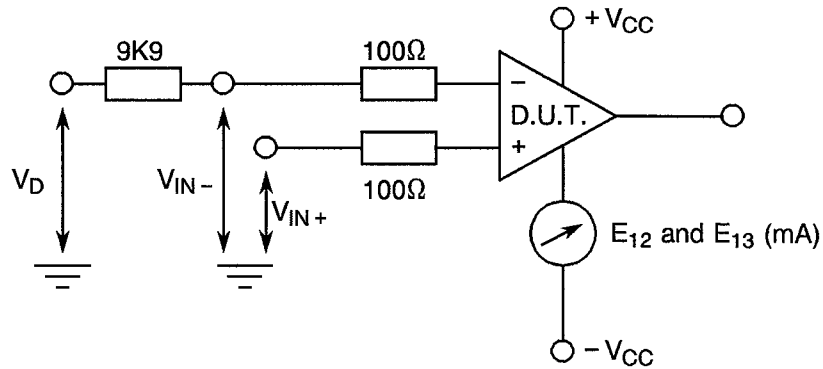
**NOTES**

1. This test circuit must be multiplied by 4.
2. The circuit shown is for  $-I_{IL}$  measurement. To re-configure for  $+I_{IL}$  measurement transfer the ammeter to the  $V_{IN+}$  terminal.
3. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

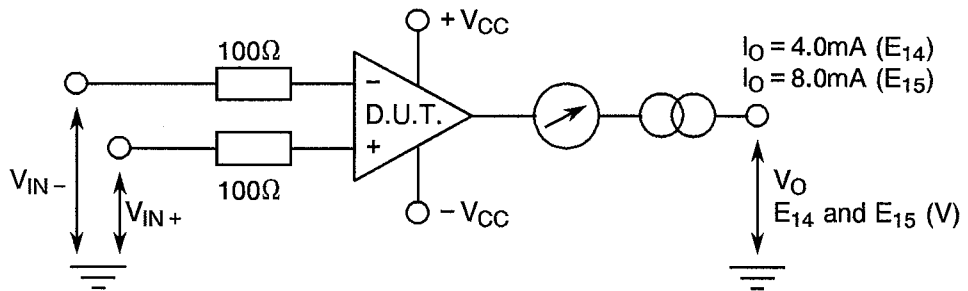
**FIGURE 4(f) - SUPPLY CURRENT**



**NOTES**

1. This test circuit must be multiplied by 4.
2.  $E_{12}$  and  $E_{13}$  to be recorded for appropriate values of  $V_{IN+}$ .
3. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.

**FIGURE 4(g) - SATURATION VOLTAGE**



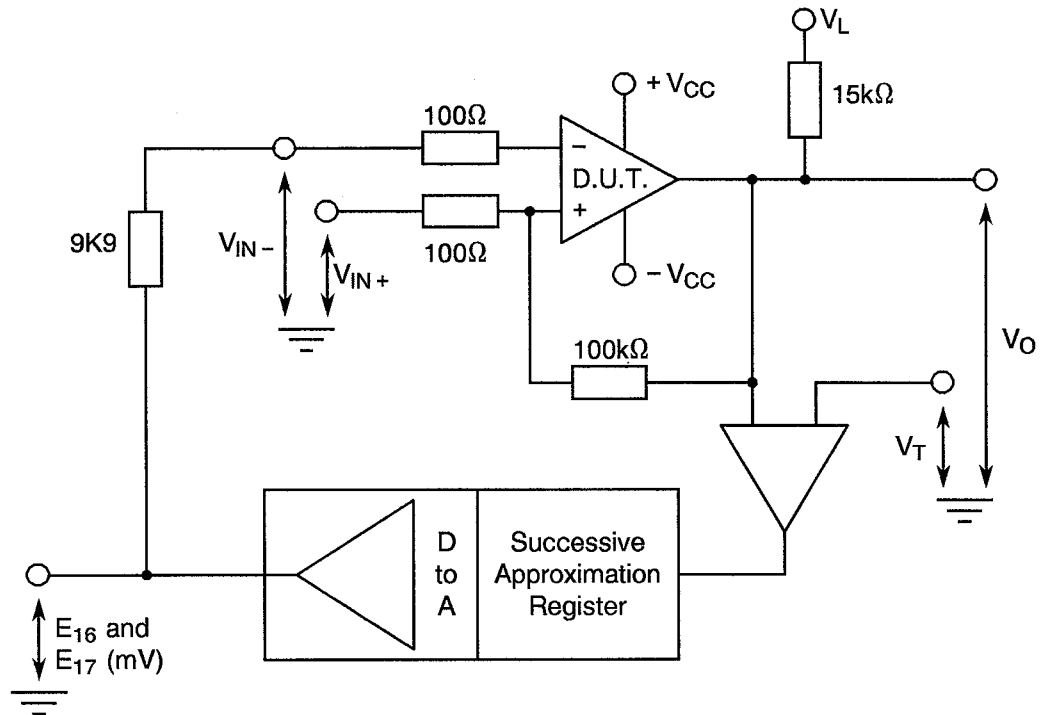
**NOTES**

1. This test circuit must be multiplied by 4.
2.  $E_{14}$  and  $E_{15}$  to be recorded for appropriate values of  $I_O$ .
3. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

FIGURE 4(h) - VOLTAGE GAIN



**NOTES**

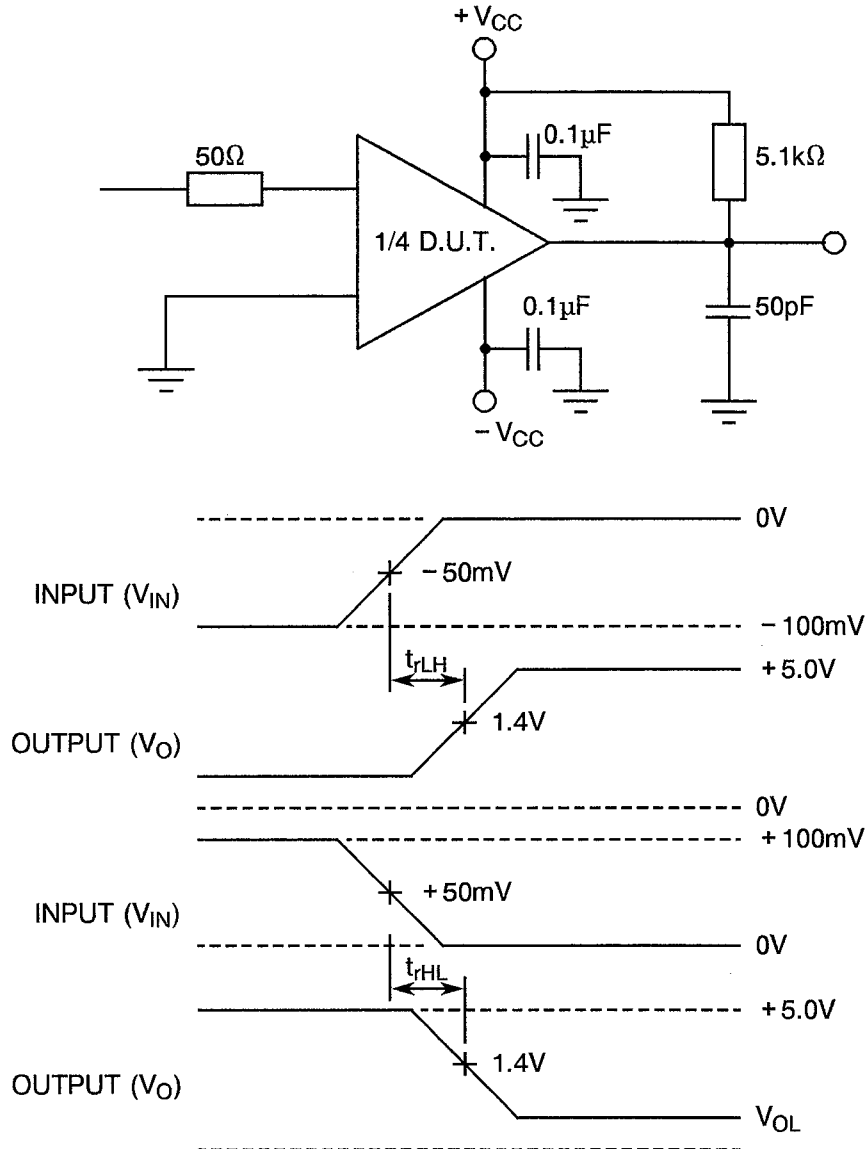
1. This test circuit must be multiplied by 4.
2. E<sub>16</sub> and E<sub>17</sub> to be recorded for appropriate values of V<sub>T</sub>.
3. Equation:-

$$A_{VS} = \frac{1000}{E_{17} - E_{16}} \text{ (V/mV)}$$

4. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.





**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)****FIGURE 4(j) - TEST CIRCUIT AND WAVEFORMS FOR RESPONSE TIME MEASUREMENT****NOTES**

1. Adjust the signal generator so that  $V_{IN}$  is a 100mV pulse train with a 10μs pulse width at 50kHz,  $t_r$  and  $t_f \leq 10\text{ns}$  and  $Z_O = 50\Omega$ .
2. Set-up Procedure:
  - (a) With  $V_{IN} = 0$ , adjust  $V_{REF}$  from -5.0mV to +5.0mV in 0.1mV steps and stop when output switches from high to low.
  - (b) Change  $V_{REF}$  from the value obtained in (a) above by the required  $V_{OD}$  (overdrive).
  - (c) Apply  $V_{IN}$  and measure the response time.
3. All resistor tolerances are  $\pm 1\%$  and all capacitor tolerances are  $\pm 10\%$ .
4. The output capacitance includes scope, probe and jig capacitance.
5. Record  $t_{rLH}$  as E<sub>18</sub> and E<sub>19</sub> with corresponding values of  $V_{OD}$ .  
Record  $t_{rHL}$  as E<sub>20</sub> and E<sub>21</sub> with corresponding values of  $V_{OD}$ .
6. Comparators not under test shall have their inputs connected to ground via 1.0kΩ resistors.

**TABLE 4 - PARAMETER DRIFT VALUES**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS ( $\Delta$ )	UNIT
9 to 12	Input Offset Voltage 3 Change	$V_{IO3}$	As per Table 2	As per Table 2	$\pm 1.0$	mV
25 to 28	Input Bias Current +3 Change	$I_{B3+}$	As per Table 2	As per Table 2	$\pm 10$	nA
41 to 44	Input Bias Current -3 Change	$I_{B3-}$	As per Table 2	As per Table 2	$\pm 10$	nA
57 to 60	Input Offset Current 3 Change	$I_{IO3}$	As per Table 2	As per Table 2	$\pm 25$	nA

**TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN**

Not applicable.

**TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS**

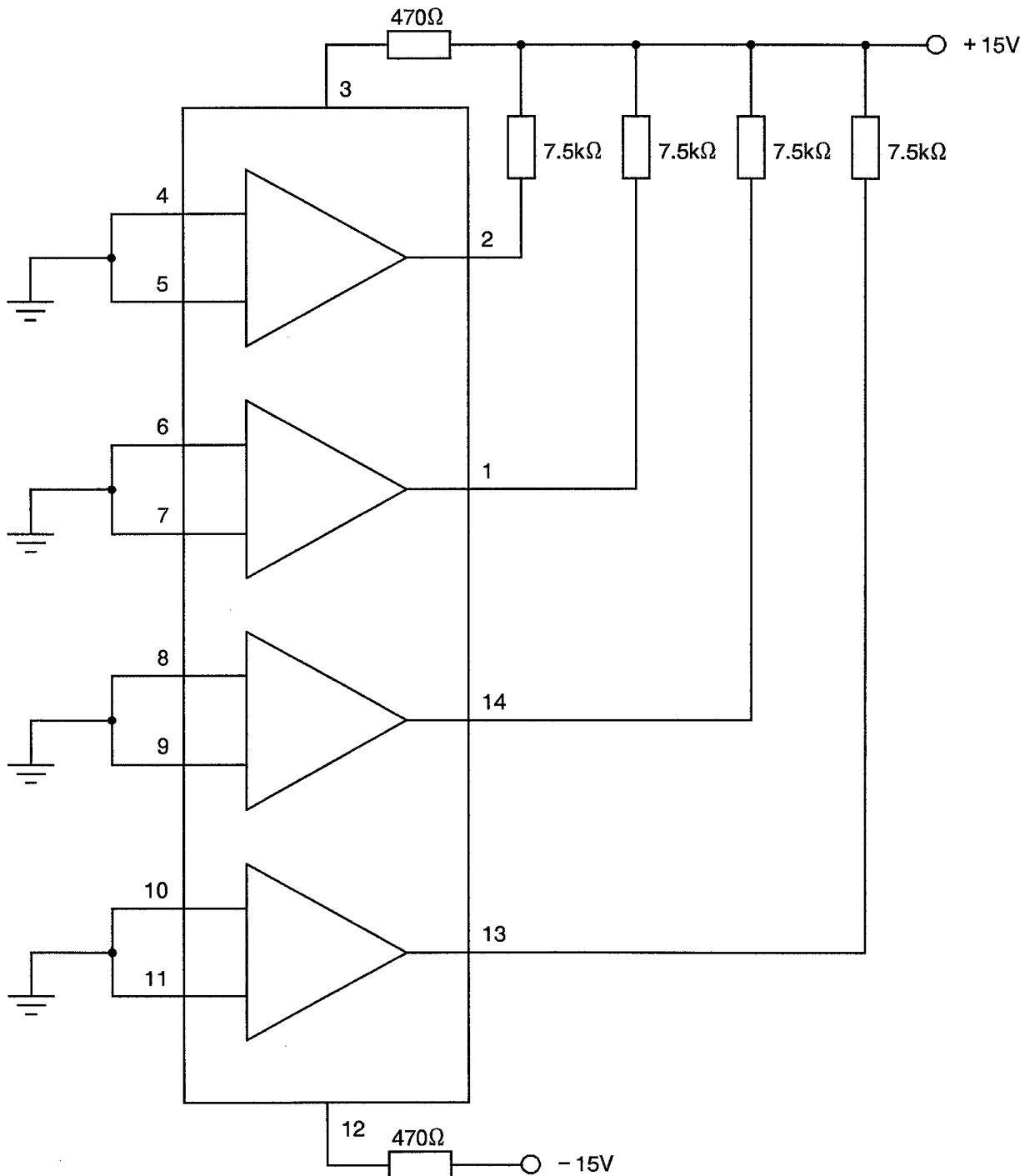
No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	$T_{amb}$	$+125 \pm 5$	$^{\circ}\text{C}$
2	Supply Voltage	$V_{CC}$	$\pm 15$	V



**FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN**

Not applicable.

**FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS**





- 4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)
- 4.8.1 Electrical Measurements on Completion of Environmental Tests  
The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.
- 4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests  
The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.
- 4.8.3 Electrical Measurements on Completion of Endurance Tests  
The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.
- 4.8.4 Conditions for Operating Life Tests (Part of Endurance Testing)  
The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.
- 4.8.5 Electrical Circuits for Operating Life Tests  
Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.
- 4.8.6 Conditions for High Temperature Storage Test (Part of Endurance Testing)  
The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING**

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS (NOTE 1)		UNIT
					MIN.	MAX.	
1 to 4	Input Offset Voltage 1	$V_{IO1}$	As per Table 2	As per Table 2	-	5.0 (2.0)	mV
17 to 20	Input Bias Current + 1	$I_{B1+}$	As per Table 2	As per Table 2	-	100	nA
33 to 36	Input Bias Current - 1	$I_{B1-}$	As per Table 2	As per Table 2	-	100	nA
49 to 52	Input Offset Current 1	$I_{IO1}$	As per Table 2	As per Table 2	-	25	nA
77	Supply Current 1	$I_{CC1}$	As per Table 2	As per Table 2	-	2.0	mA
78	Supply Current 2	$I_{CC2}$	As per Table 2	As per Table 2	-	3.0	mA
87 to 90	Voltage Gain	$A_{VS}$	As per Table 2	As per Table 2	50	-	V/mV

**NOTES**

- Limits without parenthesis are for all Variants. However, if parenthesised Limits are contained in a Limits Box, the Limits without parenthesis are for Variants 01, 02, 05, 07 and 09 and the Limits with parenthesis are for Variants 03, 04, 06, 08 and 10.