# INTEGRATED CIRCUITS, SILICON MONOLITHIC,

# REGULATING PULSE-WIDTH MODULATOR,

# BASED ON TYPE SG1524

# ESCC Detail Specification No. 9108/007

**ISSUE 1**

**October 2002**

Document Custodian: European Space Agency - see https://escies.org

**LEGAL DISCLAIMER AND COPYRIGHT**

european space agency
agence spatiale européenne

Pages 1 to 28

# INTEGRATED CIRCUITS, SILICON MONOLITHIC,

# REGULATING PULSE-WIDTH MODULATOR,

# BASED ON TYPE SG1524

# ESA/SCC Detail Specification No. 9108/007

space components
coordination group

| Issue/Rev. | Date | Approved by | |
|---|---|---|---|
| | | SCCG Chairman | ESA Director General or his Deputy |
| Issue 1 | July 1985 | - | - |
| Revision 'A' | October 1985 | - | - |
| Revision 'B' | July 1987 | - | |
| Revision 'C' | December 1991 | | |

## DOCUMENTATION CHANGE NOTICE

| Rev. Letter | Rev. Date | CHANGE<br>Reference / Item | Approved DCR No. |
|---|---|---|---|
| 'A' | Oct. '85 | P1. Cover Page | None |
| | | P2. DCN | None |
| | | P4. T of C : Figure 2 Title changed and page numbers amended | 22364 |
| | | P6. Table 1(a) : Title amended and Variants -01 and -02 added | 22364 |
| | | P7(a) Figure 2 : New page added | 22364 |
| | | P8. Figure 2 : Title amended | 22364 |
| | | P9. Notes to Figs. : Flat pack notes added and title changed | 22364 |
| 'B' | Jul. '87 | P1. Cover Page | None |
| | | P2. DCN | None |
| | | P16. Table 2 : No. 1, Units corrected | 22499 |
| | | P18. Table 3 : No. 1, Units corrected | 22499 |
| 'C' | Dec. '91 | P1. Cover Page | None |
| | | P2. DCN | None |
| | | P12. Para. 4.2.2 : Deviation deleted, "None" added | 21048 |
| | | P13. Para. 4.2.4 : Deviation deleted, "None" added | 22919 |
| | | Para. 4.2.5 : Deviation deleted, "None" added | 22919 |
| | | This specification has been transferred from hardcopy to electronic format. The content is unchanged but minor differences in presentation exist. | |

## TABLE OF CONTENTS

## 1. GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, regulating pulse width modulator, based on Type SG 1524. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

### 1.2 TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

### 1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

### 1.4 PARAMETER DERATING INFORMATION

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

### 1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

### 1.6 PIN ASSIGNMENT

As per Figure 3(a).

### 1.7 TRUTH TABLE

Not applicable.

### 1.8 CIRCUIT SCHEMATIC

As per Figure 3(b).

### 1.9 FUNCTIONAL DIAGRAM

As per Figure 3(c).

## TABLE 1(a) - TYPE VARIANTS

| DASH No. | CASE | FIGURE | LEAD MATERIAL AND/OR FINISH |
|---|---|---|---|
| -01 | FLAT | 2(a) | D2 |
| -02 | FLAT | 2(a) | D3 or D4 |
| -05 | DIL | 2(b) | D2 |
| -06 | DIL | 2(b) | D3 or D4 |

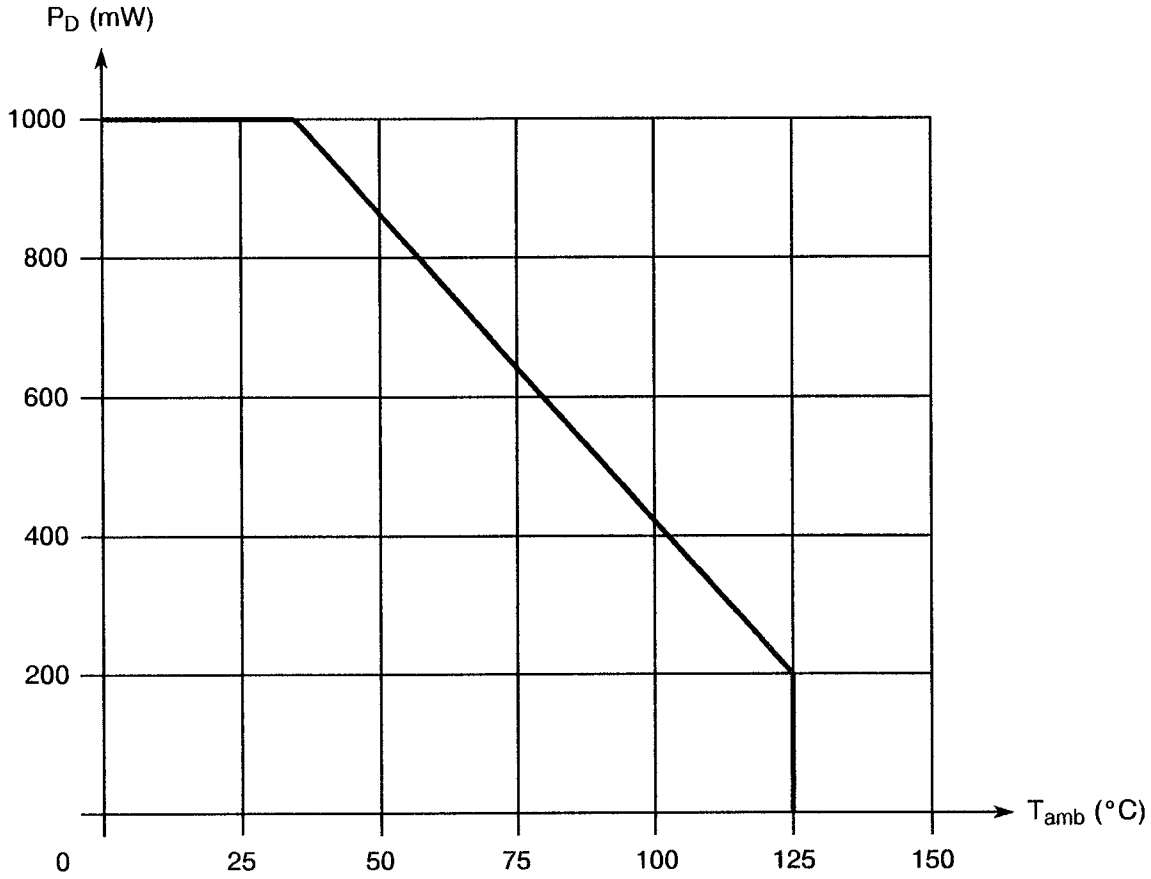
## TABLE 1(b) - MAXIMUM RATINGS

| No. | CHARACTERISTICS | SYMBOL | MAXIMUM RATINGS | UNITS | REMARKS |
|---|---|---|---|---|---|
| 1 | Supply Voltage | $V_{CC}$ | 40 | V | |
| 2 | Reference Output Current | $I_{REF}$ | 50 | mA | |
| 3 | Output Current (each Output) | $I_{OUT}$ | 100 | mA | |
| 4 | Oscillator Charging Current | $I_C$ | −5.0 | mA | |
| 5 | Device Dissipation | $P_D$ | 1000 | mWdc | Notes 1 and 2 |
| 6 | Operating Temperature | $T_{op}$ | −55 to +125 | °C | |
| 7 | Storage Temperature | $T_{stg}$ | −65 to +150 | °C | |
| 8 | Soldering Temperature | $T_{sol}$ | +265 | °C | Note 3 |

**NOTES**

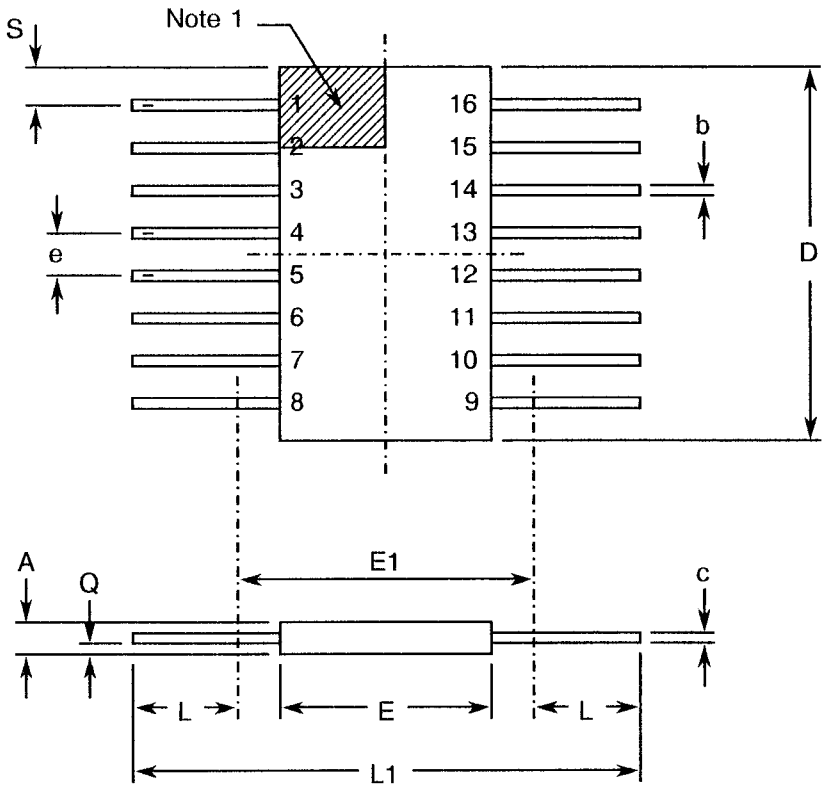
1. Must withstand added $P_D$ due to short circuit conditions (i.e. $I_{OS}$) at one output for 5 seconds.
2. At $T_{amb} \leq +25°C$. For derating at $T_{amb} > +25°C$, see Figure 1.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the package and the same lead shall not be resoldered until 3 minutes have elapsed.

**FIGURE 1 - DEVICE DISSIPATION DERATING WITH TEMPERATURE**



## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(a) - FLAT PACKAGE

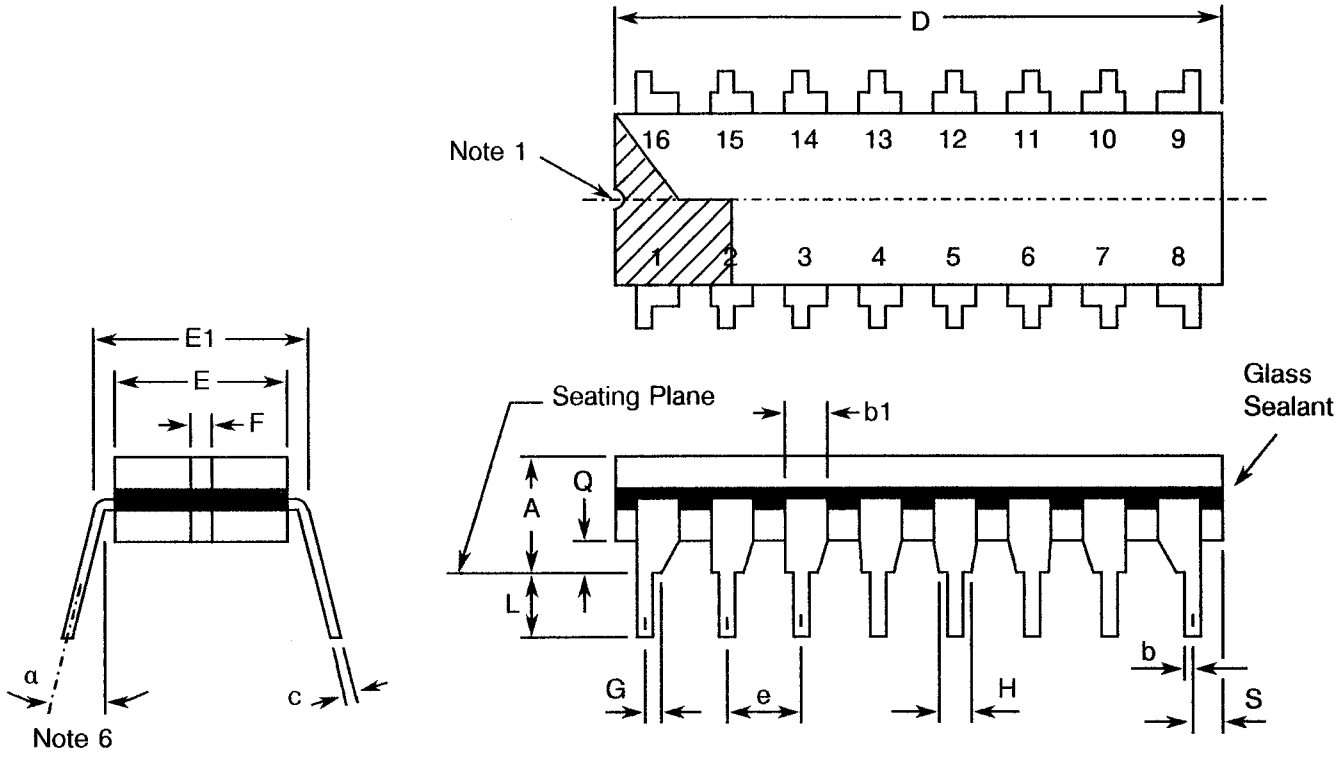



| SYMBOL | INCHES | | MILLIMETRES | | NOTES |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 0.049 | 0.080 | 1.24 | 2.03 | |
| b | 0.015 | 0.019 | 0.38 | 0.48 | 6 |
| c | 0.003 | 0.006 | 0.08 | 0.15 | 6 |
| D | 0.371 | 0.417 | 9.42 | 10.16 | |
| E | 0.247 | 0.285 | 6.27 | 7.24 | |
| E1 | - | 0.300 | - | 7.62 | 3 |
| e | 0.050 TYP. | | 1.27 TYP. | | 7, 10 |
| L | 0.310 | 0.350 | 7.87 | 8.89 | |
| L1 | 0.937 | 0.961 | 23.80 | 24.40 | |
| Q | 0.020 | 0.040 | 0.51 | 1.02 | 9 |
| S | 0.010 | 0.025 | 0.25 | 0.64 | 5 |

**NOTES:** See Page 9.

## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DIL PACKAGE




| SYMBOL | INCHES | | MILLIMETRES | | NOTES |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | - | 0.200 | - | 5.08 | |
| b | 0.015 | 0.023 | 0.38 | 0.58 | 6 |
| b1 | - | 0.070 | - | 1.78 | 6 |
| c | 0.008 | 0.014 | 0.203 | 0.356 | 6 |
| D | 0.755 | 0.785 | 19.18 | 19.94 | |
| E | 0.245 | 0.280 | 6.22 | 7.11 | |
| E1 | 0.290 | 0.310 | 7.37 | 7.87 | 3 |
| e | 0.100 TYP. | | 2.54 TYP. | | 4, 7 |
| G | 0.012 | - | 0.305 | - | |
| H | 0.030 | - | 0.76 | - | |
| L | 0.130 | 0.200 | 3.30 | 5.08 | |
| Q | 0.020 | 0.080 | 0.51 | 2.03 | 2 |
| S | 0.015 | 0.050 | 0.38 | 1.27 | 5 |
| α | 0° | 15° | 0° | 15° | 8 |

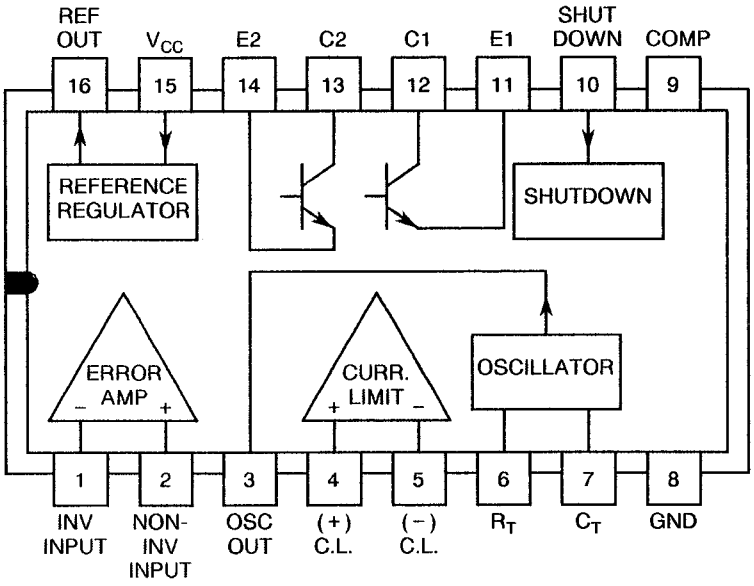
**NOTES:** See Page 9.

**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

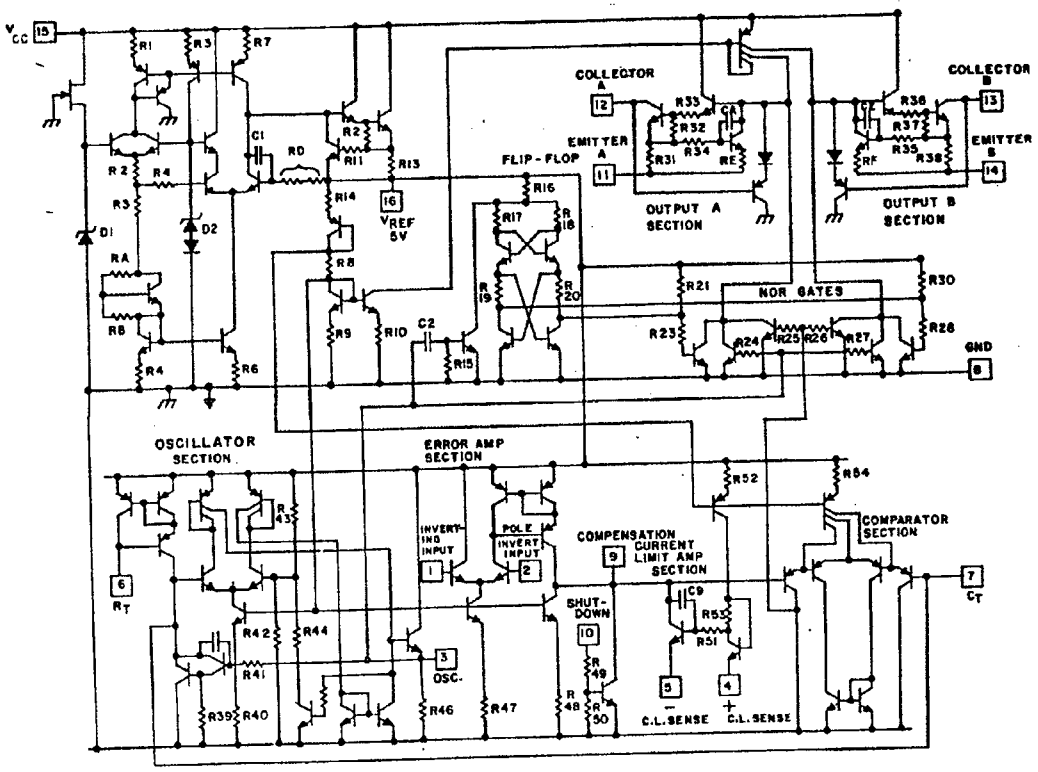
NOTES TO FIGURES 2(a) AND 2(b)

1. Index area; a notch or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. This dimension allows for off-centre lids, meniscus and glass overrun.
4. The true position pin spacing is 0.100 inch (2.54mm) between centrelines. Each pin centreline shall be located within ±0.010 inch (±0.25mm) of its true longitudinal position relative to Pins 1 and 16.
5. Applies to all 4 corners.
6. All leads.
7. 14 spaces.
8. Lead centre when $\alpha$ is 0°.
9. Dimension Q shall be measured at the point of exit of the lead from the body.
10. The true position pin spacing is 0.050 inch (1.27mm) between centrelines. Each pin centreline shall be located within ±0.005 inch (±0.13mm) of its true longitudinal position relative to Pins 1 and 16.

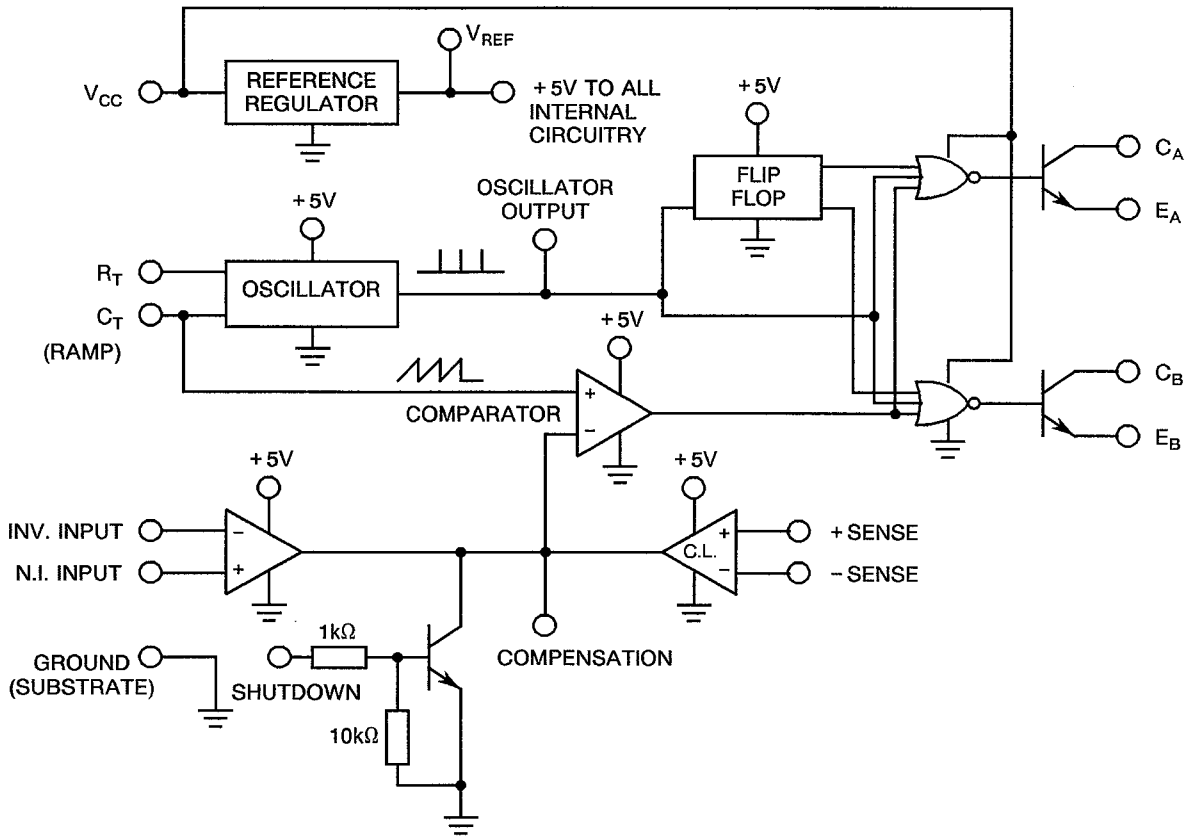
**FIGURE 3(a) - PIN ASSIGNMENT**



## FIGURE 3(b) - CIRCUIT SCHEMATIC




## FIGURE 3(c) - FUNCTIONAL DIAGRAM



## 2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

(c) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

## 3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

## 4. REQUIREMENTS

### 4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

### 4.2 DEVIATIONS FROM GENERIC SPECIFICATION

#### 4.2.1 Deviations from Special In-process Controls

None.

#### 4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) High Temperature Reverse Bias Test: Shall not be performed.

(b) Electrical Measurements at High and Low Temperatures:-
A test result summary, based on go-no-go tests and presented in histogram form, shall replace the requirement for read-and-record data for High and Low Temperature Measurements.

4.2.4 Deviations from Qualification, Environmental and Endurance Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.0 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or ceramic body, and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with either Type '2' or Type '3 or 4' finish in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

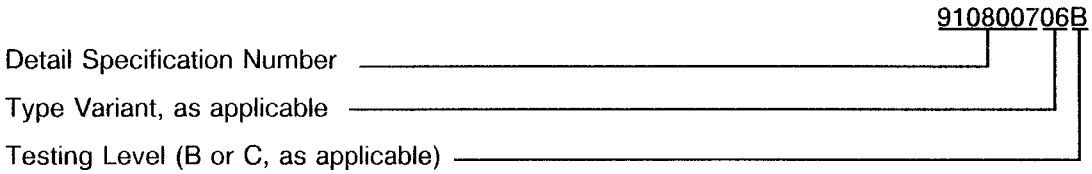
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering shall be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:




4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL CHARACTERISTICS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$°C and $-55(+5-0)$°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values ($\Delta$) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-in

The requirements for burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Burn-in

The circuit for use in performing the burn-in tests is shown in Figure 5 of this specification.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

| No. | Characteristics | Symbol | Test Method MIL-STD | | Test Fig. | Test Conditions (Pins Under Test) (Note 1) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 883 | 750 | | | Min | Max | |
| 1 | Standby Current | $I_Q$ | 3005 | - | 4(a) | $V_{IN}$ (Pin 2) = 2.0V<br>$V_{IN}$ (Pins 1-4-7-8-9-11-14) = 0V<br>Remaining inputs and outputs open.<br>$V_{CC}$ = 40V<br>(Pin 15) | 0.5 | 10 | mA |
| 2 | Reference Output Voltage | $V_{REF}$ | - | - | 4(b) | $V_{IN}$ (Pin 15) = 20V<br>(Pin 16) | 4.8 | 5.4 | V |
| 3 | Input Regulation Voltage | $V_{IR}$ | - | - | 4(b) | $V_{IN}$ (Pin 15) = 8.0 to 40 V<br>(Pin 16) | - | 20 | mV |
| 4 | Load Regulation Voltage | $V_{OR}$ | - | - | 4(b) | $I_L$ = 0 to 20 mA<br>(Pin 16) | - | 50 | mV |
| 5 | Shut-down Output Current | $I_{OS}$ | - | - | 4(b) | $V_{OUT}$ (Pin 16) = 0V<br>(Pin 16) | - | − 120 | mA |
| 6 to 7 | Collector-Base Leakage Current | $I_{CBO}$ | - | 3036 | 4(c) | $V_{CC}$ = 45V<br>(Pins 12-13) | - | 50 | µA |
| 8 to 9 | Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | - | 3071 | 4(c) | $I_C$ = 50mA<br>(Pins 12 to 11-13 to 14) | - | 2.0 | V |
| 10 to 11 | Emitter Output Voltage | $V_E$ | - | 3020 | 4(c) | $I_E$ = − 250mA<br>(Pins 11-14) | 17 | - | V |
| 12 | Input Bias Current + | $I_{B+}$ | 4001 | - | 4(d) | $V_{IC}$ = 2.5V<br>(Pins 1 to 2) | - | 10 | µA |
| 13 | Input Bias Current − | $I_{B-}$ | 4001 | - | 4(d) | $V_{IC}$ = 2.5V<br>(Pins 1 to 2) | - | 10 | µA |
| 14 | Input Offset Current | $I_{IO}$ | 4001 | - | 4(d) | $V_{CM}$ = 2.5V<br>(Pins 1 to 2) | - | 2.0 | µA |
| 15 | Input Offset Voltage | $V_{IO}$ | 4001 | - | 4(d) | $V_{IC}$ = 2.5V<br>(Pins 1 to 2) | - | 5.0 | mV |
| 16 | Open Loop Voltage Gain | $A_{VS}$ | 4004 | - | 4(e) | $V_{OUT}$ = 1.0 to 3.4 V<br>(Pin 9) | 72 | - | dB |
| 17 | Common Mode Rejection Ratio | CMRR | 4003 | - | 4(f) | $V_{CM}$ = 1.8 to 3.4 V<br>(Pins 2 to 9) | 50 | - | dB |
| 18 | Current Compensation | $I_{COMP}$ | - | - | 4(a) | $V_{IN}$ = 3.0V<br>$V_{OUT}$ = 2.5V<br>(Pin 9) | 50 | 150 | µA |

**NOTES**: 1. Unless otherwise specified: $V_{CC}$ = 20V, f = 20kHz.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

| No. | Characteristics | Symbol | Test Method MIL-STD | | Test Fig. | Test Conditions (Pins Under Test) (Note 1) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 883 | 750 | | | Min | Max | |
| 19 | Current Compensation Change | $\Delta I_{COMP}$ | - | - | 4(a) | $V_{IN}$ = 0 to 3.0 V<br>$V_{OUT}$ = 2.5V<br>(Pin 9) | - | ± 10 | µA |
| 20 | Current Bias Shutdown (1) | $I_{SD1}$ | - | - | 4(a) | $V_{COMP}$ = 0.5V<br>(Pin 10) | 40 | 150 | µA |
| 21 | Current Bias Shutdown (2) | $I_{SD2}$ | - | - | 4(a) | $V_{COMP}$ = 5.0V<br>(Pin 10) | - | 7.0 | mA |
| 22 | Offset Voltage Amplifier Current Limit | $V_{CL}$ | - | - | 4(a) | $V_{COMP}$ = 2.0V<br>(Pins 4 to 5) | 160 | 300 | mV |
| 23 | Oscillator Input Bias Current (1) | $I_{OSC1}$ | - | - | 4(a) | $V_{IN}$ = 3.5V<br>$V_{OUT}$ = 2.5V<br>(Pin 7) | - | ± 10 | µA |
| 24 | Oscillator Input Bias Current (2) | $I_{OSC2}$ | - | - | 4(a) | $V_{IN}$ = 0V<br>$V_{OUT}$ = 2.5V<br>(Pin 7) | - | ± 10 | µA |

**NOTES**: 1. Unless otherwise specified: $V_{CC}$ = 20V, f = 20kHz.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

| No. | Characteristics | Symbol | Test Method MIL-STD | | Test Fig. | Test Conditions (Pins Under Test) (Note 1) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 883 | 750 | | | Min | Max | |
| 25 | Max. Oscillator Frequency (1) | $f_{MAX1}$ | - | - | - | $R_T$ = 1.8kΩ, $C_T$ = 1.0nF<br>$V_{CC}$ = 8.0V<br>(Pin 3) | 300 | - | kHz |
| 26 | Max. Oscillator Frequency (2) | $f_{MAX2}$ | - | - | - | $R_T$ = 1.8kΩ, $C_T$ = 1.0nF<br>(Pin 3) | 300 | - | kHz |
| 27 | Oscillator Output Pulse Width | $t_p$ | - | - | - | $R_T$ = 1.8kΩ, $C_T$ = 1.0nF<br>$V_{CC}$ = 8.0V<br>(Pin 3) | 0.2 | 0.8 | µs |
| 28 | Dead Time | $t_d$ | - | - | 4(g) | $R_T$ = 1.8kΩ, $C_T$ = 10nF<br>(Pins 12 to 13) | 0.6 | 1.5 | µs |
| 29 to 30 | Turn-on Voltage Rise Time | $t_r$ | - | 3251 | - | $R_C$ = 2.0kΩ<br>(Pins 12-13) | - | 0.4 | µs |
| 31 to 32 | Turn-off Voltage Fall Time | $t_f$ | - | 3251 | - | $R_C$ = 2.0kΩ<br>(Pins 12-13) | - | 0.2 | µs |

**NOTES**: 1. Unless otherwise specified: $V_{CC}$ = 20V, f = 20kHz.

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0-0)°C, -55(+5-0)°C**

| No. | Characteristics | Symbol | Test Method MIL-STD | | Test Fig. | Test Conditions (Pins Under Test) (Note 1) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 883 | 750 | | | Min | Max | |
| 1 | Standby Current | $I_Q$ | 3005 | - | 4(a) | $V_{IN}$ (Pin 2) = 2.0V<br>$V_{IN}$ (Pins 1-4-7-8-9-11-14) = 0V<br>Remaining inputs and outputs open.<br>$V_{CC}$ = 40V<br>(Pin 15) | 0.5 | 10 | mA |
| 2 | Reference Output Voltage | $V_{REF}$ | - | - | 4(b) | $V_{IN}$ (Pin 15) = 20V<br>(Pin 16) | 4.8 | 5.4 | V |
| 3 | Input Regulation Voltage | $V_{IR}$ | - | - | 4(b) | $V_{IN}$ (Pin 15) = 8.0 to 40 V<br>(Pin 16) | - | 20 | mV |
| 4 | Load Regulation Voltage | $V_{OR}$ | - | - | 4(b) | $I_L$ = 0 to 20 mA<br>(Pin 16) | - | 50 | mV |
| 5 | Shut-down Output Current | $I_{OS}$ | - | - | 4(b) | $V_{OUT}$ (Pin 16) = 0V<br>(Pin 16) | - | -120 | mA |
| 6 to 7 | Collector-Base Leakage Current | $I_{CBO}$ | - | 3036 | 4(c) | $V_{CC}$ = 45V<br>(Pins 12-13) | - | 50 | µA |
| 8 to 9 | Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | - | 3071 | 4(c) | $I_C$ = 50mA<br>(Pins 12 to 11-13 to 14) | - | 2.0 | V |
| 10 to 11 | Emitter Output Voltage | $V_E$ | - | 3020 | 4(c) | $I_E$ = -250mA<br>(Pins 11-14) | 17 | - | V |
| 12 | Input Bias Current + | $I_{B+}$ | 4001 | - | 4(d) | $V_{IC}$ = 2.5V<br>(Pins 1 to 2) | - | 10 | µA |
| 13 | Input Bias Current - | $I_{B-}$ | 4001 | - | 4(d) | $V_{IC}$ = 2.5V<br>(Pins 1 to 2) | - | 10 | µA |
| 14 | Input Offset Current | $I_{IO}$ | 4001 | - | 4(d) | $V_{CM}$ = 2.5V<br>(Pins 1 to 2) | - | 2.0 | µA |
| 15 | Input Offset Voltage | $V_{IO}$ | 4001 | - | 4(d) | $V_{IC}$ = 2.5V<br>(Pins 1 to 2) | - | 5.0 | mV |
| 16 | Open Loop Voltage Gain | $A_{VS}$ | 4004 | - | 4(e) | $V_{OUT}$ = 1.0 to 3.4 V<br>(Pin 9) | 72 | - | dB |
| 17 | Common Mode Rejection Ratio | CMRR | 4003 | - | 4(f) | $V_{CM}$ = 1.8 to 3.4 V<br>(Pins 2 to 9) | 50 | - | dB |
| 18 | Current Compensation | $I_{COMP}$ | - | - | 4(a) | $V_{IN}$ = 3.0V<br>$V_{OUT}$ = 2.5V<br>(Pin 9) | 50 | 150 | µA |

**NOTES:** 1. Unless otherwise specified: $V_{CC}$ = 20V, f = 20kHz.

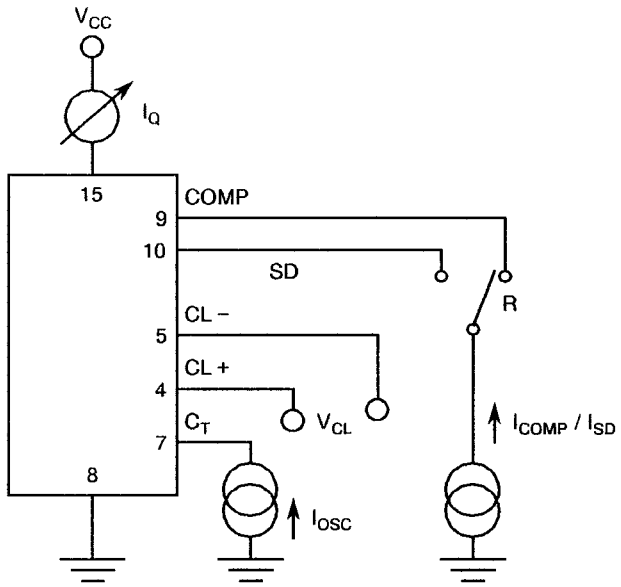
**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0-5)°C, -55(+5-0)°C (CONT'D)**

| No. | Characteristics | Symbol | Test Method MIL-STD | | Test Fig. | Test Conditions (Pins Under Test) (Note 1) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 883 | 750 | | | Min | Max | |
| 19 | Current Compensation Change | $\Delta I_{COMP}$ | - | - | 4(a) | $V_{IN}$ = 0 to 3.0 V<br>$V_{OUT}$ = 2.5V<br>(Pin 9) | - | ± 10 | µA |
| 20 | Current Bias Shutdown (1) | $I_{SD1}$ | - | - | 4(a) | $V_{COMP}$ = 0.5V<br>(Pin 10) | 40 | 150 | µA |
| 21 | Current Bias Shutdown (2) | $I_{SD2}$ | - | - | 4(a) | $V_{COMP}$ = 5.0V<br>(Pin 10) | - | 7.0 | mA |
| 22 | Offset Voltage Amplifier Current Limit | $V_{CL}$ | - | - | 4(a) | $V_{COMP}$ = 2.0V<br>(Pins 4 to 5) | 160 | 300 | mV |
| 23 | Oscillator Input Bias Current (1) | $I_{OSC1}$ | - | - | 4(a) | $V_{IN}$ = 3.5V<br>$V_{OUT}$ = 2.5V<br>(Pin 7) | - | ± 10 | µA |
| 24 | Oscillator Input Bias Current (2) | $I_{OSC2}$ | - | - | 4(a) | $V_{IN}$ = 0V<br>$V_{OUT}$ = 2.5V<br>(Pin 7) | - | ± 10 | µA |

**NOTES:** 1. Unless otherwise specified: $V_{CC}$ = 20V, f = 20kHz.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

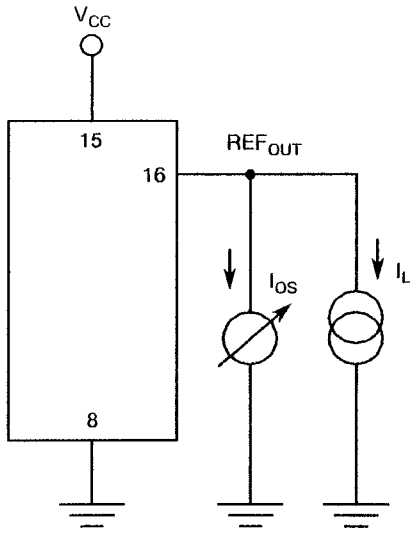
FIGURE 4(a) - STANDBY CURRENT, CURRENT COMPENSATION, CURRENT COMPENSATION CHANGE, CURRENT BIAS SHUTDOWN, OFFSET VOLTAGE AMPLIFIER CURRENT LIMIT AND INPUT BIAS CURRENT OSCILLATION




**NOTES**

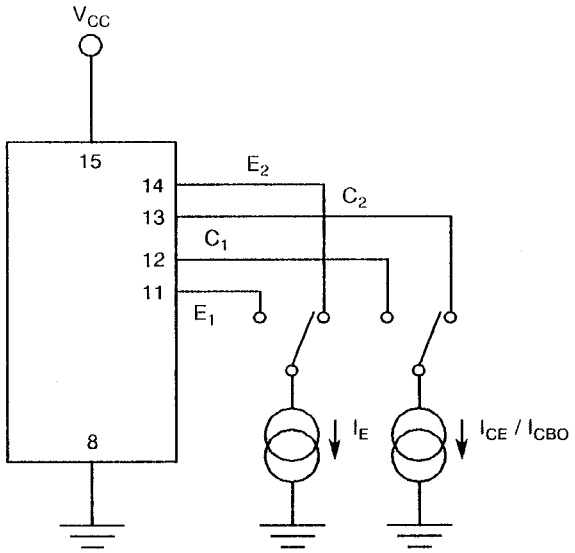
1. R is normally closed when $I_{COMP}$ is tested.

FIGURE 4(b) - REFERENCE OUTPUT VOLTAGE, INPUT REGULATION VOLTAGE, LOAD REGULATION VOLTAGE AND SHUTDOWN OUTPUT CURRENT



## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

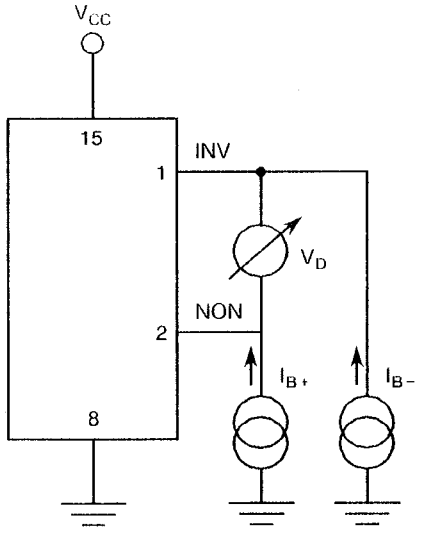
FIGURE 4(c) - COLLECTOR BASE LEAKAGE CURRENT, COLLECTOR-EMITTER SATURATION VOLTAGE AND EMITTER OUTPUT VOLTAGE




**NOTES**

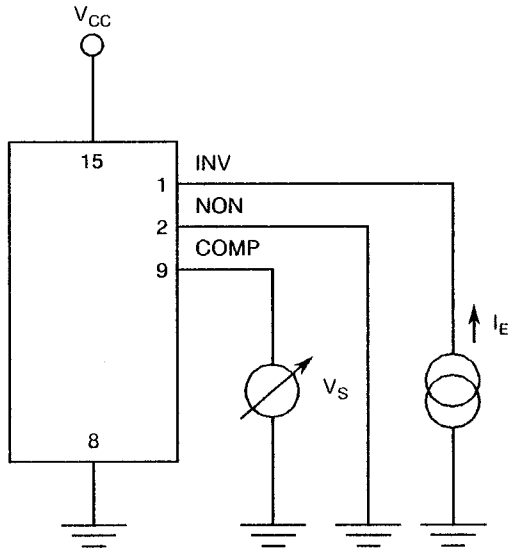
1. Figures E1 and E2 are grounded when $I_{CBD}$ and $V_{SAT}$ are tested.

FIGURE 4(d) - INPUT BIAS CURRENT +, INPUT BIAS CURRENT − AND INPUT OFFSET VOLTAGE



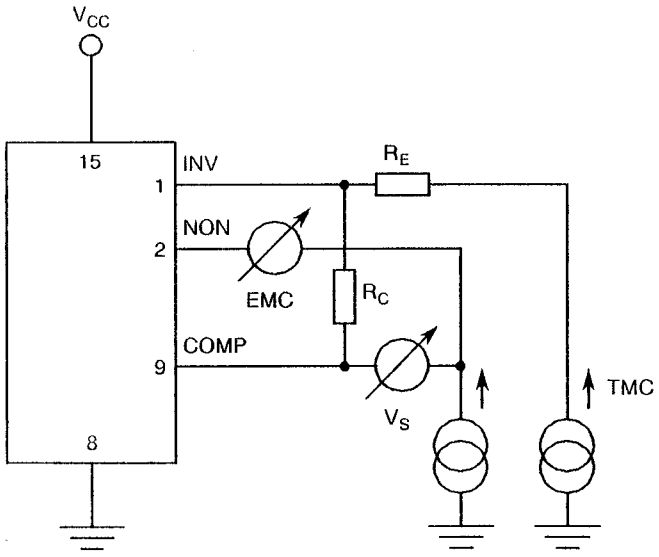
## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - OPEN LOOP VOLTAGE GAIN




$$G = 20 \text{ Log } \frac{V_S}{V_E}$$

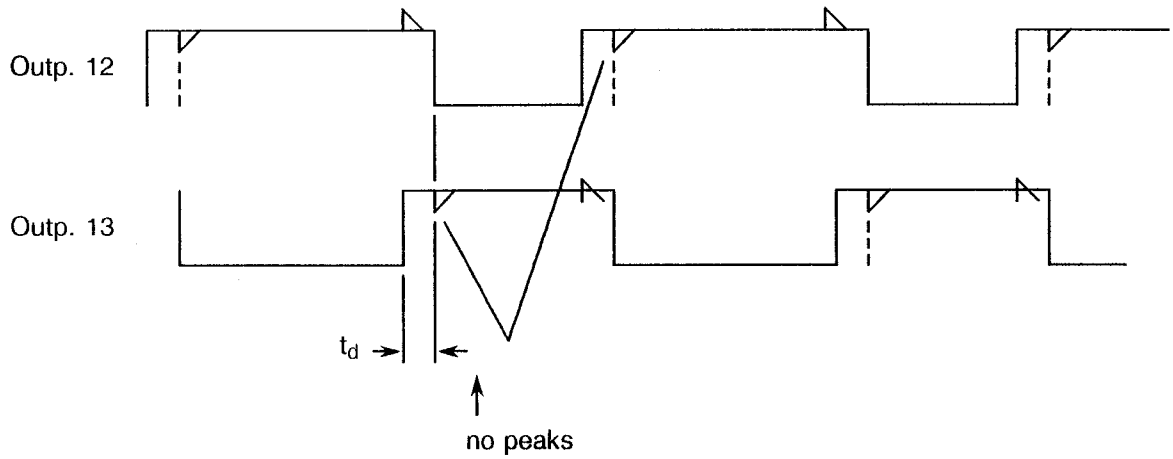
FIGURE 4(f) - COMMON MODE REJECTION RATIO




$$CMRR = \left( \frac{TMC}{V_S - TMC} \right) \left( 1 + \frac{R_C}{R_E} \right)$$

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - OUTPUT WAVEFORM FOR DEAD TIME MEASUREMENT



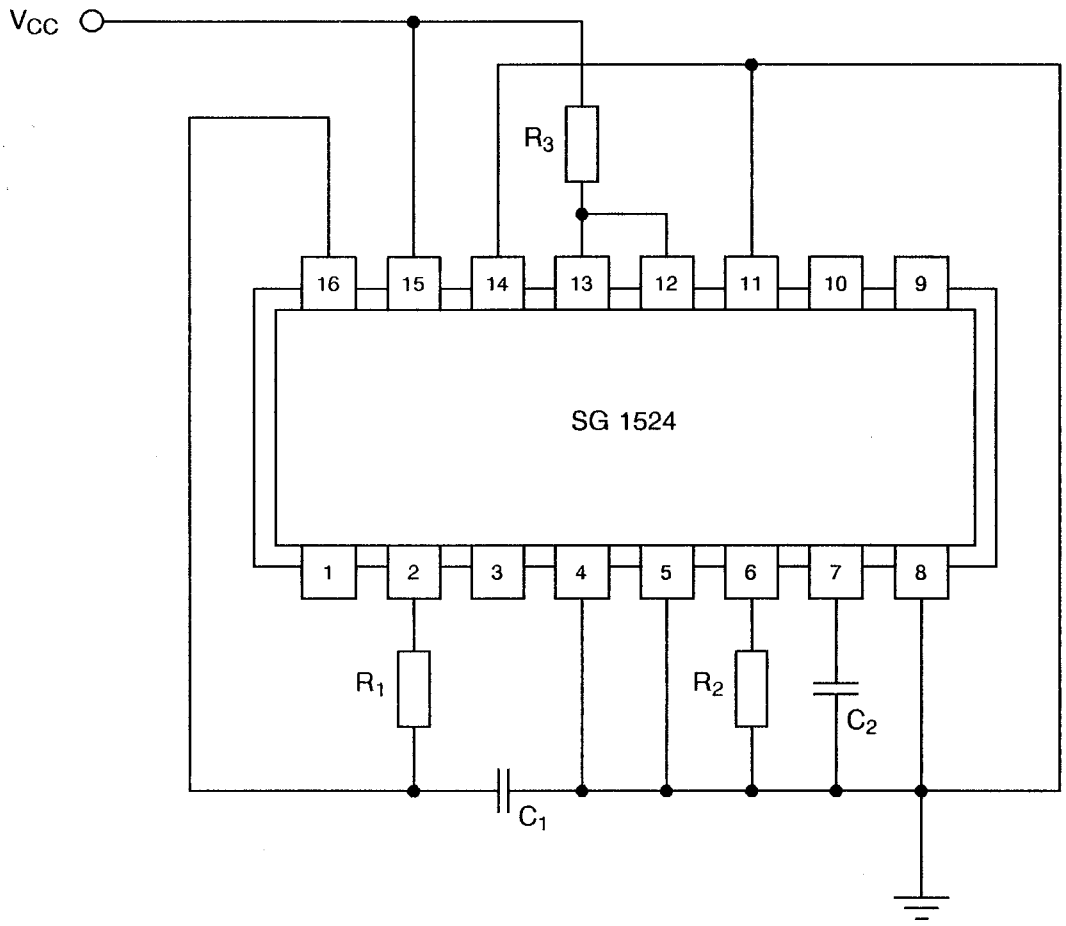
## TABLE 4 - PARAMETER DRIFT VALUES

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | CHANGE LIMITS (Δ) | UNIT |
|---|---|---|---|---|---|---|
| 1 | Standby Current | $I_Q$ | As per Table 2 | As per Table 2 | ±5.0 | % |
| 2 | Reference Output Voltage | $V_{REF}$ | As per Table 2 | As per Table 2 | ±2.0 | % |
| 3 | Input Regulation Voltage | $V_{IR}$ | As per Table 2 | As per Table 2 | ±5.0 | mV |
| 4 | Collector-Base Leakage Current | $I_{CBO}$ | As per Table 2 | As per Table 2 | ±10 | µA |
| 5 | Input Offset Voltage | $V_{IO}$ | As per Table 2 | As per Table 2 | ±1.0 | mV |

## TABLE 5 - CONDITIONS FOR BURN-IN AND OPERATING LIFE TEST

| No. | CHARACTERISTICS | SYMBOL | CONDITION | UNIT |
|---|---|---|---|---|
| 1 | Ambient Temperature | $T_{amb}$ | +125(+0−5) | °C |
| 2 | Supply Voltage | $V_{CC}$ | 30 | V |

## FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN AND OPERATING LIFE TEST




**NOTES**

1. $R_1 = 100k\Omega$.
   $R_2 = 1.8k\Omega$.
   $R_3 = 2.0k\Omega$, 1.0W.
   $C_1 = 0.1\mu F$.
   $C_2 = 1.0nF$.

## 4.8 ENVIRONMENTAL AND ENDURANCE TESTS

### 4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

### 4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

### 4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

### 4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

### 4.8.5 Electrical Circuits for Operating Life Tests

The circuits for use in performing the operating life tests is shown in Figure 5.

### 4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS DURING AND ON COMPLETION OF ENDURANCE TESTING**

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | CHANGE LIMITS (Δ) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 1 | Standby Current | $I_Q$ | As per Table 2 | As per Table 2 | ±5.0 | - | - | % |
| 2 | Reference Output Voltage | $V_{REF}$ | As per Table 2 | As per Table 2 | ±2.0 | - | - | % |
| 3 | Input Regulation Voltage | $V_{IR}$ | As per Table 2 | As per Table 2 | ±5.0 | - | - | mV |
| 6 to 7 | Collector-Base Leakage Current | $I_{CBO}$ | As per Table 2 | As per Table 2 | ±10 | - | - | µA |
| 15 | Input Offset Voltage | $V_{IO}$ | As per Table 2 | As per Table 2 | ±1.0 | - | - | mV |

**APPENDIX 'A'**



AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|---|---|
| Para. 4.2.1 | Scanning Electron Microscope (SEM) Inspection may be performed using TIF document TIF 3.61.610.001. |
| Para. 4.2.2<br>Para. 4.2.4<br>Para. 4.2.5 | External Visual Inspection may be performed using TIF document TI 50.42-3035. |
| Para. 4.2.3 | As for 4.2.2 plus Radiographic Inspection may be performed using TIF document TIF 50.42-3002. |
| Para. 4.2.2 | Internal Visual Inspection may be performed using TIF documents TI 50.22.1045 and TI 50.22.1002. |
| Para. 4.2.2 | Prior to Die Shear Test, TIF may perform a Radiographic Inspection on the randomly chosen samples to be subjected to this test. |
| Para. 4.2.2<br>Para. 4.2.3<br>Para. 4.2.4<br>Para. 4.2.5 | Seal Test (Fine Leak) may be performed using TIF document 50.42.1024 and Seal Test (Gross Leak) may be performed using TIF document 50.42.2015. |