



Page 1 of 24

**INTEGRATED CIRCUITS, MONOLITHIC, CMOS  
SILICON-ON-SAPPHIRE, 7-BIT RF DIGITAL STEP  
ATTENUATOR, 50Ohm**

**BASED ON TYPE PE43751**

**ESCC Detail Specification No. 9202/081**

Issue 1	July 2014
---------	-----------



Document Custodian: European Space Agency – see <https://escies.org>

**LEGAL DISCLAIMER AND COPYRIGHT**

European Space Agency, Copyright © 2014. All rights reserved.

The European Space Agency disclaims any liability or responsibility, to any person or entity, with respect to any loss or damage caused, or alleged to be caused, directly or indirectly by the use and application of this ESCC publication.

This publication, without the prior permission of the European Space Agency and provided that it is not used for a commercial purpose, may be:

- copied in whole, in any medium, without alteration or modification.
- copied in part, in any medium, provided that the ESCC document identification, comprising the ESCC symbol, document number and document issue, is removed.



**DOCUMENTATION CHANGE NOTICE**

(Refer to <https://escies.org> for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

**TABLE OF CONTENTS**

1	GENERAL	5
1.1	SCOPE	5
1.2	APPLICABLE DOCUMENTS	5
1.3	TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS	5
1.4	THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS	5
1.4.1	The ESCC Component Number	5
1.4.2	Component Type Variants	5
1.5	MAXIMUM RATINGS	6
1.6	HANDLING PRECAUTIONS	6
1.7	PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION	7
1.7.1	Ceramic Quad Flat Package (CQFP-32) - 32 Terminals	7
1.8	FUNCTIONAL DIAGRAM	8
1.9	PIN ASSIGNMENT AND DESCRIPTION	9
1.10	FUNCTIONAL DESCRIPTION	9
1.10.1	Overview	9
1.10.1.1	Parallel/Serial Selection	10
1.10.1.2	Serial Mode Interface	10
1.10.1.3	Parallel Mode Interface	12
1.10.1.4	Reset Control	13
1.11	INPUT AND OUTPUT PROTECTION NETWORKS	14
2	REQUIREMENTS	15
2.1	GENERAL	15
2.1.1	Deviations from the Generic Specification	15
2.1.1.1	Deviations from Screening Tests - Chart F3	15
2.2	MARKING	15
2.3	ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES	15
2.3.1	Room Temperature Electrical Measurements	15
2.3.2	High and Low Temperatures Electrical Measurements	20
2.4	PARAMETER DRIFT VALUES	20
2.5	INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS	21
2.6	POWER BURN-IN CONDITIONS	21
2.7	OPERATING LIFE CONDITIONS	22
2.8	TOTAL DOSE RADIATION TESTING	22
2.8.1	Bias Conditions and Total Dose Level for Total Dose Radiation Testing	22
2.8.2	Electrical Measurements for Total Dose Radiation Testing	23
	APPENDIX 'A'	24

## 1 GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

### 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000.
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

### 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

### 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

#### 1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920208101R

- Detail Specification Reference: 9202081
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R (as required)

#### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	PE43751	CQFP-32	G2	10	R [100kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

### 1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Prolonged use of the device at the maximum ratings may reduce the device's overall reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Positive Power Supply Voltage Range	$V_{DD}$	-0.3 to 4	V	Note 1
Negative Power Supply Voltage Range	$V_{SS}$	-3.7 to 0.3	V	Note 2
Voltage at any Digital Input	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V	Note 3
Input Power (50 $\Omega$ ) Range 9kHz $\leq f_{in} \leq$ 20MHz 20MHz $< f_{in} \leq$ 6GHz	$P_{in}$	+9 +23	dBm dBm	
Operating Temperature Range	$T_{op}$	-40 to +85	$^{\circ}C$	
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}C$	
Soldering Temperature	$T_{sol}$	+265	$^{\circ}C$	Note 4

#### **NOTES:**

1. Device is functional for  $2.7V < V_{DD} < 3.6V$ .
2. Device is functional for  $-3.3V < V_{SS} < -2.7V$ .
3. Device is functional for 0V to  $V_{DD}$
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed

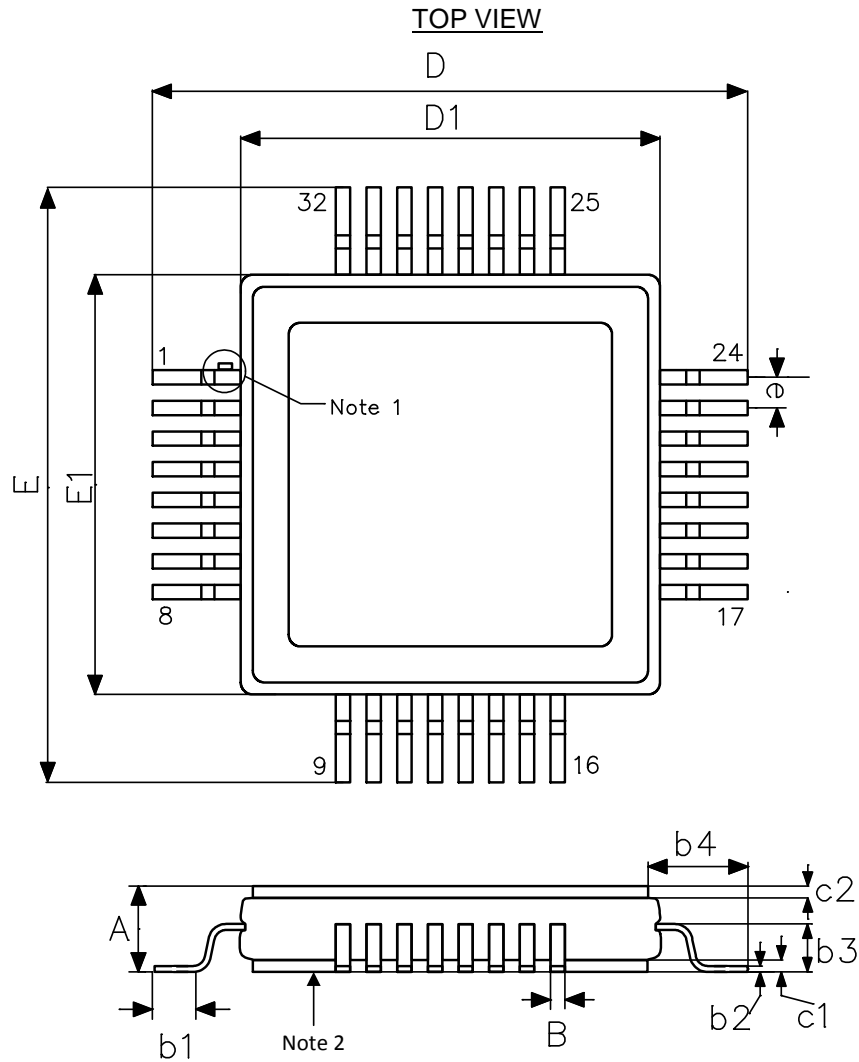
### 1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 4000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

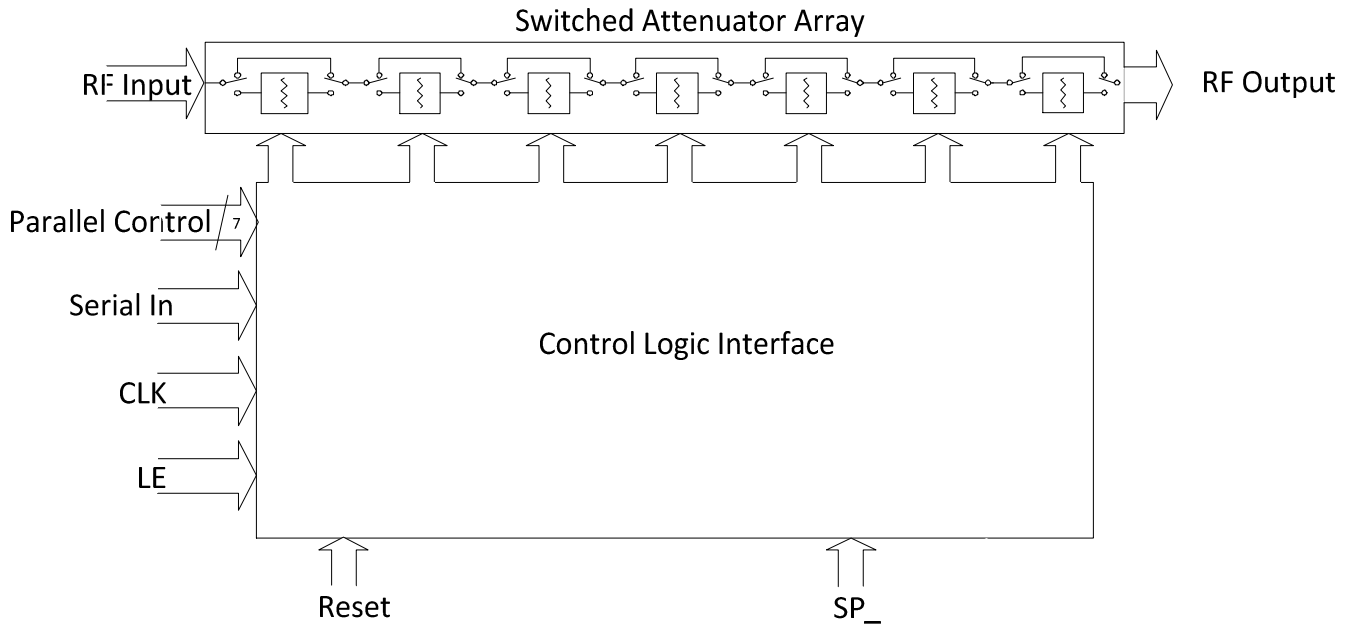
1.7.1 Ceramic Quad Flat Package (CQFP-32) - 32 Terminals



Symbols	Dimensions (mm)		Notes
	Min	Max	
A	-	1.82	3
B	0.25	0.35	3
b1	0.88	-	3
b2	0.1	0.16	3
b3	0.76 Typical		3
b4	2.26 Typical		3
c1	0.2	0.3	3
c2	0.25 Typical		
D / E	12.93 Typical		3
D1 / E1	-	8.89	
e	0.65 BSC		3

**NOTES:**

1. A terminal 'pip' identification mark shall be located in the region of Pin 1 as shown. Terminal numbers shall increase counter clockwise when viewed from the top of the package.
2. The bottom of the package shall have a paddle (an exposed solder pad) for connection to ground.
3. Applies to all 32 terminals (8 per side).

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT AND DESCRIPTION

The table below describes each pin's assignment, type and standard, plus a brief description of its functionality.

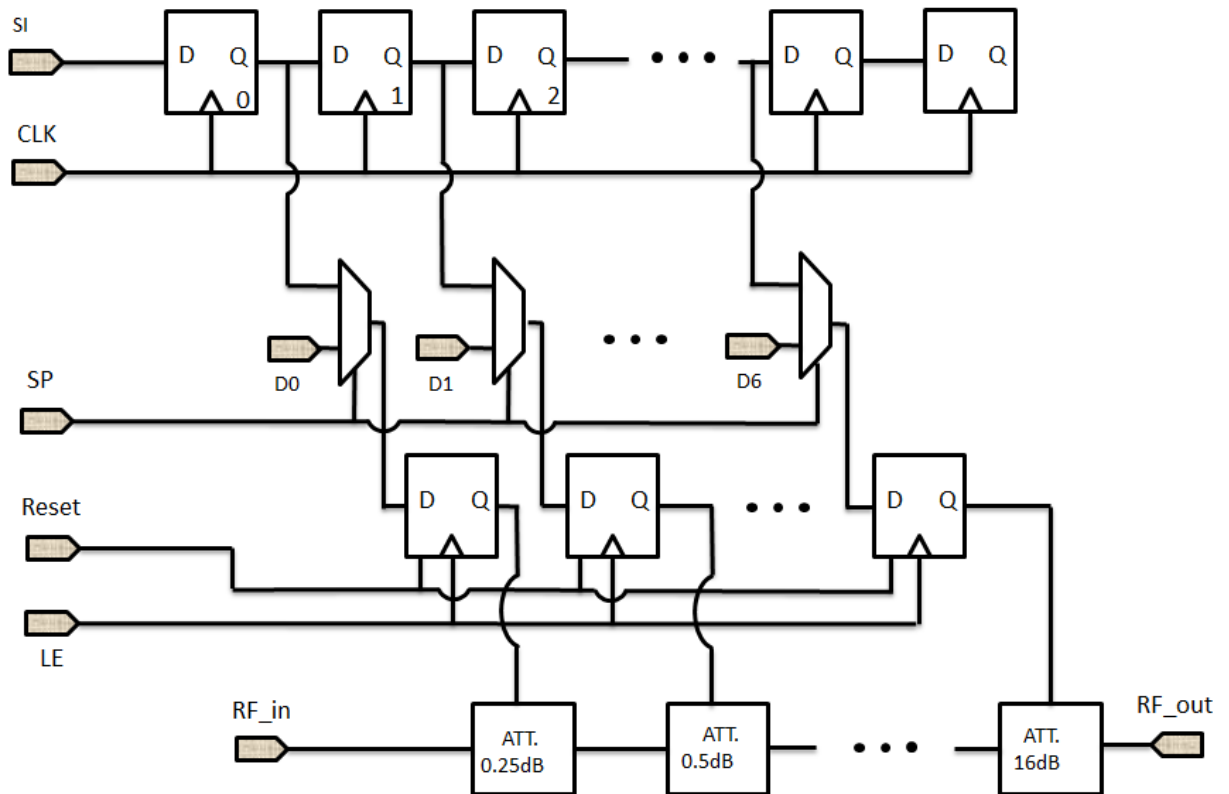
Pin No.	Pin Name	Pin Type	Pin Standard	Serial/Parallel Mode	Description
1	GND	-	-	-	Ground
2	SP	Digital Input	CMOS	Both	Serial/Parallel mode select
3	RESET	Digital Input	CMOS	Both	Reset to maximum attenuation
4	VDD	Power Supply	-	-	Positive power supply pin
5	GND	-	-	-	Ground
6	RFIN	Analogue Input	RF	Both	50Ω RF input port
7-18	GND	-	-	-	Ground
19	RFOUT	Analogue Output	RF	Both	50Ω RF output port
20	GND	-	-	-	Ground
21	VSS	Power Supply	-	-	Negative power supply pin
22	LE	Digital Input	CMOS	Both	Transparent latch enable
23	SI	Digital Input	CMOS	Serial	Serial interface Data input
24	GND	-	-	-	Ground
25	CLK	Digital Input	CMOS	Serial	Serial interface Clock input
26	D0	Digital Input	CMOS	Parallel	Parallel control bit: 0.25dB
27	D1	Digital Input	CMOS	Parallel	Parallel control bit: 0.5dB
28	D2	Digital Input	CMOS	Parallel	Parallel control bit: 1dB
29	D3	Digital Input	CMOS	Parallel	Parallel control bit: 2dB
30	D4	Digital Input	CMOS	Parallel	Parallel control bit: 4dB
31	D5	Digital Input	CMOS	Parallel	Parallel control bit: 8dB
32	D6	Digital Input	CMOS	Parallel	Parallel control bit: 16dB
Paddle	GND	-	-	-	Ground

1.10 FUNCTIONAL DESCRIPTION

1.10.1 Overview

The PE43751 Digital Step Attenuator (DSA) consists of 50Ω resistive attenuators and CMOS/SOS RF switches to provide both high linearity and bandwidth. The switches are controlled via integrated CMOS logic.

Digital Step Attenuator Block Diagram



1.10.1.1 Parallel/Serial Selection

Either a parallel or serial-addressable interface can be used to control the DSA. The SP bit provides this selection, with SP = LOW selecting the parallel interface and SP = HIGH selecting the serial-addressable interface.


1.10.1.2 Serial Mode Interface

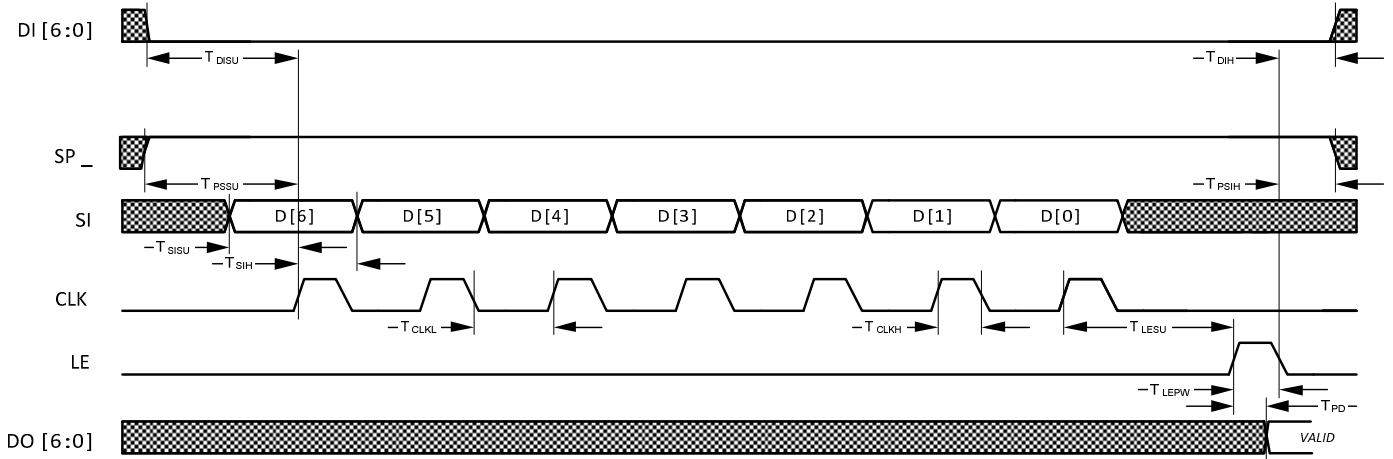
The serial-addressable interface is a 7-bit serial-in, parallel-out shift register buffered by a transparent latch. The 7-bits make up the Attenuation Word, which controls the state of the DSA.

The serial-addressable interface is controlled using three CMOS-compatible signals: Serial-In (SI), Clock (CLK), and Latch Enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in MSB of the Attenuation word first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The serial-addressable timing diagram is illustrated below.

Serial Mode Timing Diagram

 Bits can either be set to logic high or logic low



Symbol	Parameter	Limits		Units
		Min	Max	
$F_{CLK}$	Serial clock frequency	-	10	MHz
$T_{CLKH}$	Serial clock HIGH time	30	-	ns
$T_{CLKL}$	Serial clock LOW time	30	-	ns
$T_{LESU}$	Last serial clock rising edge setup time to Latch Enable rising edge	10	-	ns
$T_{LEPW}$	Latch Enable min. pulse width	30	-	ns
$T_{SISU}$	Serial data setup time	10	-	ns
$T_{SIH}$	Serial data hold time	10	-	ns
$T_{DISU}$	Parallel data setup time	100	-	ns
$T_{DIH}$	Parallel data hold time	100	-	ns
$T_{PSSU}$	Parallel/Serial setup time	100	-	ns
$T_{PSH}$	Parallel/Serial hold time	100	-	ns
$T_{PD}$	Digital register delay (internal)	-	10	ns

Serial Mode Truth Table (Main Attenuation States)

Serial Attenuation Word							Attenuation Setting
D6 (MSB) (first in)	D5	D4	D3	D2	D1	D0 (LSB) (last in)	
L	L	L	L	L	L	L	0dB (Reference IL)
L	L	L	L	L	L	H	0.25dB
L	L	L	L	L	H	L	0.5dB
L	L	L	L	H	L	L	1dB
L	L	L	H	L	L	L	2dB
L	L	H	L	L	L	L	4dB
L	H	L	L	L	L	L	8dB
H	L	L	L	L	L	L	16dB
H	H	H	H	H	H	H	31.75dB

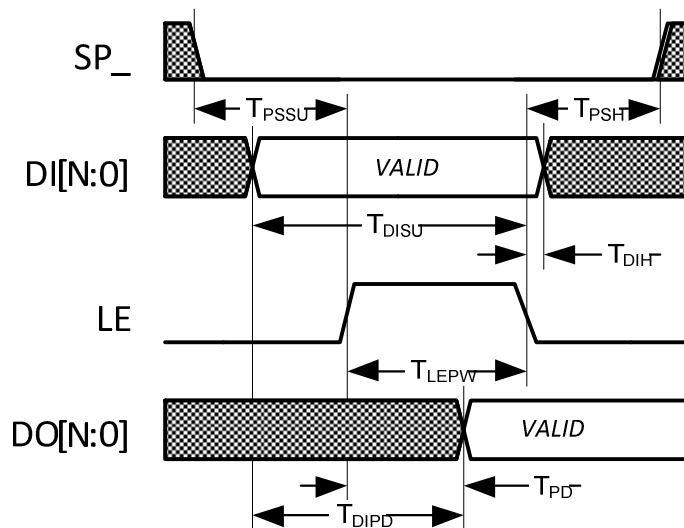
1.10.1.3 *Parallel Mode Interface*

The parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state.

For latched-parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW, to latch a new attenuation state into the device. Data is latched through to the attenuator elements on the rising edge of LE.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will immediately change device state to new attenuation.

Parallel Mode Timing Diagram



Symbol	Parameter	Limits		Units
		Min	Max	
$T_{LEPW}$	Latch Enable minimum pulse width	30	-	ns
$T_{DISU}$	Parallel data setup time	100	-	ns
$T_{DIH}$	Parallel data hold time	100	-	ns
$T_{PSSU}$	Parallel/Serial setup time	100	-	ns
$T_{PSIH}$	Parallel/Serial hold time	100	-	ns
$T_{PD}$	Digital register delay (internal)	-	10	ns
$T_{DIPD}$	Digital register delay (internal, direct mode only)	-	5	ns

Parallel Mode Truth Table (Main States)

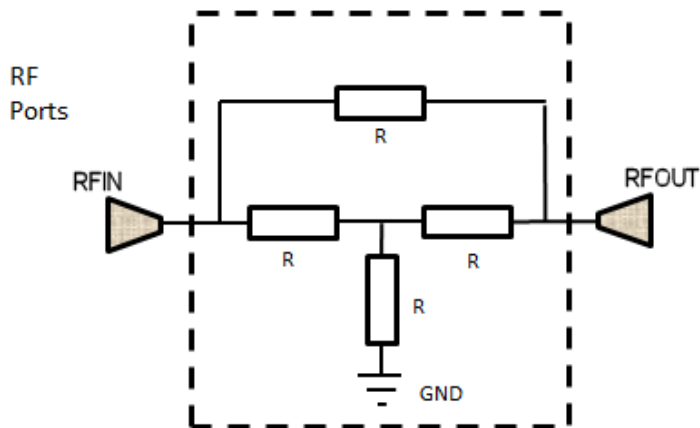
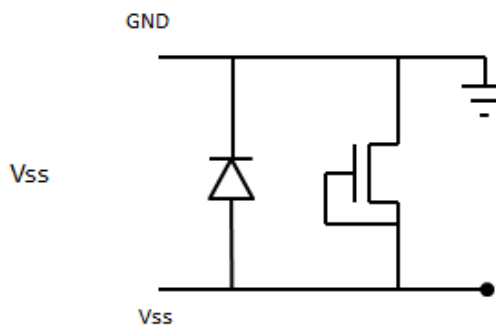
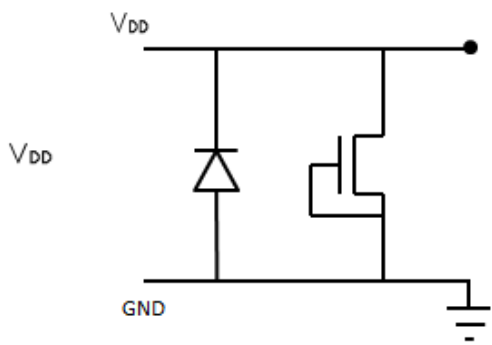
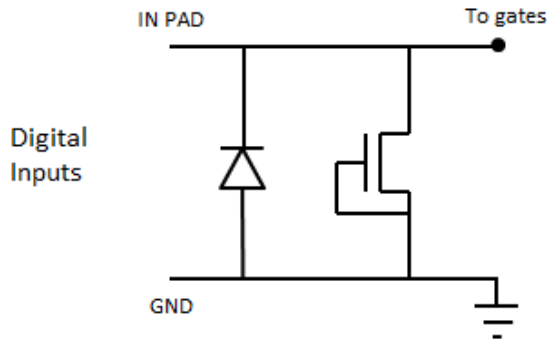
Parallel Attenuation Word							Attenuation Setting
D6 (MSB)	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	0dB (Reference IL)
L	L	L	L	L	L	H	0.25dB
L	L	L	L	L	H	L	0.5dB
L	L	L	L	H	L	L	1dB
L	L	L	H	L	L	L	2dB
L	L	H	L	L	L	L	4dB
L	H	L	L	L	L	L	8dB
H	L	L	L	L	L	L	16dB
H	H	H	H	H	H	H	31.75dB

**1.10.1.4 Reset Control**

While the RESET pin is held HIGH, the DSA will be held at the maximum attenuation setting (31.75dB). For both the serial-addressable and latched-parallel modes of operation the device will remain in this state until the RESET pin is returned LOW.

In direct-parallel mode, the DSA can be preset to any state within the maximum attenuation range by pre-setting the parallel control pins prior to power-up and tying the LE pin HIGH.

1.11 INPUT AND OUTPUT PROTECTION NETWORKS



**2 REQUIREMENTS**

**2.1 GENERAL**

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification.

**2.1.1 Deviations from the Generic Specification**

**2.1.1.1 Deviations from Screening Tests - Chart F3**

High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB Burn-in shall be omitted.

**2.2 MARKING**

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.

**2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES**

Electrical measurements shall be performed at room, high and low temperatures.

**2.3.1 Room Temperature Electrical Measurements**

Electrical measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

**DC CHARACTERISTICS**

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Continuity Check – $V_{DD}$	$V_{SH}$	-	$V_{DD} = V_{SS} = 0V$ $I_{IN} = -200\mu A$	-900	-600	mV
Continuity Check – $V_{SS}$	$V_{SH}$	-	$V_{DD} = V_{SS} = 0V$ $I_{IN} = -200\mu A$	500	900	mV
Continuity Check – Digital Inputs	$V_{SH}$	-	$V_{DD} = V_{SS} = 0V$ $I_{IN} = -200\mu A$	-900	-600	mV
Continuity Check – Analogue Input and Output	$V_{SH}$	-	$V_{DD} = V_{SS} = 0V$ $I_{IN} = -10mA$	-1.1	-0.3	V
Positive Supply Current with No Attenuation	$I_{DD0dB}$	3005	Serial Mode, 0dB Attenuation	-	1	mA
Negative Supply Current with No Attenuation	$I_{SS0dB}$	3005	Serial Mode, 0dB Attenuation	-	10	mA
Functional Test 1 - Nominal Clock Duration	-	3014	CLKH = CLKL = 50ns, f = 10MHz Note 2	Go/NoGo		-
Functional Test 2 – Clock HIGH Duration	-	3014	CLKH = 30ns, CLKL = 70ns, f = 10MHz Note 2	Go/NoGo		-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 3 – Clock LOW Duration	-	3014	CLKH = 70ns, CLKL = 30ns, f = 10MHz Note 2	Go/NoGo		-
Input Voltage - HIGH Level – Digital Inputs	V <sub>IL</sub>	-	RFIN = 400mV	800	-	mV
Input Voltage - HIGH Level – Digital Inputs	V <sub>IH</sub>	-	RFIN = 400mV	-	1.9	V
Output Voltage - Attenuation: 0.25dB	V <sub>RFOUT0.25dB</sub>	-	0.25dB Attenuation, RFIN = 400mV	382	392	mV
Output Voltage - Attenuation: 0.5dB	V <sub>RFOUT0.5dB</sub>	-	0.5dB Attenuation, RFIN = 400mV	370	385	mV
Output Voltage - Attenuation: 1dB	V <sub>RFOUT1dB</sub>	-	1dB Attenuation, RFIN = 400mV	344	366	mV
Output Voltage - Attenuation: 2dB	V <sub>RFOUT2dB</sub>	-	2dB Attenuation, RFIN = 400mV	290	315	mV
Output Voltage - Attenuation: 4dB	V <sub>RFOUT4dB</sub>	-	4dB Attenuation, RFIN = 400mV	219	250	mV
Output Voltage - Attenuation: 8dB	V <sub>RFOUT8dB</sub>	-	8dB Attenuation, RFIN = 400mV	132	162	mV
Output Voltage - Attenuation: 16dB	V <sub>RFOUT16dB</sub>	-	16dB Attenuation, RFIN = 400mV	52	69	mV
Input Leakage Current, LOW Level – Digital Inputs	I <sub>IL</sub>	3009	V <sub>IN</sub> (Under Test) = 0V V <sub>IN</sub> (Remaining Inputs) = V <sub>DD</sub>	-1	1	nA
Input Leakage Current, HIGH Level – Digital Inputs	I <sub>IH</sub>	3010	V <sub>IN</sub> (Under Test) = V <sub>DD</sub> V <sub>IN</sub> (Remaining Inputs) = 0V	0	100	nA

RF CHARACTERISTICS

Switching Time – Min to Max Attenuation	t <sub>on</sub>	-	R <sub>Fin</sub> = +10dBm, f = 1GHz LE = V <sub>DD</sub> /2 to 10% R <sub>Fin</sub> max	240	2700	ns
Switching Time – Max to Min Attenuation	t <sub>off</sub>	-	R <sub>Fin</sub> = +10dBm, f = 1GHz LE = V <sub>DD</sub> /2 to 90% R <sub>Fin</sub> max	40	250	ns
Output Rise Time – Max to Min Attenuation	t <sub>rise</sub>	-	R <sub>Fin</sub> = +10dBm, f = 1GHz 10% to 90% R <sub>Fin</sub> max	80	2200	ns
Output Fall Time – Min to Max Attenuation	t <sub>fall</sub>	-	R <sub>Fin</sub> = +10dBm, f = 1GHz 90% to 10% R <sub>Fin</sub> max	40	550	ns
Insertion Loss (at 10MHz) (S-parameter: S21)	IL <sub>10M</sub>	-	P <sub>in</sub> = +10dBm, f = 10MHz	0.5	2.1	dB
Insertion Loss (at 1GHz) (S-parameter: S21)	IL <sub>1000M</sub>	-	P <sub>in</sub> = +10dBm, f = 1GHz	0.5	3.3	dB
Insertion Loss (at 2GHz) (S-parameter: S21)	IL <sub>2000M</sub>	-	P <sub>in</sub> = +10dBm, f = 2GHz	0.5	3.3	dB
Insertion Loss (at 3GHz) (S-parameter: S21)	IL <sub>3000M</sub>	-	P <sub>in</sub> = +10dBm, f = 3GHz	0.5	3.3	dB
Gain Compression at Maximum P <sub>in</sub> (S-parameter: delta S21)	P <sub>out</sub>		0dB Attenuation, f = 2GHz P <sub>in</sub> = +0dBm and +23dBm	24	28.5	dB



Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Monotonicity Error - Attenuation: 4dB	ME <sub>4dB</sub>	-	4dB Attenuation, f = 2.2GHz P <sub>in</sub> = +10dBm	-0.5	0.5	dB
Monotonicity Error - Attenuation: 8dB	ME <sub>8dB</sub>	-	8dB Attenuation, f = 2.2GHz P <sub>in</sub> = +10dBm	-0.5	0.5	dB
Input Return Loss (at 10MHz) (S-parameter: S11)	IRL <sub>10M</sub>	-	P <sub>in</sub> = +10dBm, f = 10MHz	-60	-13.5	dB
Input Return Loss (at 1GHz) (S-parameter: S11)	IRL <sub>1000M</sub>	-	P <sub>in</sub> = +10dBm, f = 1GHz	-60	-6.5	dB
Input Return Loss (at 2GHz) (S-parameter: S11)	IRL <sub>2000M</sub>	-	P <sub>in</sub> = +10dBm, f = 2GHz	-60	-6.5	dB
Input Return Loss (at 3GHz) (S-parameter: S11)	IRL <sub>3000M</sub>	-	P <sub>in</sub> = +10dBm, f = 3GHz	-60	-6.5	dB
Output Return Loss (at 10MHz) (S-parameter: S22)	ORL <sub>10M</sub>	-	P <sub>in</sub> = +10dBm, f = 10MHz	-60	-13.5	dB
Output Return Loss (at 1GHz) (S-parameter: S22)	ORL <sub>1000M</sub>	-	P <sub>in</sub> = +10dBm, f = 1GHz	-60	-6.5	dB
Output Return Loss (at 2GHz) (S-parameter: S22)	ORL <sub>2000M</sub>	-	P <sub>in</sub> = +10dBm, f = 2GHz	-60	-6.5	dB
Output Return Loss (at 3GHz) (S-parameter: S22)	ORL <sub>3000M</sub>	-	P <sub>in</sub> = +10dBm, f = 3GHz	-60	-6.5	dB
Third Order Intercept Point – Attenuation: 0dB	IIP3 <sub>0dB</sub>	-	0dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Third Order Intercept Point – Attenuation: 0.25dB	IIP3 <sub>0.25dB</sub>	-	0.25dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Third Order Intercept Point – Attenuation: 0.5dB	IIP3 <sub>0.5dB</sub>	-	0.5dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Third Order Intercept Point – Attenuation: 1dB	IIP3 <sub>1dB</sub>	-	1dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Third Order Intercept Point – Attenuation: 2dB	IIP3 <sub>2dB</sub>	-	2dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Third Order Intercept Point – Attenuation: 4dB	IIP3 <sub>4dB</sub>	-	4dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Third Order Intercept Point – Attenuation: 8dB	IIP3 <sub>8dB</sub>	-	8dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Third Order Intercept Point – Attenuation: 16dB	IIP3 <sub>16dB</sub>	-	16dB Attenuation, P <sub>in</sub> = +18dBm f1 = 895MHz & f2 = 905MHz	45	75	dB
Attenuation Error (at 10MHz) - Attenuation: 0dB	AE0dB <sub>10M</sub>	-	0dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.5	0.5	dB
Attenuation Error (at 1GHz) - Attenuation: 0dB	AE0dB <sub>1000M</sub>	-	0dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-0.5	0.5	dB
Attenuation Error (at 2GHz) - Attenuation: 0dB	AE0dB <sub>2000M</sub>	-	0dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-0.5	0.5	dB
Attenuation Error (at 3GHz) - Attenuation: 0dB	AE0dB <sub>3000M</sub>	-	0dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-0.5	0.5	dB
Attenuation Error (at 4GHz) - Attenuation: 0dB	AE0dB <sub>4000M</sub>	-	0dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-0.5	0.5	dB

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Attenuation Error (at 6GHz) - Attenuation: 0dB	AE0dB <sub>6000M</sub>	-	0dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-0.5	0.5	dB
Attenuation Error (at 10MHz) - Attenuation: 0.25dB	AE0.25dB <sub>10M</sub>	-	0.25dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.5	0.5	dB
Attenuation Error (at 1GHz) - Attenuation: 0.25dB	AE0.25dB <sub>1000M</sub>	-	0.25dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-0.5	0.5	dB
Attenuation Error (at 2GHz) - Attenuation: 0.25dB	AE0.25dB <sub>2000M</sub>	-	0.25dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-0.5	0.5	dB
Attenuation Error (at 3GHz) - Attenuation: 0.25dB	AE0.25dB <sub>3000M</sub>	-	0.25dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-0.5	0.5	dB
Attenuation Error (at 4GHz) - Attenuation: 0.25dB	AE0.25dB <sub>4000M</sub>	-	0.25dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-0.5	0.5	dB
Attenuation Error (at 6GHz) - Attenuation: 0.25dB	AE0.25dB <sub>6000M</sub>	-	0.25dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-0.5	0.5	dB
Attenuation Error (at 10MHz) - Attenuation: 0.5dB	AE0.5dB <sub>10M</sub>	-	0.5dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.5	0.5	dB
Attenuation Error (at 1GHz) - Attenuation: 0.5dB	AE0.5dB <sub>1000M</sub>	-	0.5dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-0.5	0.5	dB
Attenuation Error (at 2GHz) - Attenuation: 0.5dB	AE0.5dB <sub>2000M</sub>	-	0.5dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-0.5	0.5	dB
Attenuation Error (at 3GHz) - Attenuation: 0.5dB	AE0.5dB <sub>3000M</sub>	-	0.5dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-0.5	0.5	dB
Attenuation Error (at 4GHz) - Attenuation: 0.5dB	AE0.5dB <sub>4000M</sub>	-	0.5dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-0.5	0.5	dB
Attenuation Error (at 6GHz) - Attenuation: 0.5dB	AE0.5dB <sub>6000M</sub>	-	0.5dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-0.5	0.5	dB
Attenuation Error (at 10MHz) - Attenuation: 1dB	AE1dB <sub>10M</sub>	-	1dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.5	0.5	dB
Attenuation Error (at 1GHz) - Attenuation: 1dB	AE1dB <sub>1000M</sub>	-	1dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-0.5	0.5	dB
Attenuation Error (at 2GHz) - Attenuation: 1dB	AE1dB <sub>2000M</sub>	-	1dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-0.5	0.5	dB
Attenuation Error (at 3GHz) - Attenuation: 1dB	AE1dB <sub>3000M</sub>	-	1dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-0.5	0.7	dB
Attenuation Error (at 4GHz) - Attenuation: 1dB	AE1dB <sub>4000M</sub>	-	1dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-0.8	0.7	dB
Attenuation Error (at 6GHz) - Attenuation: 1dB	AE1dB <sub>6000M</sub>	-	1dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-1.3	0.9	dB
Attenuation Error (at 10MHz) - Attenuation: 2dB	AE2dB <sub>10M</sub>	-	2dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.5	0.5	dB
Attenuation Error (at 1GHz) - Attenuation: 2dB	AE2dB <sub>1000M</sub>	-	2dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-0.5	0.5	dB
Attenuation Error (at 2GHz) - Attenuation: 2dB	AE2dB <sub>2000M</sub>	-	2dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-0.5	0.5	dB
Attenuation Error (at 3GHz) - Attenuation: 2dB	AE2dB <sub>3000M</sub>	-	2dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-0.7	0.7	dB

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Attenuation Error (at 4GHz) - Attenuation: 2dB	AE2dB <sub>4000M</sub>	-	2dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-1.8	0.7	dB
Attenuation Error (at 6GHz) - Attenuation: 2dB	AE2dB <sub>6000M</sub>	-	2dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-1.8	1.5	dB
Attenuation Error (at 10MHz) - Attenuation: 4dB	AE4dB <sub>10M</sub>	-	4dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.5	0.5	dB
Attenuation Error (at 1GHz) - Attenuation: 4dB	AE4dB <sub>1000M</sub>	-	4dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-0.6	0.5	dB
Attenuation Error (at 2GHz) - Attenuation: 4dB	AE4dB <sub>2000M</sub>	-	4dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-0.8	0.5	dB
Attenuation Error (at 3GHz) - Attenuation: 4dB	AE4dB <sub>3000M</sub>	-	4dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-1.2	0.5	dB
Attenuation Error (at 4GHz) - Attenuation: 4dB	AE4dB <sub>4000M</sub>	-	4dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-2.8	0.5	dB
Attenuation Error (at 6GHz) - Attenuation: 4dB	AE4dB <sub>6000M</sub>	-	4dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-3.2	1.5	dB
Attenuation Error (at 10MHz) - Attenuation: 8dB	AE8dB <sub>10M</sub>	-	8dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.5	0.7	dB
Attenuation Error (at 1GHz) - Attenuation: 8dB	AE8dB <sub>1000M</sub>	-	8dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-0.8	0.9	dB
Attenuation Error (at 2GHz) - Attenuation: 8dB	AE8dB <sub>2000M</sub>	-	8dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-1.1	0.8	dB
Attenuation Error (at 3GHz) - Attenuation: 8dB	AE8dB <sub>3000M</sub>	-	8dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-1.7	0.8	dB
Attenuation Error (at 4GHz) - Attenuation: 8dB	AE8dB <sub>4000M</sub>	-	8dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-4.5	0.8	dB
Attenuation Error (at 6GHz) - Attenuation: 8dB	AE8dB <sub>6000M</sub>	-	8dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-6	1.8	dB
Attenuation Error (at 10MHz) - Attenuation: 16dB	AE16dB <sub>10M</sub>	-	16dB Attenuation, P <sub>in</sub> = +10dBm f = 10MHz	-0.6	1.1	dB
Attenuation Error (at 1GHz) - Attenuation: 16dB	AE16dB <sub>1000M</sub>	-	16dB Attenuation, P <sub>in</sub> = +10dBm f = 1GHz	-1.2	1.4	dB
Attenuation Error (at 2GHz) - Attenuation: 16dB	AE16dB <sub>2000M</sub>	-	16dB Attenuation, P <sub>in</sub> = +10dBm f = 2GHz	-1.4	1.4	dB
Attenuation Error (at 3GHz) - Attenuation: 16dB	AE16dB <sub>3000M</sub>	-	16dB Attenuation, P <sub>in</sub> = +10dBm f = 3GHz	-1.5	1.4	dB
Attenuation Error (at 4GHz) - Attenuation: 16dB	AE16dB <sub>4000M</sub>	-	16dB Attenuation, P <sub>in</sub> = +10dBm f = 4GHz	-4	1.4	dB
Attenuation Error (at 6GHz) - Attenuation: 16dB	AE16dB <sub>6000M</sub>	-	16dB Attenuation, P <sub>in</sub> = +10dBm f = 6GHz	-4	6	dB
Attenuation Error (at 10MHz) - Attenuation: Max (31.75dB)	AEMaxdB <sub>10M</sub>	-	Max (31.75dB) Attenuation, P <sub>in</sub> = +10dBm, f = 10MHz	-1.2	2.2	dB
Attenuation Error (at 20MHz) - Attenuation: Max (31.75dB)	AEMaxdB <sub>20M</sub>	-	Max (31.75dB) Attenuation, P <sub>in</sub> = +10dBm, f = 10MHz	-1.2	2.2	dB
Attenuation Error (at 500MHz) - Attenuation: Max (31.75dB)	AEMaxdB <sub>500M</sub>	-	Max (31.75dB) Attenuation, P <sub>in</sub> = +10dBm, f = 10MHz	-1.2	2.2	dB

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Attenuation Error (at 1GHz) - Attenuation: Max (31.75dB)	AEMaxdB <sub>1000M</sub>	-	Max (31.75dB) Attenuation, P <sub>in</sub> = +10dBm, f = 1GHz	-1.5	2.5	dB
Attenuation Error (at 2GHz) - Attenuation: Max (31.75dB)	AEMaxdB <sub>2000M</sub>	-	Max (31.75dB) Attenuation, P <sub>in</sub> = +10dBm, f = 2GHz	-1.5	2.5	dB
Attenuation Error (at 3GHz) - Attenuation: Max (31.75dB)	AEMaxdB <sub>3000M</sub>	-	Max (31.75dB) Attenuation, P <sub>in</sub> = +10dBm, f = 3GHz	-1.5	3.3	dB
Attenuation Error (at 4GHz) - Attenuation: Max (31.75dB)	AEMaxdB <sub>4000M</sub>	-	Max (31.75dB) Attenuation, P <sub>in</sub> = +10dBm, f = 4GHz	-1.5	3.8	dB

**NOTES:**

1. Unless otherwise specified:

- Each characteristic shall be tested for both V<sub>DD</sub> = 2.7V, V<sub>SS</sub> = -2.7V and V<sub>DD</sub> = 3.6V, V<sub>SS</sub> = -3.3V.
- All inputs and outputs shall be tested for each characteristic (as applicable).
- Digital input conditions shall be V<sub>IH</sub> = V<sub>DD</sub>, V<sub>IL</sub> = 0V.
- Inputs not under test shall be V<sub>IN</sub> = V<sub>SS</sub> or V<sub>DD</sub> and outputs not under test shall be open.

2. Functional testing shall be performed using suitable test patterns to verify correct function per truth table and timing diagram requirements.

2.3.2 High and Low Temperatures Electrical Measurements

Electrical measurements shall be performed at T<sub>amb</sub> = +85 (+0 -5)°C and T<sub>amb</sub> = -40 (+5 -0)°C

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T<sub>amb</sub> = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units	
		Drift Value Δ	Absolute		
			Min		Max
Output Voltage - Attenuation: 2dB	V <sub>RFOUT2dB</sub>	±2%	290	315	mV
Output Voltage - Attenuation: 4dB	V <sub>RFOUT4dB</sub>	±3%	219	250	mV
Output Voltage - Attenuation: 8dB	V <sub>RFOUT8dB</sub>	±5%	132	162	mV

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}\text{C}$ .

The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

In addition, the drift values ( $\Delta$ ) for the following characteristics shall not be exceeded:

Characteristics	Symbols	Drift Value $\Delta$	Units
Output Voltage - Attenuation: 2dB	$V_{RFOUT2dB}$	$\pm 2\%$	mV
Output Voltage - Attenuation: 4dB	$V_{RFOUT4dB}$	$\pm 3\%$	mV
Output Voltage - Attenuation: 8dB	$V_{RFOUT8dB}$	$\pm 5\%$	mV

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units	Notes
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	$^{\circ}\text{C}$	
Positive Supply Voltage (VDD)	$V_{DD}$	+3.3 (+0 -5 %)	V	
Negative Supply Voltage (VSS)	$V_{SS}$	-2.7 (+0 -5 %)	V	
Analogue Input (RFIN)	$P_{in}$	10MHz sine wave, $V_{CM} = 0V, V_{pp} = 3.0V$	-	1
Analogue Output Load (RFOUT)	$R_L$	High Impedance	-	
Digital Inputs (SP, RESET, LE, SI, CLK, Dn)	$V_{IN}$	0 or $V_{DD}$	V	2
Vector Length	$t_O$	1	$\mu\text{s}$	2

**NOTES:**

1. The RF input signal shall be fed through a suitable series capacitor.

2. The device shall be burned-in using 'functional' vectors that are looping indefinitely in order to exercise the DUT through various attenuation states in both parallel and serial modes. There shall be 10 different vectors in each sequence with a vector length as specified, as follows:

Vector Number	Series/Parallel Mode	Attenuation Word	Comment
1	Parallel	0000000	Attenuation: 0db
2	Parallel	1010101	Attenuation: 21.25dB
3	Parallel	1111111	Attenuation: Max (31.75dB)
4	Parallel	0101010	Attenuation: 10.5dB
5	Parallel	0000000	Attenuation: 0db
6	Serial	0000000	Attenuation: 0db
7	Serial	1010101	Attenuation: 21.25dB
8	Serial	1111111	Attenuation: Max (31.75dB)
9	Serial	0101010	Attenuation: 10.5dB
10	Serial	0000000	Attenuation: 0db

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Components shall be biased in both ON and OFF configurations as detailed below. The required test samples shall be divided equally between both bias configurations.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Bias conditions:

- OFF Configuration Continuous Bias Conditions: All terminals shall be connected to ground with  $T_{amb} = +22 \pm 3^{\circ}\text{C}$ .
- ON Configuration Continuous Bias Conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+22 ±3	°C
Positive Supply Voltage (VDD)	$V_{DD}$	+3.3 (+0 -5 %)	V
Negative Supply Voltage (VSS)	$V_{SS}$	-3.0 (+0 -5 %)	V
Analogue Input (RFIN)	$P_{in}$	+10dBm minimum, $f \geq 10\text{MHz}$	-
Analogue Output Load (RFOUT)	$R_L$	50	$\Omega$
Digital Input : D5 (Attenuation: 8dB)	$V_{IN}$	$V_{DD}$	V
Digital Inputs : SP, RESET, LE, SI, CLK, D0, D1, D2, D3, D4, D6	$V_{IN}$	0	V

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Electrical Measurements at Room temperature.

The parameters to be measured during and on completion of irradiation testing are shown below.

DC CHARACTERISTICS

Characteristics	Symbols	Limits		Units
		Min	Max	
Positive Supply Current with No Attenuation	$I_{DD0dB}$	-	1	mA
Negative Supply Current with No Attenuation	$I_{SS0dB}$	-	10	mA

RF CHARACTERISTICS

Insertion Loss (at 10MHz) (S-parameter: S21) Note 1	$IL_{10M}$	0.5	2.1	dB
Insertion Loss (at 1GHz) (S-parameter: S21) Note 1	$IL_{1000M}$	0.5	3.3	dB
Insertion Loss (at 2GHz) (S-parameter: S21) Note 1	$IL_{2000M}$	0.5	3.3	dB
Insertion Loss (at 3GHz) (S-parameter: S21) Note 1	$IL_{3000M}$	0.5	3.3	dB

**NOTES:**

1. S-parameter characteristics shall only be measured on completion of irradiation testing.

**APPENDIX 'A'**  
**AGREED DEVIATIONS FOR PEREGRINE SEMICONDUCTOR EUROPE (GB)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Screening Tests – Chart F3	Following PIND, additional Seal (Fine and Gross Leak) and External Visual Inspection may also be performed.
	Initial High and Low Temperatures Electrical Measurements may also be performed prior to Burn-in.
Deviations from Screening Tests – Chart F3 & Para. 7.1.1	<p>For components that form part of the delivery lot, lead crop and form may be performed at any point prior to final Seal.</p> <p>Measurement of characteristics in the RF Characteristics section of either Room Temperature Electrical Measurements or High and Low Temperatures Electrical Measurements, may be performed separately from the DC Characteristics, subsequent to lead crop and form.</p> <p>Selection of components to be subjected to Qualification and Periodic Tests may be performed prior to the completion of Screening Tests.</p> <p>For components that will be subjected to Qualification and Periodic Tests, lead crop and form may not be performed during Screening Tests. Accordingly, characteristics in the RF Characteristics section of either Room Temperature Electrical Measurements or High and Low Temperatures Electrical Measurements, may not be measured during Screening Tests.</p>
Deviations from Screening Tests – Chart F3 & Paras. 6.2.3 & 6.4.1	Any failures that occur during measurement of characteristics in the RF Characteristics section of either Room Temperature Electrical Measurements or High and Low Temperatures Electrical Measurements, may not be counted as parameter limit failures during Check for Lot Failure.
Deviations from Screening Tests – Chart F3 & Para. 9.7	<p>Radiographic Inspection shall be performed in accordance with ESCC Basic Specification No. 20900. The Manufacturer may perform the inspection at any point during Screening Tests subsequent to Serialisation and prior to final Seal.</p> <p>Radiographic Inspection photographic results shall be recorded against component serial number and included in the data documentation package.</p>
Deviations from Qualification and Periodic Tests – Chart F4 & Para. 7.6.2	<p>Lead crop and form may be performed at any point during Qualification and Periodic Tests.</p> <p>Measurement of characteristics in the RF Characteristics section of Intermediate and End-Point Electrical Measurements may be performed separately from the DC Characteristics, subsequent to lead crop and form. Any failures of RF Characteristics may not be counted as electrical failures when determining lot failure.</p>
	Permanence of Marking may not be performed on devices which have been laser marked.