EVALUATION TEST PROGRAMME FOR

MONOLITHIC INTEGRATED CIRCUITS

ESCC Basic Specification No. 2269000

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1 PURPOSE

The purpose of this specification is to establish the procedure to be followed in the evaluation of component capabilities as required for space applications and thereby to anticipate, as far as possible, component behaviour during qualification testing. Therefore, the aim of such testing shall be to overstress specific characteristics of the component concerned with a view to the detection of possible failure modes. Additionally, a detailed destructive physical analysis shall be performed to detect any design and construction defects which may affect the reliability of the component and to facilitate failure analysis activities. The evaluation shall also include a check of the susceptibility of the component to ESD damage.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification.

2.1 ESCC SPECIFICATIONS

No. 9000, Integrated Circuits, Monolithic.

No. 20400, Internal Visual Inspection.

No. 20500, External Visual Inspection.

No. 20900, Radiographic Inspection.

No. 22900, Total Dose Steady-State Irradiation Test Method.

No. 23800, Electrostatic Discharge Sensitivity Test Method.

Unless otherwise stated herein, reference within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

IEC Publication No. 68, Basic Environmental Testing Procedures.

IEC Publication No. 747, Semiconductor Devices: Discrete Devices and Integrated Circuits.

MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

MIL-STD-883, Test Methods and Procedures for Microelectronics.

ESA PSS-01-702, A Thermal Vacuum Test for the Screening of Space Materials.

3 PROCEDURE

Standard components shall be selected from a homogeneous lot at the Manufacturer to be evaluated. These components shall not have been submitted to any screening or burn-in, but must have been manufactured in conformity with high reliability practice and an established Process Identification Document (PID) or an identifiable process which shall form the basis for the PID.

The tests specified in the programme shall be performed in the sequence shown in Chart I. All results shall be recorded and failed components submitted to a failure analysis. Probable failure modes and mechanisms shall be determined.

The evaluation test programme shall be performed, under the supervision of the ESCC Executive, by the Manufacturer or at a test laboratory approved by the ESCC Executive.

4 TEST PROGRAMME SEQUENCE AND SAMPLE DISTRIBUTION

4.1 SELECTION OF COMPONENTS FOR EVALUATION TESTING

The number of components to be selected for evaluation testing shall depend on whether a single component type or a family of parts is evaluated and the number of component types chosen to represent the family.

Not less than 103 specimens shall be used for each test programme.

The component types chosen to represent a family shall cover the range of components to be evaluated and be representative of the different package and pin configurations under consideration. They shall also be the most suitable for highlighting those characteristics and parameters that are pertinent to an investigation into failure modes and weaknesses.

The samples shall be as specified by, or as agreed with, the ESCC Executive.

The above mentioned quantity shall be submitted to the full evaluation procedure whenever a new technology has been applied to the components concerned, where there is insufficient experience in their production.

4.2 DETAIL SPECIFICATIONS

Should a Detail Specification for the device(s) to be evaluated not exist, the Manufacturer shall prepare such a document(s) in accordance with the established ESCC format and submit it to the ESCC Executive for provisional approval. This shall then serve as a basis for the ordering and testing of the relevant components.

4.3 INSPECTION RIGHTS

The ESCC Executive reserves the right to inspect at any time the components processed for evaluation purposes. The Manufacturer shall notify the ESCC Executive at least three working days in advance of the date of internal visual inspection (but see Para. 4.4).

4.4 CONTROL DURING FABRICATION

The components shall be produced as defined in Para. 3 of this specification. Internal visual inspections shall be performed on the lot to be tested to the extent that this forms part of the Manufacturer's standard procedures. Progress of the components shall be observed closely and recorded together with an analysis of any reject. A chart showing the numbers in/out and failure cause for each fabrication stage shall be submitted to the ESCC Executive.

5 INSPECTION

5.1 GENERAL

The components shall be checked to verify their suitability for the Evaluation Test Programme. Defects or deviations from the established ESCC requirements may invalidate the evaluation. For each measurement or inspection performed, the results shall be summarised in terms of quantity tested, quantity passed and quantity rejected. If devices are rejected, the reason shall be clearly identified.

5.2 DIMENSIONS (100%)

All devices shall be inspected in accordance with Figure 2 of the Detail Specification (go-no-go). Where gauges exist for performance of measurements, these may be used. For packages with a high pin count, the measurements may be performed using a sampling scheme which shall be approved by the ESCC Executive. Rejected components shall be replaced.

5.3 WEIGHT (100%)

All devices shall be weighed. Any devices that exceed the weight defined in the Detail Specification shall be rejected and replaced.

5.4 ELECTRICAL MEASUREMENTS (100%)

These measurements shall be performed in accordance with Table 2 of the Detail Specification at an ambient temperature of +22 ±3°C (go-no-go). Rejected components shall be replaced.

5.5 EXTERNAL VISUAL INSPECTION (100%)

All devices shall be inspected in accordance with ESCC Basic Specification No. 20500. Rejected components shall be replaced.

5.6 PARTICLE IMPACT NOISE DETECTION (PIND) (100%)

All devices shall be tested in accordance with the requirements of ESCC Generic Specification No. 9000, Para. 9.7. Rejected components shall be replaced.

5.7 RADIOGRAPHIC INSPECTION (100%)

All devices shall be inspected in accordance with ESCC Basic Specification No. 20900. Additional axes to those specified in the relevant ancillary specification of ESCC Basic Specification No. 20900 may be radiographed if, by so doing, it is possible to observe any faults. Rejected components shall be replaced.

5.8 HERMETICITY (100%)

Fine and gross leak tests shall be performed on all components in accordance with the requirements of ESCC Generic Specification No. 9000, Para. 9.8. Rejected components shall be replaced.

5.9 MARKING AND SERIALISATION (100%)

All components shall be marked and serialised in accordance with the standard procedures of the Manufacturer concerned.

5.10 MATERIALS AND FINISHES

All non-metallic materials and finishes, that are not within a hermetically sealed enclosure, of the components specified herein shall be tested in accordance with ESA PSS-01-702 to verify its outgassing requirements, unless relevant data is available.

5.11 COMPLETION OF INSPECTION

The completion of inspection shall result in a batch of components that have been verified as to their suitability for the Evaluation Test Programme, i.e. each component has satisfied the requirements of Paras. 5.2 to 5.10 inclusive.

6 INITIAL ELECTRICAL MEASUREMENTS (100% READ AND RECORD)

These measurements shall be made according to Tables 2 and 3 of the Detail Specification. All characteristics shall be recorded against serial numbers.

7 EVALUATION TEST PROGRAMME

7.1 GENERAL

The evaluation tests shall be performed as specified in Chart I. The components shall be randomly divided into three groups and their associated subgroups in the proportions indicated in Chart I. When a family of components is under investigation, the variations within that family must be represented in each group/subgroup. The Subgroup 2A tests shall be completed and the results analysed before the Subgroup 3B tests are commenced.

All failed components shall be analysed. The depth of analysis shall depend upon the circumstances in which failure occurred and upon whether useful information may be gained. As a minimum, the failure mode shall be determined in each case. Components not failing catastrophically, i.e. those displaying out-of-tolerance electrical parameters, shall not be removed from the test sequence but monitored to observe degradation trends.

7.2 GROUP 1 - CONTROL GROUP

This group shall be retained for comparison purposes. Whenever electrical measurements are made on any devices under test, these devices shall also be measured.

7.3 GROUP 2 - DESTRUCTIVE TESTS

7.3.1 General

This group shall be randomly divided into five subgroups in the proportions indicated in Chart I.

7.3.2 Subgroup 2A - Step-Stress Tests

7.3.2.1 General

This subgroup shall be randomly divided into two further subgroups in the proportions indicated in Chart I. The step-stress sequence shall be terminated when 50% (rounded up) of the specimens have been destroyed, unless practical reasons prevent this.

7.3.2.2 Determination of Thermal Resistance/Conductivity

MIL-STD-883, Method 1012. (A special constructed device or test structure might be necessary for the performance of this test).

7.3.2.3 Parameters to be measured during Step-Stress Tests

During step-stress tests, electrical measurements shall be made in accordance with Table 4 of the Detail Specification. Should Table 4 of the Detail Specification not be established, the parameters to be measured shall be selected from Table 2 of the Detail Specification. In the case of doubt as to the applicability of any Table 2 parameter, the parameter shall be measured. Quiescent current (if applicable) shall be measured in all cases. At the termination of the step-stress sequences, any surviving devices shall have their thermal resistance/conductivity measured as specified in Para. 7.3.2.2.

7.3.2.4 Subgroup 2A(i) - Temperature Step-Stress Test

The tests in this subgroup shall be performed as specified in Chart II. Electrical measurements shall be made as defined in Para. 7.3.2.3 above. The starting temperature (which will be no higher than the maximum operating temperature as defined in the Detail Specification) and the temperature steps (with a maximum step of 25°C) to be employed will be decided by the ESCC Executive.

7.3.2.5 Subgroup 2A(ii) - Power Step-Stress Test

(a) Applicability

This test is only applicable to devices where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(b) Procedure

The tests in this subgroup shall be performed as specified in Chart III. Electrical measurements shall be made as defined in Para. 7.3.2.3 above. The starting power (which will be no higher than the maximum input power as defined in the Detail Specification) and the power steps (with a maximum step of 20%) to be employed will be decided by the ESCC Executive.

7.3.2.6 Analysis of Subgroup 2A

The analysis of Subgroup 2A shall be presented to the ESCC Executive in a graphical form, supported by the actual results, as follows:

- The number of functional failures shall be plotted against each temperature or power level (if applicable) applied. The cumulative failure rate shall also be plotted.
- The parameters (as defined in Para. 7.3.2.3 above) shall be monitored, recorded and plotted against time for each temperature or power level (if applicable) as appropriate.
- The average drift of the parameters at each temperature or power level applied shall be plotted against temperature or power (if applicable) as appropriate.

The analysis of the results of Subgroup 2A(i and ii (if applicable)) shall be used to determine the most effective temperatures and power (if applicable) for the accelerated electrical endurance test (Subgroup 3B).

7.3.3 Subgroup 2B - Radiation Tests

7.3.3.1 Total Dose Steady-State Radiation Test

In accordance with ESCC Basic Specification No. 22900.

7.3.4 Subgroup 2C - Construction Analysis

7.3.4.1 Internal Water Vapour Content

MIL-STD-883, Method 1018, Procedure 1.

7.3.4.2 Opening

The devices shall be opened using a technique which does not contaminate the internal structure or in any way impair the ability to observe defects.

7.3.4.3 Internal Visual Inspection

Each device shall be visually inspected in accordance with ESCC Basic Specification No. 20400. Photographs shall be taken as follows:

(a) An overall photograph of the opened device.
(b) An overall photograph of the die.
(c) Photographs of any anomalies found.

7.3.4.4 Scanning Electron Microscope (SEM) Inspection

This inspection shall include, but shall not necessarily be limited to, examination of the following:

(a) Detailed examination of any anomalies identified by the internal visual inspection (Para. 7.3.4.3 above). Photographs shall be taken of the above.

(b) Low magnification (up to 500X) shall be used to assess:
 (i) Clearance of bond wires at the die edge.
 (ii) Quality of bonding at the die.
 (iii) Quality of bonding at the post.

 Photographs shall be taken of the above.

(c) High magnification (1000x or greater) shall be used to assess:
   (i) Metallisation coverage and consistency at steps.
   (ii) Metallisation coverage at contact windows, bonding pads, etc.

   Photographs shall be taken of the above.

   In the case of devices with a glassivated surface, this examination shall first be attempted through the glassivation.

   If the resolution is inadequate, the glassivation shall be removed. This step must be postponed until the bond strength (Para. 7.3.4.5) test has been performed.

   For devices with multi-level metallisation, the upper layer(s) shall be removed to permit assessment of the above mentioned features. This step shall also be postponed until the bond strength test (Para. 7.3.4.5) has been performed.

7.3.4.5 Bond Strength Test

In accordance with ESCC Generic Specification No. 9000, Para. 9.2.1.

7.3.4.6 Die Shear Test

(a) Precautions
   If it is known, or believed, that beryllium oxide or other toxic substances are used in the construction of the device, precautionary measures shall be employed.
(b) Procedure
   In accordance with ESCC Generic Specification No. 9000, Para. 9.2.2.

7.3.4.7 Microsectioning

(a) Precautions
   As per Para. 7.3.4.6(i) above.
(b) Glassivation Layer Integrity (if applicable)
   MIL-STD-883, Method 2021.
(c) Mounting
   The device(s) shall be mounted on a carrier or in a transparent thermosetting resin. This shall have a curing temperature below the maximum storage temperature of the device(s). The resin shall be evacuated after mixing and after the device has been mounted in the uncured resin.
(d) Microsectioning
   The device(s) shall be ground and polished to achieve a surface finish of at least 0.1 micron. To improve definition and detail, chemical etches shall be used to highlight junction definition, metallographic features, etc. The following, not exhaustive, features shall be assessed:
   (i) Diffusion and oxide characteristics.
   (ii) Metal/semiconductor interfaces.
   (iii) Metal/metal interfaces.
   (iv) Thickness and consistency of layers; particularly insulating layers in devices with multiple layer metallisation.
   (v) Plating thickness and consistency on posts and pins.

   Photographs shall be taken of the above.

7.3.5 <u>Subgroup 2D - Package Tests</u>

7.3.5.1 General

The devices in this subgroup shall be divided between Paras. 7.3.5.2, 7.3.5.3 and 7.3.5.4 in the ratio 4:4:2. Any devices from Paras. 7.3.5.2 or 7.3.5.3 that have not been destroyed shall then be subjected to Para. 7.3.5.4.

7.3.5.2 Thermal Tests

(a) Applicability
These tests must be performed on electrically good devices.

(b) Procedure

(i) Temperature Cycling
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.5 - 100 cycles instead of 10 cycles.

(ii) Seal Test
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.8.

(iii) Electrical Measurements
These measurements shall be made in accordance with Table 2 of the Detail Specification.

(iv) Thermal Shock
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.16 - 100 cycles instead of 10 cycles.

(v) Seal Test
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.8.

(vi) Electrical Measurements
These measurements shall be made in accordance with Table 2 of the Detail Specification.

7.3.5.3 Mechanical Tests

(a) Tests that must be performed on electrically good devices

(i) Shock
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.13 - 50 pulses (per orientation) instead of 5 pulses (per orientation).

(ii) Seal Test
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.8.

(iii) Electrical Measurements
These measurements shall be made in accordance with Table 2 of the Detail Specification.

(iv) Vibration
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.14 - 120 sweeps (total) instead of 12 sweeps (total).

(v) Seal Test
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.8.

(vi) Electrical Measurements
These measurements shall be made in accordance with Table 2 of the Detail Specification.

(b) Tests that can be performed on electrical rejects

(i) Solderability
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.18.

(ii) Permanence of Marking
All devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.19.

(iii) Lid Torque
MIL-STD-883, Method 2024.

7.3.5.4 Resistance to Soldering Heat

(a) Applicability
This test must be performed on electrically good devices.

(b) Procedure
IEC Publication No. 68-2-20 Test 'Tb', Method '1A' with no thermal screen or flux for 10 ±1s, or MIL-STD-750, Method 2031. Following each cycle, electrical measurements shall be performed in accordance with Table 2 (go-no-go) of the Detail Specification and a seal test shall be performed in accordance with Para. 7.3.5.2(iii) above. The test shall be repeated until the device has failed or 5 cycles have been performed whichever is the sooner.

7.3.5.5 Pin To Pin Isolation

(a) Applicability
This test must be performed on empty package(s) that have been through the normal assembly procedures up to sealing.

(b) Procedure
MIL-STD-883, Method 1003.

7.3.6 Subgroup 2E - Electrical Tests

7.3.6.1 General

The components in this subgroup shall be randomly divided between those tests that are performed.

7.3.6.2 Electrostatic Discharge Sensitivity (ESDS) Test

ESD testing shall be performed in accordance with ESCC Basic Specification No. 23800. If the component under examination is not categorised into one of the 3 classes listed, then the component shall be termed "unclassified".

When the evaluation covers a family or series of components, the types selected for this test shall be representative of all protection circuits within this family or series.

7.3.6.3 Characterisation

(a) Safe Operating Area
(i) Applicability
This test is only applicable to devices where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. Additionally, it shall only be applied to integrated circuits that do not have internal output protection circuitry. The ESCC Executive shall review the component type and technology to determine the applicability of the test.
(ii) Procedure
IEC Publication No. 747-7, Para. 11.3.4. The ESCC Executive shall review the component type and technology to determine the test conditions.

(b) Current Limits
The design of each device under investigation shall be examined to ensure that no part of the device carries more than the maximum current defined by the technology or process design rules.

(c) Breakdown Voltage, Input or Output
   (i) Applicability
   This test is only applicable to digital devices.
   (ii) Procedure
   MIL-STD-883, Method 3008 shall be applied to find the limiting value.

(d) Input Interaction
   (i) Applicability
   This test is applicable to digital devices.
   (ii) Digital Devices Procedure
   The truth table shall be applied at the maximum operating frequency under the conditions specified in the truth table.

(e) Verification of Functionality
The functionality of the device shall be explored over varying temperature ranges, levels of supply voltage, etc. The ESCC Executive shall review the component type and technology to determine the exact procedure to be adopted. Data shall be presented, preferably, in a graphical form: Schmoo plots for example.

7.4 GROUP 3 - ENDURANCE TESTS

7.4.1 General

This group shall be randomly divided into 3 subgroups in the proportions indicated in Chart I.

7.4.2 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test

Unless otherwise specified in the Detail Specification, all devices shall be subjected to the test in accordance with ESCC Generic Specification No. 9000, Para. 9.23.

7.4.3 Subgroup 3B - Accelerated Electrical Endurance Test

This group shall be randomly divided into 3 subgroups in the proportions indicated in Chart I. The applicable tests shall not be performed until the subgroup 2A tests have been completed and analysed, and 3 test conditions selected. The tests in this group shall be performed as specified in Chart IV.

The temperatures T_1, T_2 and T_3 shall be chosen such that within approximately 1000, 500 and 168 hours, the parameter(s) defined in Para. 7.3.2.3 above can be expected to have drifted to an extreme of the permitted range. A common applied power (if applicable) also determined from the Subgroup 2A tests, shall be used. If the power step-stress test was not performed, the devices shall be operated at their maximum rated dissipation. Intermediate electrical measurements shall be performed in accordance with Para. 7.3.2.3 above at the following times:

T_1 (1000 hrs)	T_2 (500 hrs)	T_3 (168 hrs)
168 (+24 -0) hrs	168 (+24 -0) hrs	168 (+24 -0) hrs
500 (+24 -0) hrs	500 (+24 -0) hrs	-
168 (+24 -0) hrs	-	-

Failed components shall be removed for analysis as specified in Para. 7.1.

7.4.4 Subgroup 3C - Extended Burn-in Test

The devices shall be tested for 1000 hours at the conditions defined in the Detail Specification for burn-in. Intermediate electrical measurements shall be performed in accordance with Para. 7.3.2.3 above at the following times: 168 (+24 -0) hrs, 500 (+24 -0) hrs and 1000 (+24 -0) hrs. If the

conditions determined for the 1000 hour subgroup in 7.4.3 above are identical to those defined for burn-in, this test shall not be performed.

7.5 GROUP 4 - RESERVE

Should any additional tests be considered necessary, the devices in this subgroup shall be used.

8 DATA DOCUMENTATION

8.1 GENERAL REQUIREMENTS

An evaluation test report shall be established. This shall comprise the following:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Sample identification.
(e) Production data.
(f) Inspection data.
(g) Initial electrical measurements.
(h) Group 1 - Control Group data.
(i) Thermal Resistance/Conductivity data.
(j) Subgroup 2A(i) - Temperature Step-Stress test data.
(k) Subgroup 2A(ii) - Power Step-Stress test data (if applicable).
(l) Subgroup 2B - Radiation tests data.
(m) Subgroup 2C - Construction Analysis data.
(n) Subgroup 2D - Package tests data.
(o) Subgroup 2E - Electrical tests data.
(p) Subgroup 3A - High Temperature Reverse Bias (HTRB) test data (if applicable).
(q) Subgroup 3B - Accelerated Electrical Endurance test data.
(r) Subgroup 3C - Extended Burn-in test data.
(s) Group 4 - Reserve data (if applicable).
(t) Summary of results and conclusions.

Items (a) to (t) inclusive shall be grouped, preferably as subpackages, and for identification purposes, each page shall include the following information:

- Manufacturer's/test house's name.
- Lot identification.
- Date of establishment of the document.
- Page number.

8.2 COVER SHEET(S)

The cover sheet (or sheets) of the evaluation test report shall include as a minimum:

(a) Reference to this document, including issue and date.
(b) Component type and number.
(c) Lot identification.
(d) Manufacturer's/test house's name and address.
(e) Location of the manufacturing plant/test house.
(f) Signature on behalf of the Manufacturer/test house.
(g) Total number of pages of the evaluation test report.

8.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be included in the evaluation test report. Where applicable, this list shall contain the inventory number, Manufacturer type number, serial number, calibration status data, etc. This list shall indicate for which tests such equipment was used.

8.4 LIST OF TEST REFERENCES

This list shall include all references or codes which are necessary to correlate the test data provided with the applicable tests.

8.5 SAMPLE IDENTIFICATION (PARA. 4.1)

This shall identify the criteria used for the selection of the particular components used for the tests, when evaluating a range of components by means of representative samples.

8.6 PRODUCTION DATA (PARA. 4.4)

The progress of the components through the normal manufacturing processes shall be documented. The components failing a particular process shall be detailed, together with the reason for their removal.

8.7 INSPECTION DATA (PARA. 5)

The number of components subjected to each test shall be identified together with the number and reason for any rejects. Radiographs (if applicable) of any failed components shall be presented.

8.8 INITIAL ELECTRICAL MEASUREMENTS (PARA. 6)

All data shall be recorded against serial numbers. A histogram of device parameters shall be produced.

8.9 GROUP 1 - CONTROL GROUP DATA (PARA. 7.2)

All data shall be recorded against serial numbers.

8.10 SUBGROUP 2A - STEP-STRESS TESTS DATA

8.10.1 Thermal Resistance/Conductivity Data (Para. 7.3.2.2)

All data shall be recorded against serial numbers.

8.10.2 Subgroup 2A(i) - Temperature Step-Stress Test Data (Para. 7.3.2.4)

All data shall be recorded against serial numbers. This shall include:

(a) Starting temperature.
(b) Temperature steps.
(c) Electrical measurements tabulated for each step.
(d) Graphical output as defined in Para. 7.3.2.6.
(e) Analysis of any failed components as defined in Para. 7.1.
(f) Thermal resistance/conductivity measurements from surviving devices.

8.10.3 Subgroup 2A(ii) - Power Step-Stress Test Data (Para. 7.3.2.5) (if applicable)
All data shall be recorded against serial numbers. This shall include:

(a) Starting power.
(b) Power steps.
(c) Electrical measurements tabulated for each step.
(d) Graphical output as defined in Para. 7.3.2.6.
(e) Analysis of any failed components as defined in Para. 7.1.
(f) Thermal resistance/conductivity measurements from surviving devices.

8.11 SUBGROUP 2B - RADIATION TESTS DATA (PARA. 7.3.3)

All data shall be recorded against serial numbers. This shall include:

(a) Total dose steady-state test data.

8.12 SUBGROUP 2C - CONSTRUCTION ANALYSIS DATA (PARA. 7.3.4)

All data shall be recorded against serial numbers. This shall include:

(a) Internal water vapour content data.
(b) Photographs.
(c) SEM photographs.
(d) Results of bond strength test.
(e) Results of die shear test.
(f) Glassivation layer integrity test data (if applicable).
(g) Microsectioning photographs.

8.13 SUBGROUP 2D - PACKAGE TESTS DATA (PARA. 7.3.5)

All data shall be recorded against serial numbers. This shall include:

(a) Thermal tests data.
(b) Mechanical tests data.
(c) Resistance to soldering heat test data.
(d) Pin to pin isolation test data.

8.14 SUBGROUP 2E - ELECTRICAL TESTS DATA (PARA. 7.3.6)

All data shall be recorded against serial numbers. This shall include:

(a) ESDS test data.
(b) Characterisation data.

8.15 GROUP 3 - ENDURANCE TESTS DATA

8.15.1 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test Data (Para. 7.4.2) (if applicable)
All data shall be recorded against serial numbers.

8.15.2 Subgroup 3B - Accelerated Electrical Endurance Test Data (Para. 7.4.3)
All data shall be recorded against serial numbers. This shall include:

(a) Temperatures T_1, T_2 and T_3 chosen.
(b) Power chosen (if applicable).
(c) Electrical measurements tabulated and plotted for each intermediate time as defined in Para. 7.4.3.
(d) Drift values referred to the initial electrical measurements (Para. 6).
(e) Analysis of any failed components as defined in Para. 7.1.

8.15.3 Subgroup 3C - Extended Burn-in Test Data (Para. 7.4.4)
All data shall be recorded against serial numbers.

8.16 GROUP 4 - RESERVE DATA (PARA. 7.5) (IF APPLICABLE)

All data shall be recorded against serial numbers.

8.17 SUMMARY OF RESULTS AND CONCLUSIONS

The above shall be briefly reviewed, indicating the success or otherwise of the evaluation test programme. Any production screens that need to be introduced into the PID shall be outlined.

CHART I – EVALUATION TEST PROGRAMME

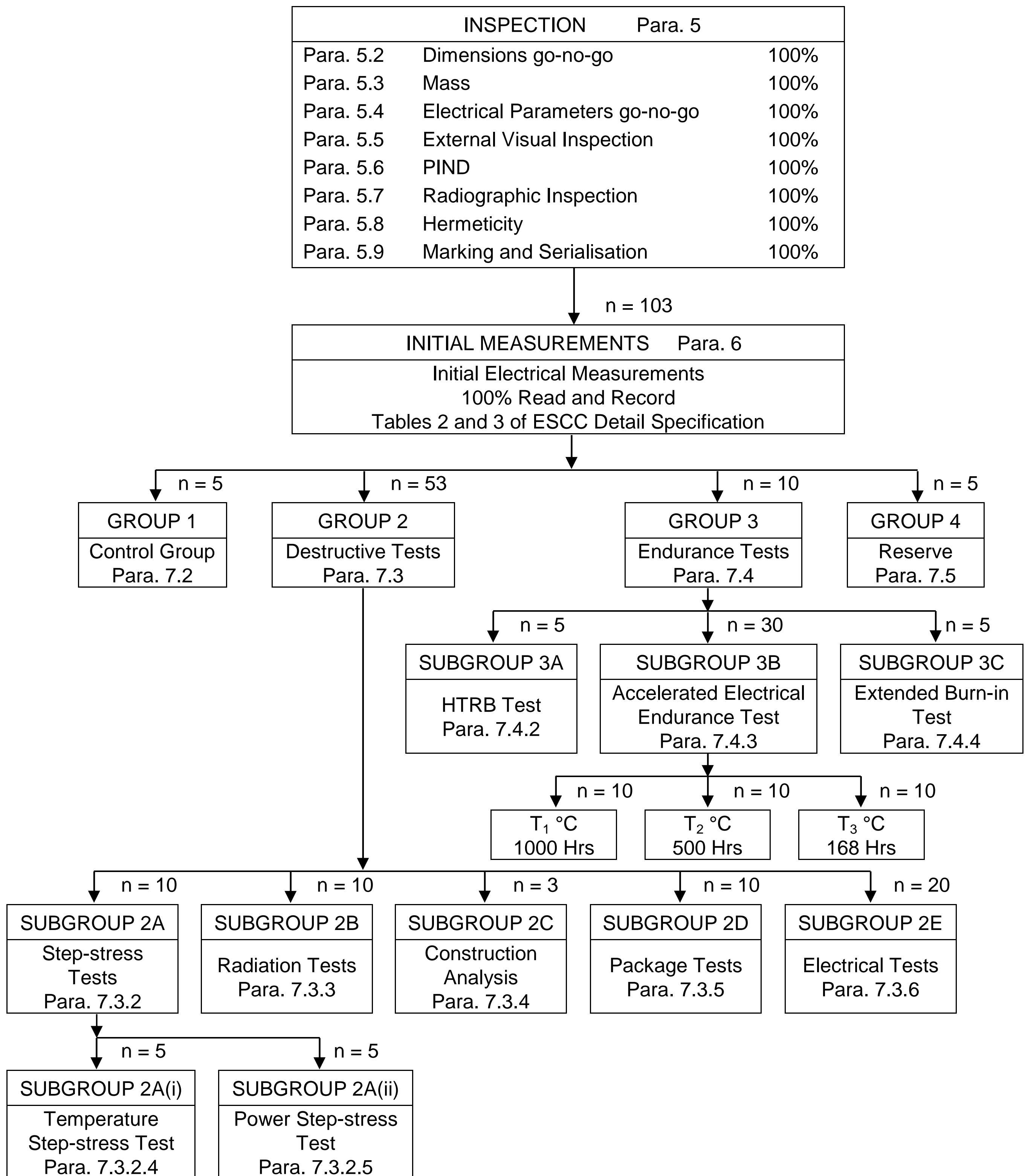
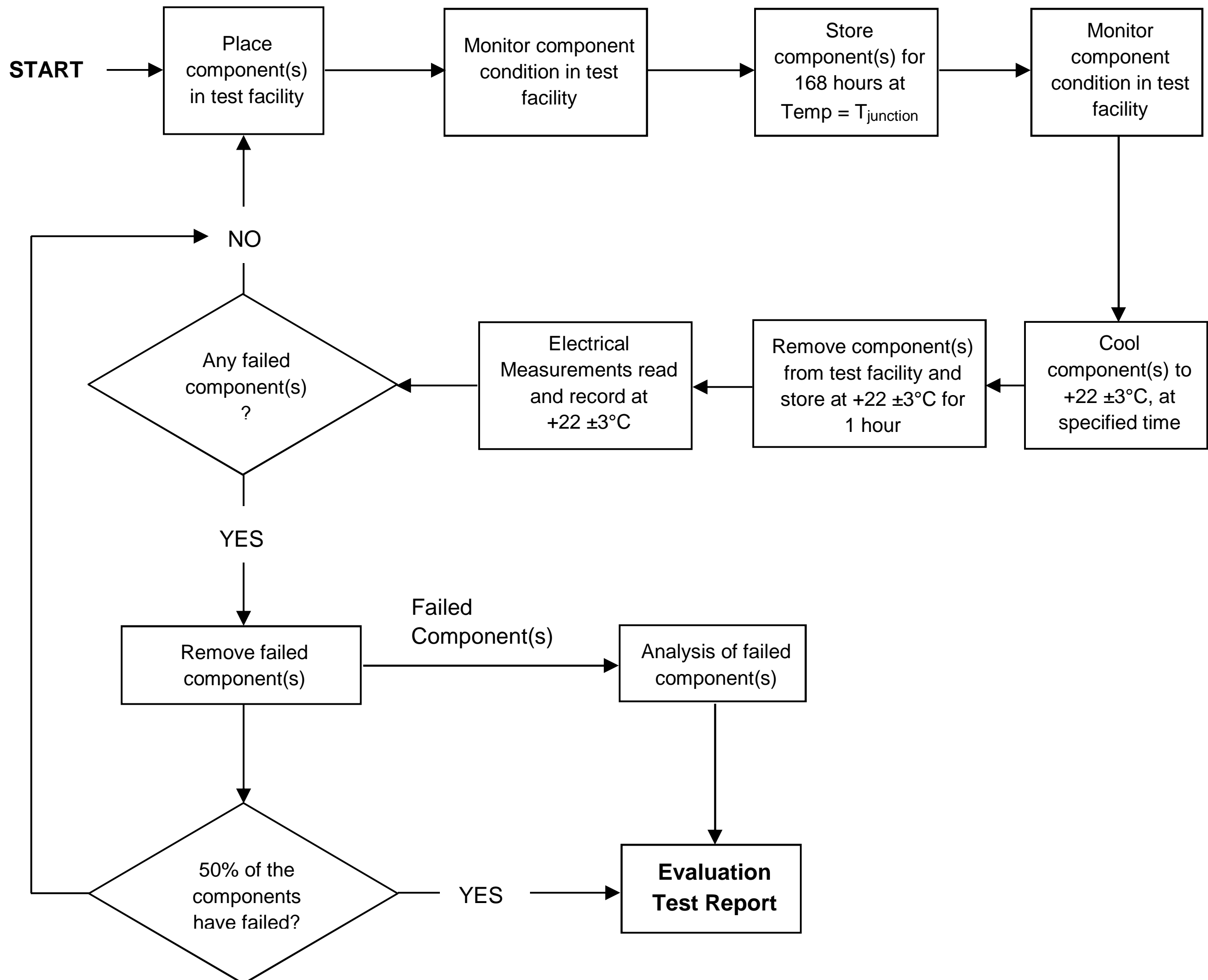


CHART II – TEMPERATURE STEP-STRESS SEQUENCE



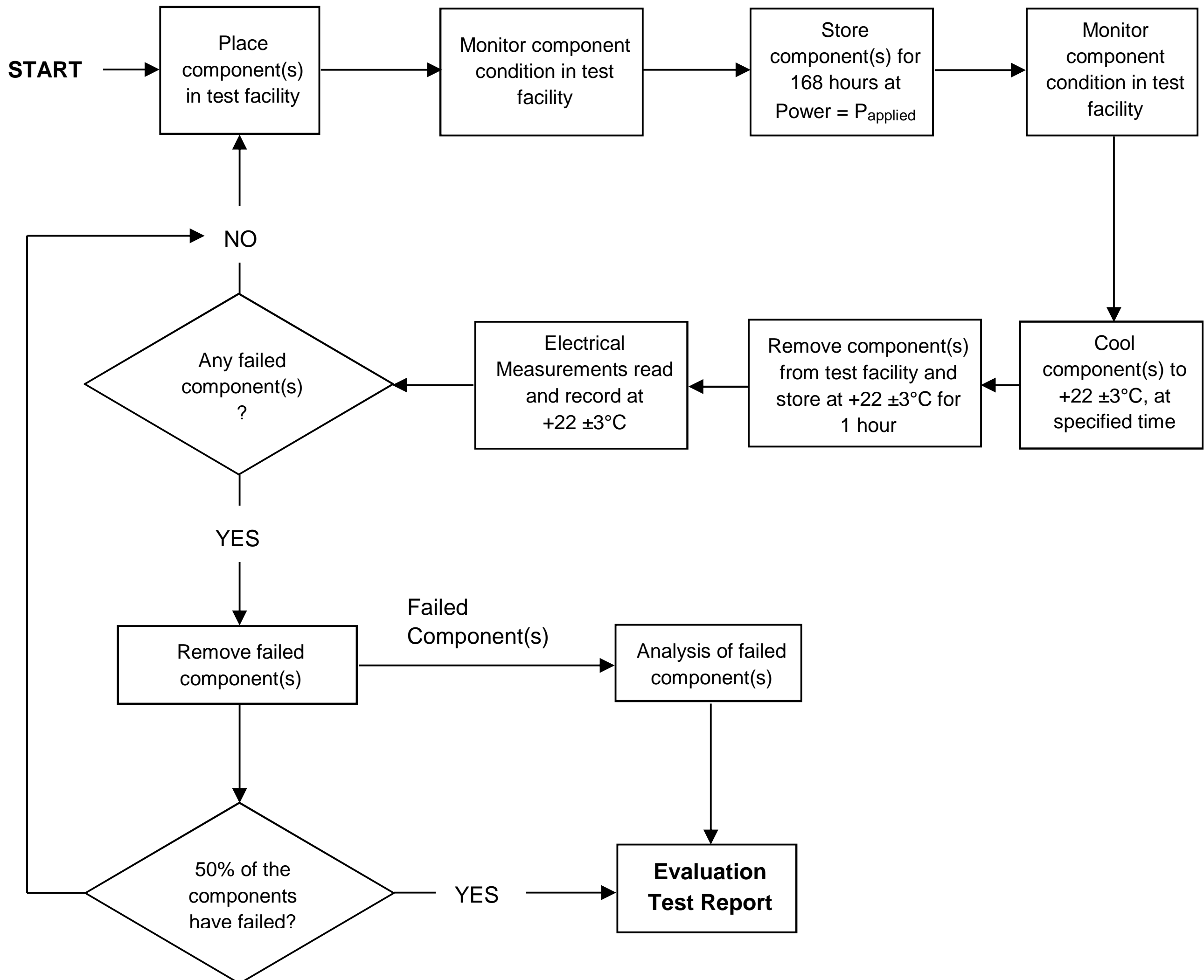
NOTES

1. Temperature steps with $T_{junction}$:

First step:	T_0	(°C)
	T_1	(°C)
	T_2	(°C)
Last step:	T_n	(°C)

with (T_n > … T_2 > T_1 > T_0)

CHART III - POWER STEP-STRESS SEQUENCE



NOTES

1. Power steps with $P_{applied}$:

First step: P_0 (W)

P_1 (W)

P_2 (W)

Last step: P_n (W)

with ($P_n > \dots P_2 > P_1 > P_0$)