REQUIREMENTS FOR CAPABILITY APPROVAL OF MONOLITHIC MICROWAVE INTEGRATED CIRCUITS (MMICS)

ESCC Detail Specification No. 2439010

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1 PURPOSE

This specification defines the requirements for the Capability Approval of Monolithic Microwave Microcircuit technologies. It outlines the requirements for the definition of the Capability Domain and its boundaries, the evaluation of a Capability Domain, Capability Approval testing and Type Approval testing. ESCC Basic Specification No. 24300 gives the general requirements for Capability Approval of electronic component technologies.

2 APPLICABLE DOCUMENTS

The following ESCC specifications are applicable to the extent specified herein. The relevant issues shall be those in effect on the date the Capability Approval is granted by the ESCC Executive.

No. 9010, Monolithic Microwave Integrated Circuits (MMICs)

No. 20200, Component Manufacturer Evaluation.

No. 22700, Requirements and Guidelines for the Process Identification Document (PID).

No. 24300, Requirements for the Capability Approval of Electronic Component Technologies for Space Application.

3 INTRODUCTION

Capability Approval is a status given to a Manufacturer for a specified Monolithic Microwave Microcircuit technology domain after successful completion of a Capability Approval Programme as described in ESCC Basic Specification No. 24300, the relevant section of ESCC Generic Specification No. 9010 and this document.

4 DEFINITION OF CAPABILITY DOMAIN AND BOUNDARIES

4.1 GENERAL

The Manufacturer shall define the Capability Domain for which Capability Approval is sought as required in ESCC Basic Specification No. 24300.

This definition shall result in the Process Identification Document (PID). The general requirements for this document are given in ESCC Basic Specification No. 22700.

This definition has to demonstrate that the Capability Domain represents a structured, clearly and controllably restricted, fully documented design methodology and manufacturing process for Monolothic Microwave Integrated Circuits (MMICs).

The definition of the Capability Domain shall also comprise the areas listed in the following paragraphs at least to the extent detailed therein. Additional information shall be supplied whenever necessitated by the particular nature of the technology under approval. In case any one of the characteristics in the following paragraphs should not apply to the technology and/or methodology under approval, this shall be stated in the PID.

Within the definition of the Capability Domain, 6 areas are of particular concern:

- The physical design and procedures which are closely related to the manufacturing process.
- The design system and procedures used to implement the circuit design methodology.
- The interface between circuit design and manufacturing.
- The manufacturing itself.
- The inspection and test procedures.
- The traceability.

These areas are addressed in the subsequent paragraphs.

4.2 PHYSICAL DESIGN

The physical design is governed by a set of technology specific rules and parameters, commonly called 'Design Rules'. These rules define the construction and composition of all structures foreseen for the design and manufacture of a Monolithic Microwave Integrated Circuit in a specific technology.

The description of the physical design requires the definition of at least the following characteristics:

The layout rule set which specifies the topology of all physical structures, including those for alignment and test purposes in terms of:

- Function (e.g. active layer, recess, conductor, contact, dielectric, passivation, …).
- Shape (e.g. aspect ratios, polygon, angles, …).
- Size (e.g. minimum/maximum width/length/depth, …).
- Positioning (e.g. overlaps of compound structures, spacing between structures of equal or different nature).
- The vertical dimensions of all layers (e.g. epitaxy, mesa, recess, implantation, bridge, trenches, metallisation, ...).

The electrical rules and parameters set in terms of:

- The DC and RF current carrying capability of all layers which may be used for interconnecting purposes.
- The specific capacitance between layers (e.g. poly/substrate,metal/substrate, metal/dielectric/metal) distinguishing sheet and edge capacitances.
- Gate capacitance.
- Sheet resistivity of layers used for resistors.
- Dielectric breakdown voltages (DC and RF maximum values).
- Transistor and diode parameters including limits of application.
- Passive component parameters including limits of application.
- Critical distance between components (side-gating, backgating, coupling, etc.).

Other relevant parameters or restrictions not covered in the previous points like suitability to implement analogue/digital circuits or special circuit design techniques.

Limits of biasing, temperature, drive level, power and/or gate width per unity of area.

4.3 DESIGN SYSTEM

The design methodology is defined by the design system and all other procedures applied in the design of a Monolithic Microwave Integrated Circuit. The design system comprises simulation models, basic design data and software.

Capability Approval of a design system requires as a minimum:

- The implementation of a configuration control system guaranteeing the traceability of all software and data forming part of the system and
- The application of a quality assurance system addressing at least documentation procedures, acceptance testing prior to system release and the organisation of error reporting and corrective action procedures.

Both systems shall be fully documented and their application has to be evident. At least the following items shall be covered in the PID:

(a) A general description of the design system including block diagrams representing:
- The software structure of the system.
- The design flow, distinguishing between interactive and automatic actions.

(b) The library of fixed cells, including pad cells, shall be described at least in terms of the following relevant details:
- The layout of all the discrete cells characterised by its name, connections and dimensions including limits of these parameters.
- The detailed circuit schematic including effective element size.
- The final layout after completion of all post processing steps such as compaction or shrinking. It shall be presented in the form of plot on a scale allowing clear recognition of all structures.

(c) The library of the models for the active and passive cells in terms of at least the following relevant details:
- DC, small signal and large signal models of all discrete cells, as applicable, with their scaling rules and limits of validity for each models.
- Typical and maximum variations of all the electrical parameters of the discrete cells within wafers and from wafer to wafer.

The verification procedure of all the models shall be described.

(d) Software and associated data shall be described in terms of:
- The origin and version of commercial software allowed for electrical design, verification and layout.
- The version and programming language for in-house developed software.
- Verification of the in-house software shall be described.
- Definition of data formats.
- Definition of programme interfaces.

(e) A description of the configuration control system.

(f) A description of the quality assurance system.

4.4 INTERFACE BETWEEN COMPONENT DESIGN AND MANUFACTURING

For components intended to be qualified by means of type approval on the basis of Capability Approval, a statement of compliance (Design Compliance Matrix) is required. This statement confirms the compliance of a particular component within the Capability Domain(s) to which it is attributed. This statement of compliance shall be issued during design reviews in the form of a Design Compliance Matrix.

During the design review the following items shall be addressed in this order:

- MMIC architecture.
- MMIC schematics.
- Simulation results.
- Sensitivity and stability analysis.

- Layout.
- Derating analysis.
- Design compliance matrix.
- Detail Specification.

The Design Compliance Matrix (checklist) shall be agreed by the Manufacturer and the Designer. Evidence that the design is completely within, and limited to, the approved Capability Domain shall be submitted to the ESCC Executive. The Design Compliance Matrix shall address as a minimum the following items:

- The component has been designed with the capability approved circuitry, models, layout, etc. as stated in the PID.
- Any discrepancies, modifications of models, layout, etc. shall be clearly described and assessed.
- The results of the Manufacturer layout checking.
- An assessment from the Manufacturer that the foreseen function(s) and characteristics are realistic within the framework of the Capability Domain.

The Designer shall provide full information regarding documentation control and traceability of:

- The hardware, software, data safe-keeping and traceability used for this design.
- The description of the function and expected characteristic.
- Stability and sensitivity analysis of the component.
- Derating analysis.

The ESCC Executive shall have free access to this information at the Designer's premises.

This compliance matrix form shall be referenced in the PID and shall be applied for design performed in the Manufacturer facilities and by external design facilities.

4.5 MANUFACTURE

4.5.1 Materials

The Manufacturer shall describe the procedures for selection, procurement and control of materials used for the production of components within the Capability Domain. The PID shall, as a minimum, cover the following items:

- The selection and qualification (approval methodology) of the materials used. A list of procurement specifications for the selected materials.
- A list of incoming inspection procedures and other documents used to ensure the consistent quality of materials used.
- Procedures for traceability and control of limited shelf life items.

4.5.2 Technologies

The Manufacturer's description of the basic technologies for the manufacturing of Monolithic Microwave Microcircuits shall at least cover:

- Type of technology i.e. MESFET, HEMT, HBT, BJT, etc.
- Type of substrate (GaAs, Si, SiGe, InP, etc.), orientation, epitaxy, backside etc.
- Method of pattern formation.
- Method for die attach.
- Material and method for wire bonding.
- Encapsulation method, materials and material combinations used.
- Range of packages (if applicable).

4.5.3 Processes

The Manufacturer shall describe the processes for the manufacture of components within the Capability Domain. He shall also give references to the documents specifying the processes. At least the following areas shall be covered including a statement of the equipment used:

- Clean room conditions.
- Wafer preparation.
- Mask manufacture and methods for identification of masks.
- Photolithographic methods (application and drying of photoresist, exposure, development, etching, photoresist removal, cleaning etc.).
- Active layer formation including etching methods.
- Dielectric and passivation deposition processes.
- Wafer storage conditions before, during and after process.
- Probing, dicing.
- Assembly (die attach, wire bonding, encapsulation).

The PID shall contain a list (if applicable) of all package types and pin counts to be included in the Capability Domain.

The package with the highest pin count of each type represents a boundary of the Capability Domain.

4.6 INSPECTION AND TEST

The Manufacturer shall describe the inspection and test methods giving references to the documents specifying the methods. As a minimum the following areas shall be covered:

- Incoming inspection testing.
- In-process inspection.
- Wafer acceptance testing.
- Precap inspection (if applicable).
- Final production testing.
- Burn-in and electrical testing.
- Type Approval testing.
- Lot Acceptance testing.

4.7 TRACEABILITY

The Manufacturer shall describe his method for assuring traceability of materials, test structures and components. At least the following points shall be covered:

- The use of purchase orders and specifications.
- The use of route sheet and travellers.
- The traceability of test structures.

If the Manufacturer intends to deliver naked dice in the frame of the Capability Approval, the naked dice shall be marked (position, etc.).

5 TEST STRUCTURES AND MEASUREMENT METHODS

5.1 GENERAL

Technology Characterisation Vehicles (TCVs), Dynamic Evaluation Circuits (DECs) and Representative Integrated Circuits (RICs) which are required for Evaluation, Capability Approval testing and process control shall be described in the PID. They shall be produced strictly according to this document. Production, Wafer Acceptance Test, Final Production Test and Burn-in tests shall be to the highest level specified in the PID.

The description of the TCV, DEC and RIC within the PID shall include Detail Specification and Design Compliance Matrix.

5.2 TECHNOLOGY CHARACTERISATION VEHICLE (TCV)

A TCV shall consist of basic active and passive elements from the cell library including specific elements relevant of the technology. The TCV could be a set of different test vehicles. Process Control Monitor (PCM) elements could be included in the TCV. The TCV must be designed with the most constrained design rules. TCV structures shall be provided to verify all relevant material, process and fixed cell DC parameters:

- Interface properties.
- Sheet resistance for each non dielectric layer e.g. epitaxial layers, implanted regions, etc.
- Ohmic contacts.
- Thin film resistors and implanted resistors.
- Implantation barriers.
- Etching.
- Surface quality.
- Side/back gating.
- Via-hole.
- Air bridge.
- Interconnection layers.
- Transmission/coupling lines.
- Discrete capacitors.
- Leakage currents.
- Wire bonding.
- Die bonding.
- Mask alignment.

N.B.
The use of two TCVs is recommended, (one "cold" and one "dissipating") to facilitate definition of life testing conditions.

5.3 DYNAMIC EVALUATION CIRCUIT (DEC)

A Dynamic Evaluation Circuit shall be one or a set of discrete active elements. It shall be able to be bonded into a discrete package. This package must minimise any RF parasitic effects. The DEC shall also be designed in order to allow RF-on-Wafer measurements.

The Dynamic Evaluation Circuit shall be designed to allow the assessment of the RF performance of the technology. The following parameters shall be addressed when they are relevant to this test structure:

- Scattering parameters.
- Power compression parameters.
- Noise figures and associated gain.
- Phase, time transfer delay parameters.
- AM/PM conversion.
- etc.

5.4 REPRESENTATIVE INTEGRATED CIRCUIT (RIC)

The Representative Integrated Circuit (RIC) is a complex or a set of complex integrated circuit(s) designed fully in accordance within the Capability Domain. The RIC shall also be designed to allow RF-on-Wafer measurements.

The purpose of the RIC is mainly:

- To partially validate the design domain (design models, design system, layout rules, etc.).
- To partially assess the reliability of a complex MMIC and in particular some applications that can be considered critical (e.g. differential amplifier, saturated applications, ...).

MMICs that have already been developed, or are under development, may be proposed as RICs provided they are in accordance with the Capability Domain and as far as they are representative and useful to verify the design and manufacture capability.

N.B.
The involvement of an external design centre is recommended but not mandatory.

5.5 DESIGN AND LAYOUT RULES

TCVs, DECs and RICs shall be provided to verify the geometrical layout rule set and to allow electrical and optical evaluation of the layer to layer misalignment which might occur during manufacturing.

In order to magnify problems and to enhance the diagnostic capabilities, test structures with design layout rules beyond worst case may be added where these would help to define process and device limits and help to assess reliability.

5.6 TECHNOLOGY

Additional appropriate test structures shall be provided for the evaluation of other known failure modes or parametric sensitivity or degradation affecting the technology under approval when subjected to radiation or other specific applications.

6 EVALUATION OF A CAPABILITY DOMAIN

The evaluation of a Capability Domain shall be in accordance with the requirements of ESCC Basic Specification No. 22600 and related ancillary specifications.

On completion of evaluation testing, the final definition of the Capability Domain and its boundaries shall be agreed between the Manufacturer and the ESCC Executive and the Capability Abstract shall be issued.

7 CAPABILITY APPROVAL TESTING

7.1 GENERAL

The general requirements for the preparation of a Capability Approval test programme are defined in ESCC Basic Specification No. 24300. This programme shall be reviewed and approved by the ESCC Executive prior to the start of Capability Approval testing.

The Capability Approval test programme for technologies covered by this specification shall generally consist of the tests and subgroups given in Chart I of this specification. The requirements specified therein may be reduced by the ESCC Executive if it is demonstrated that particular requirements have already been covered in a different but equivalent qualification, evaluation or Capability Approval programme. The test vehicles submitted to Chart I testing shall be the RIC as defined in the PID. All packaging related tests shall be performed on the package with the highest pincount for each type of package as stated in the PID.

Prior to Capability Approval testing (Chart I of this specification):

- Wafer Lot Acceptance (Para. 5.2 of ESCC No. 9010) shall be performed.
- Wafer Screening (Chart II(a) of ESCC No. 9010) shall be performed.
- Wafer Acceptance Testing (Chart III(a) of ESCC No. 9010) shall be carried out on both TCV and DEC.
- RICs shall be submitted to Final Production tests (Chart II(b) of ESCC No. 9010) and Burn-in and Electrical Measurements (Chart III(b) of ESCC No. 9010).

7.2 CAPABILITY APPROVAL TEST REPORT

On completion of the Capability Approval testing the Manufacturer shall assemble all relevant test data and documentation in the form of a test report. This report shall be sent to the ESCC Executive for review.

8 COMPONENT TYPE APPROVAL TEST

8.1 GENERAL

For a component type manufactured within a Monolithic Microwave Microcircuit Capability Domain the qualification procedure of ESCC Basic Specification No. 24300 shall apply.

Component Type Approval testing is only applicable to those components that have been designed and manufactured within the boundaries of an approved Capability Domain and for which a statement of compliance has been issued.

The Component Type Approval testing shall be performed on the specified sample, chosen at random from components which have successfully passed the tests in Charts II(b) and III(b) of ESCC Generic Specification No. 9010 for testing level 'B'. Component Type Approval testing shall consist of the tests specified in Chart II of this specification.

Sample size shall be 10 pieces minimum. Accept criteria shall be zero failures.

8.2 TEST METHODS AND CONDITIONS

8.2.1 Thermal Analysis

Thermal analysis shall be performed using adequate methods to identify "hot-spots" which shall include, but not be limited to, infra-red cameras or liquid crystal. Regions of abnormally elevated temperature shall be identified and characterised.

8.2.2 DC and RF Characterisation

Characterisation shall be carried out under "worst-case" operating conditions which shall include, when applicable, but not be restricted to:

- RF overdriving.
- Input/Output mismatching.
- Source and load pulling.
- Pushing and pulling (oscillators).
- Pulse operation applications.

8.2.3 Operating Life Test

Operating life test shall be performed in accordance with ESCC Generic Specification No. 9010, Paras. 9.25.1 and 9.5.4. The acceptance criteria shall be no failures allowed.

9 REDUCTION, EXTENSION AND CHANGE OF THE CAPABILITY DOMAIN

Any modification such as reduction, extension and change of the Capability Domain shall be in accordance with ESCC Basic Specification No. 24300.

In order to classify potential modifications, an evaluation matrix shall be included in the PID. This evaluation matrix features the parameters defining the Capability Domain and their interdependence. The relevance of a parameter in conjunction with the consequences for related parameters will support an efficient classification as minor or major changes.

For the distinction between minor and major changes the following shall be considered as a general guideline:

- Minor changes shall have no or only little impact on the Capability Domain and its boundaries and must be downward compatible (previously designed components must still be manufacturable without redesign or changes to their specification). This may be the case for isolated parameter changes or the replacement of equipment and materials for the purpose of yield enhancement or to improve safety margins. The expansion of libraries can be considered a minor modification if similar prototypes are already existing but require documentation as per Para. 4.3 of this document.

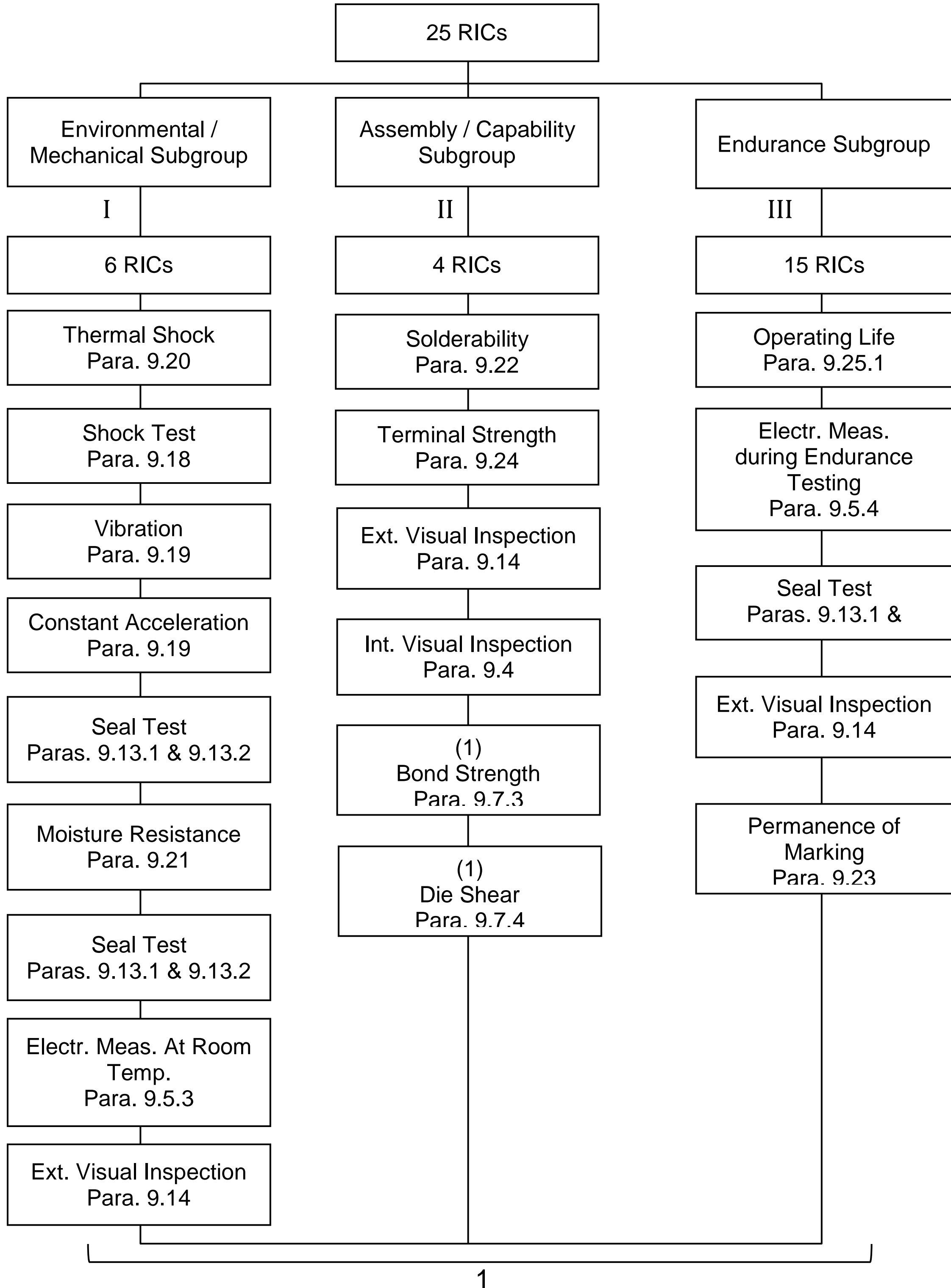
In case of doubt or if circuit performance or radiation tolerance is adversely affected changes must be classified as major.

10 PROCUREMENT

Procurement of components manufactured within the Capability Domain shall be in accordance with the requirements of Section 8 of ESCC Generic Specification No. 9010.

CHART I – CAPABILITY APPROVAL TESTING

All referenced paragraphs in this Chart refer to ESCC Generic Specification No. 9010.

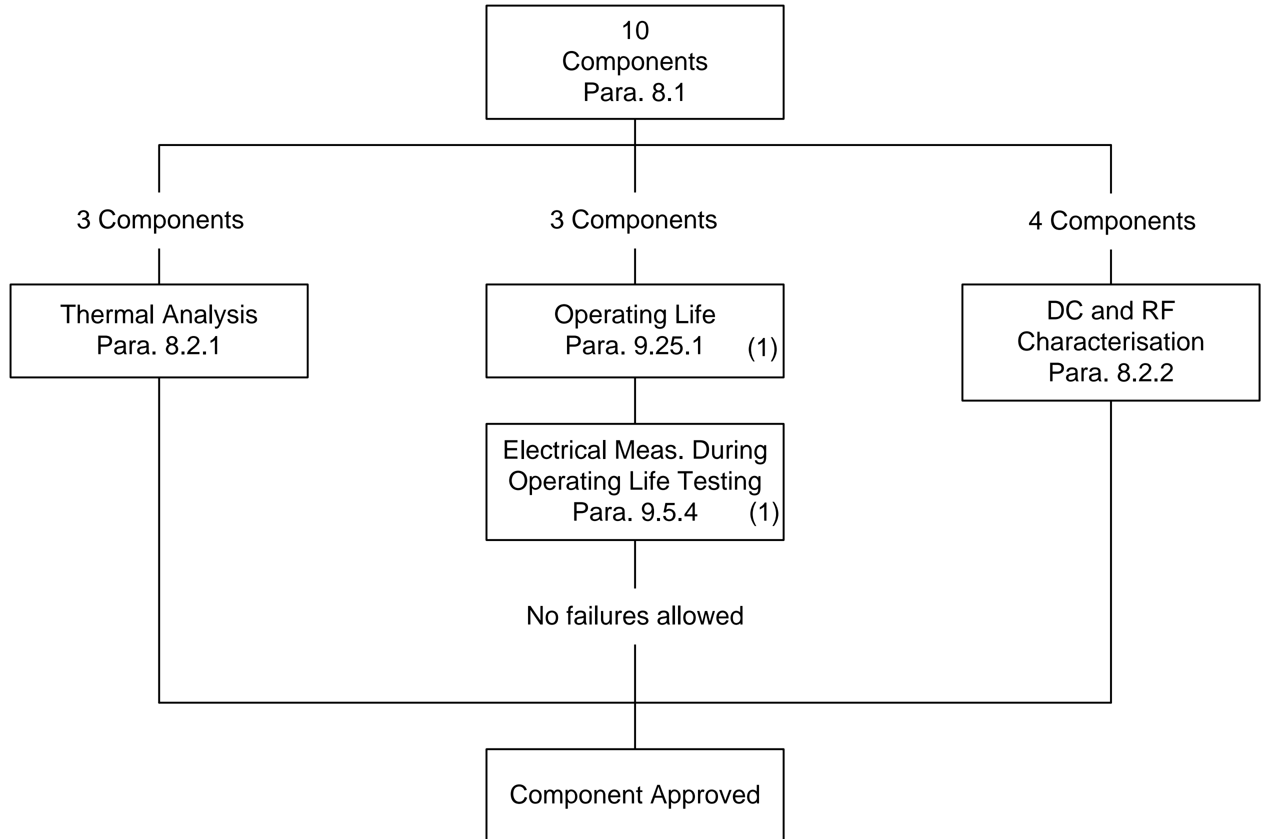


Total allowable number of failed components: 1.

NOTES

1. No failures allowed for these tests.

CHART II – TYPE APPROVAL TESTING



NOTES

1. The paragraph references are from ESCC Generic Specification No. 9010.