REQUIREMENTS

FOR CAPABILITY APPROVAL OF

MONOLITHIC MICROCIRCUIT TECHNOLOGIES

ESCC Basic Specification No. 2439000

Issue 2	January 2014

Document Custodian: European Space Agency – see https://escies.org

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DCR No.	CHANGE DESCRIPTION
799, 827	Specification upissued to incorporate editorial changes per DCR.

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1 PURPOSE

This specification defines the requirements for Capability Approval of Monolithic Microcircuit Technologies. It outlines the requirements for the definition of the Capability Domain and its boundaries, the evaluation of a Capability Domain, Capability Approval Testing and component type approval testing. ESCC Basic Specification No. 24300 gives the general requirements for Capability Approval of electronic component technologies.

2 APPLICABLE DOCUMENTS

The following ESCC specifications are applicable to the extent specified herein. The relevant issues shall be those in effect on the date the Capability Approval is granted.

No. 24300, Requirements for the Capability Approval of Electronic Component Technologies for Space Application.

No. 20200, Requirements for the Evaluation of a Manufacturer for the Manufacture and Supply of Standard Electronic Components for Space Application.

No. 22700, Requirements and Guidelines for the Process Identification Document (PID).

No. 9000, Integrated Circuits, Monolithic.

3 INTRODUCTION

Capability Approval is a status given to a Manufacturer for a specified monolithic microcircuit technology domain after successful completion of a capability approval programme as described in ESCC Basic Specification No. 24300, the relevant parts of ESCC Generic Specification No. 9000 and this document.

4 DEFINITION OF CAPABILITY DOMAIN AND BOUNDARIES

4.1 GENERAL

The Manufacturer shall define the Capability Domain for which Capability Approval is sought as required in ESCC Basic Specification No. 24300.

This definition shall result in the Process Identification Document (PID). The general requirements for this document are given in ESCC Basic Specification No. 22700.

This definition has to demonstrate that the Capability Domain represents a structured, clearly and controllably restricted, fully documented design methodology and/or manufacturing process for monolithic integrated circuits.

This definition has to comprise the areas listed in the following paragraphs at least to the extent detailed therein. Additional information has to be supplied whenever necessitated by the particular nature of the technology under approval. In case any one of the characteristics in the following paragraphs should not apply to the technology and/or methodology under approval, this shall be stated and substantiated in the PID.

Within the definition of the Capability Domain, 6 areas are of particular concern:

- The physical design and procedures which are closely related to the manufacturing process.
- The design system and procedures used to implement the circuit design methodology.
- The interface between circuit design and manufacturing.
- The manufacturing itself.
- The inspection and test procedures.
- The traceability.

These areas are addressed in the subsequent paragraphs.

Capability Approval can be separately requested for a manufacturing process including all related aspects of physical design and test, and an automated circuit design methodology.

However, the Capability Approval for a design system can only be obtained in conjunction with a capability approved or approvable technology which is to be explicitly referenced in the definition of the Capability Domain of the design system.

4.2 PHYSICAL DESIGN

The physical design is governed by a set of technology specific rules and parameters, commonly called 'Design Rules'. These rules define the construction and composition of all structures foreseen for the design and manufacture of a monolithic integrated circuit in a specific technology. The description of the physical design requires the definition of at least the following characteristics.

The layout rule set which specifies the topology of all physical structures, including those for alignment and test purposes in terms of:

- Function (e.g. diffusion, conductor, contact, dielectric, ...).
- Shape (e.g. aspect ratios, polygon, angles, ...).
- Size (e.g. minimum/maximum width/length/depth, ...).
- Positioning (e.g. overlaps of compound structures, spacing between structures of equal or different nature).

The vertical dimensions of all layers (e.g. depth of diffusion, trenches; thickness of polysilicon, metalisation, ...).

The electrical rule and parameter set in terms of:

- Sheet resistivities.
- The current carrying capability of conductive layers.
- Sheet and edge capacitances.
- Dielectric breakdown voltages.
- Transistor parameters and associated simulation models.

Other relevant parameters or restrictions not covered in the previous points like suitability to implement analogue/digital circuits or special circuit design techniques.

Gate arrays and similar type integrated circuits exhibiting a partially fixed topology require a complete description of all masters to be included in the Capability Domain which includes the layout of elementary cells, the pad arrangement and a detailed presentation of the power and ground routing.

4.3 DESIGN SYSTEM

The design methodology is defined by the design system and all other procedures applied in the design of an integrated circuit. The design system comprises all software, basic design data and the hardware platform.

Capability Approval of a design system requires as a minimum:

1. The implementation of a configuration control system guaranteeing the traceability of all software and data forming part of the system and
2. The application of a quality assurance system addressing at least documentation procedures, acceptance testing prior to system release and the organisation of error reporting and corrective action procedures.

Both systems shall be fully documented and their application has to be evident.

At least the following items shall be covered in the PID.

(a) A general description of the design system including block diagrams representing:
- The software structure of the system.
- The design flow, distinguishing between interactive and automatic actions.
- The data flow within the system, with emphasis on the dynamics of the accumulated design data.

(b) A description of the hardware platform (e.g. work stations, memory requirements, LAN, host computers etc.).

(c) The library of fixed cells, including pad cells, shall be described at least in terms of the following relevant details:
- The circuit symbol characterised by its name and input/output connections with signal names and associated function.
- The logic diagram and truth table supplemented by a state diagram for sequential circuits.
- All relevant electrical and timing parameters including the driving capability and short circuit protection of outputs and the static and dynamic power consumption.
- The detailed circuit schematic including effective transistor sizes.
- The final layout after completion of all postprocessing steps like compaction or shrinking. It shall be presented in form of a coloured plot in a scale allowing distinction of all structures.

  The development process of the cell library shall be described in terms of geometrical, functional, electrical and timing checks performed for verification.

(d) Software and associated data shall be described in terms of:
- The origin and version of the programme.
- A comprehensive description of its functional scope.
- The programming language and the amount of code.
- The memory requirement.
- Definition of data formats and description languages.
- Definition of programme interfaces.
- A description of the human interface with admitted or required interactivity and output format.
- All software serving simulation type purposes requires a detailed description of the underlying models and their parametric capability.
- Parametrisable, flexible circuits which are based on a dedicated library of subcells different from the library of fixed cells addressed earlier, shall be defined in terms of all characteristics listed in this paragraph.

(e) A description of the configuration control system.

(f) A description of the quality assurance system.

4.4 INTERFACE BETWEEN COMPONENT DESIGN AND MANUFACTURING

For components intended to be qualified by means of type approval on the basis of Capability Approval a statement of compliance is required.

This statement confirms the compliance of a particular component with the Capability Domain(s) to which it is attributed. The statement of compliance shall be issued prior to the release of a design for production and establishes the three following facts.

1. The component has been designed exclusively with capability approved circuitry as stated in the PID. In general this has to be verified by a documented test. However, this test may be waived for design systems which do not permit the creation and manipulation of a layout by a User or the importation of foreign circuitry.
2. The component has been designed such that it is compliant with all the technology related geometrical, electrical and other rules stated in the PID. In general this shall be verified by a documented test.
   The responsibility for this design rule verification resides with the Manufacturer.
3. The netlist and layout data are 100% compatible. In general this shall be verified by a documented test.

The tests used to establish the compliance of a component to its attributed Capability Domain shall be defined in the PID.

4.5 MANUFACTURE

4.5.1 Materials

The Manufacturer shall describe the procedures for selection, procurement and control of materials used for the production of components within the Capability Domain. The PID shall as a minimum cover the following items:

- The selection and approval of the materials used.
- A list of procurement specifications for the selected materials.
- A list of incoming inspection procedures and other documents used to ensure the consistent quality of materials used.
- Procedures for traceability and control of limited shelf life items.

4.5.2 Technologies

The Manufacturer's description of the basic technologies for the manufacturing of monolithic microcircuits shall at least cover :

- Type of technology i.e. CMOS, I2L, SOS etc.
- Type of substrate, orientation, epitaxy, backside etc.
- Method of pattern formation.
- Method of die attach.
- Material and method of wire bonding.
- Encapsulation method, materials and material combinations used.
- Range of packages.

4.5.3 Processes

The Manufacturer shall describe the processes for the manufacture of components within the Capability Domain. He shall also give reference to the documents specifying the processes. At least the following areas shall be covered including a statement on the equipment used:

- Clean room conditions.
- Wafer preparation.
- Mask manufacture and methods for identification of masks.
- Photolithographicmethods (application and drying of photoresist, exposure, development, etching, photoresist removal, cleaning etc).
- Doping processes (diffusion, ion implantation).
- Oxidation processes.
- Passivation processes.
- Rework procedures.
- Probing, dicing.
- Assembly (die attach, wire bonding, encapsulation).

The PID shall contain a list of all package types and pincounts to be included in the Capability Domain.

The package with the highest pincount of each type represents a boundary of the Capability Domain.

4.6 INSPECTION AND TEST

The Manufacturer shall describe the inspection and test methods giving references to the documents specifying the methods. At least the following areas shall be covered:

- Incoming inspection testing.
- In-process inspection.
- Precap inspections.
- Final production testing.
- Burn-in and electrical testing.
- Lot acceptance testing.
- External and internal inspections.

4.7 TRACEABILITY

The Manufacturer shall describe his method for assuring traceability of materials, test structures and components. At least the following points shall be covered:

- The use of purchase orders and specifications.
- The use of route sheets and travellers.
- The traceability of test structures.

5 TEST STRUCTURES AND MEASUREMENT METHODS

5.1 GENERAL

Test structures which are required for evaluation, Capability Approval Testing and process control shall be described in the PID and shall be produced strictly according to this document. Production and screening shall be to the highest level specified in the PID. Test structures shall be incorporated at appropriate locations on all wafers and where applicable on each die. The description of the test structures within the PID shall include the test and/or measurement method to be applied. Test structures for Capability Approval Testing shall be incorporated into a test die serving as a test vehicle as outlined in the relevant paragraph of this specification.

5.2 PROCESS AND DEVICE CHARACTERISTICS

Test structures shall be provided to verify all relevant material, process and device parameters such as those listed below:

- Interface properties.
- Crystalline defects in the semiconductor material.
- Sheet resistance for each nondielectric layer e.g. diffused or implanted regions, polysilicon metal or other.
- Contact resistance.
- Dielectric isolation (breakdown voltage).
- Transistor parameters.
- Carrier mobilities.
- Minimum line widths.
- Interface state density.
- Doping profiles.
- Leakage currents.
- Wire bonding.
- Die bonding.
- Junction alignment.

5.3 DESIGN AND LAYOUT RULES

Test structures shall be provided to verify the geometrical layout rule set and to allow electrical or optical evaluation of layer-to-layer misalignment which might occur during manufacturing.

In order to magnify problems and to enhance the diagnostic capabilities, test structures with design layout rules beyond worst case should be added when feasible. These types of structures will help to define process and device limits and help to assure reliability.

5.4 CIRCUIT PERFORMANCE

Test structures shall be provided to characterise static and dynamic circuit performance in terms of quiescent currents, threshold voltages, propagation delays and other relevant parameters for test circuits and production circuits.

Propagation delays shall be measured by means of ring oscillator type circuits or delay chains unless dedicated test circuits of a different type are more suitable for a particular technology.

Test dice shall include additional functional circuitry as available and representative for the cell library.

Particularly complex cells and software generated circuit modules like RAMs, ROMs, PLAs and any other macro functions shall be appropriately considered.

5.5 DEVICE AND CIRCUIT RELIABILITY INCLUDING RADIATION TOLERANCE

Test structures shall be provided to establish circuit reliability by verifying the stability of the semiconductor material when subject to stresses such as voltage, temperature, humidity and radiation. Where appropriate the following test structures shall be included:

- Transistors and capacitors for measurement of oxide charge density and threshold voltage shifts.
- Diodes and transistors for the measurement of leakage currents.
- Resistors for the measurement of current carrying capabilities and electromigration.

Provisions shall also be included for measuring dielectric breakdown voltage for each dielectric layer. The breakdown test is a destructive test and requires several structures to obtain a set of values over the temperature range. A ring oscillator or delay chain type structure shall also be included to determine the shift in gate delay as a result of thermal stress or radiation. Appropriate test structures shall be provided for the evaluation of other known failure modes or parametric degradations affecting the technology under approval when subjected to radiation.

5.6 TECHNOLOGY

Additional test structures for a particular technology shall be used when appropriate.

5.7 TEST DICE

Wafers in all production lots of circuits intended to be or already qualified on the basis of Capability Approval should include test dice entirely composed of test structures to monitor the stability of the manufacturing process.

These test dice shall include test structures to allow an appropriate evaluation of the radiation tolerance of the process.

Those test dice which are suitable to provide data on radiation tolerance and component reliability may also be employed for wafer acceptance testing. All test dice shall be covered by specifications and shall be kept under configuration control.

A minimum of 3 test dice shall be distributed over each wafer of a production lot unless a different quantity and allocation establishing an equivalent degree of test coverage is agreed by the ESCC Executive and stated in the PID.

6 EVALUATION OF CAPABILITY DOMAIN

The evaluation of a Capability Domain shall be in accordance with the requirements of ESCC Basic Specification No. 22600.

Upon completion of evaluation testing, the final definition of the Capability Domain and its boundaries shall be agreed between the Manufacturer and the ESCC Executive and the Capability Abstract shall be issued.

7 CAPABILITY APPROVAL TESTING

7.1 GENERAL

The general requirements for the preparation of a Capability Approval test programme are defined in ESCC Basic Specification No. 24300. This programme shall be reviewed and approved by the ESCC Executive prior to the start of Capability Approval testing.

The Capability Approval test programme for technologies covered by this specification shall generally consist of the tests and subgroups given in Chart I of this specification. The test vehicles submitted to Chart I testing shall be the test structures as defined in Para. 5 of this specification. All packaging related tests shall be performed on the package with the highest pincount for each type of package as stated in the PID.

7.2 CAPABILITY APPROVAL TEST REPORT

On completion of the Capability Approval testing the manufacturer shall collect all relevant test data and documentation in form of a test report. This report shall be sent to the ESCC Executive for review.

8 COMPONENT TYPE APPROVAL TEST

For a component type manufactured within a monolithic microcircuit Capability Domain the qualification procedure of ESCC Basic Specification No. 24300 shall apply.

Component type approval testing is only applicable to those components that have been designed and manufactured within the boundaries of an approved Capability Domain and for which a statement of compliance has been issued.

The component type approval testing shall be performed on the specified sample, chosen at random from components which have successfully passed the tests in Charts F2 and of ESCC Generic Specification No. 9000, and shall consist of an operating life test in accordance with ESCC Generic Specification No. 9000, Para. 8.19.

Sample size shall be 3 pieces minimum.

Accept criteria shall be zero failures.

9 REDUCTION, EXTENSION AND CHANGE OF THE CAPABILITY DOMAIN

Any modification such as reduction, extension and change of the Capability Domain shall be in accordance with ESCC Basic Specification No. 24300.

In order to classify potential modifications, a matrix shall be included in the PID. This matrix shall list the parameters defining the Capability Domain and their interdependence. The importance of a parameter in conjunction with the consequences to related parameters will determine whether a change is minor or major.

For the distinction between minor and major changes the following shall be considered as a general guideline:

Minor changes shall have no or only little impact on the Capability Domain and its boundaries and must be downward compatible (previously designed components must still be manufacturable without redesign or changes to their specification). This may be the case for isolated parameter changes or the replacement of equipment and materials for the purpose of yield enhancement or to improve safety margins.

The expansion of libraries can be considered a minor modification if similar prototypes are already existing but requires documentation as per Para. 4.3 of this document.

In case of doubt or if circuit performance or radiation tolerance is adversely affected changes must be classified as major.

10 PROCUREMENT

Procurement of components manufactured within the capability boundaries shall be in accordance with the requirements of Section 7 of ESCC Generic Specification No. 9000.

CHART I - CAPABILITY APPROVAL TESTING

All referenced paragraphs in Chart I refer to ESCC Generic Specification No. 9000.

All notes refer to the notes to Chart F4 of ESCC Generic Specification No. 9000.