SCANNING ELECTRON MICROSCOPE (SEM) INSPECTION OF SEMICONDUCTOR DICE

ESCC Basic Specification No. 21400

Issue 2	February 2014

Document Custodian: European Space Agency – see https://escies.org

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DCR No.	CHANGE DESCRIPTION
838	Specification upissued to incorporate editorial changes per DCR.

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1 SCOPE

1.1 GENERAL

This specification describes the equipment and procedures to be used for the Scanning Electron Microscope (SEM) inspection of discrete semiconductor devices and integrated circuits.

When SEM Inspection is called for in an ESCC specification, it shall be used in conjunction with the relevant ancillary ESCC specification, numbered in the 21400 series, wherein the specific accept/reject criteria are prescribed (see Section 5).

1.2 ALTERNATIVE STANDARDS

Where the configuration of a particular component is not in accordance with the examples shown in this specification, or where current in-house inspection drawings or standards (accepted in the PID) are to be used, it shall be the Manufacturer's responsibility to obtain the formal interpretation from the ONS, or its designated representative, of any deviation.

2 DEFINITIONS

2.1 SEM INSPECTION LOT

A SEM inspection lot is defined as a number of wafers of the same type which are selected from the same diffusion, oxidation and metallisation run and from which a defined number of wafers shall be examined with the Scanning Electron Microscope.

2.2 OXIDE STEPS

Oxide steps are defined as any sloped or abrupt change in thickness of silicon oxide, silicon nitride and/or any other insulating layers on a semiconductor or integrated circuit.

2.3 MULTI-LEVEL METALLISATION SYSTEM

A multi-level metallisation system consists of two or more layers of metal, or any other conductive material, which are separated from each other by an insulating material.

2.4 MULTI-LAYERED-METAL

Multi-layered-metal is defined as two or more layers of metal or any other conductive material used for interconnections that are not isolated from each other by a grown or deposited insulating material.

2.5 CRITICAL AREAS

Critical areas shall be deemed to be those areas where, by virtue of design, an increased possibility of failure must be assumed. Such areas shall be clearly identified by the Manufacturer by the provision of an enlarged photograph of the complete die.

Examples of critical areas are:

- very small distances between conductors.
- very narrow conductors.
- very high and steep oxide steps.
- very small contact windows.

2.6 FAILED DICE

Failed dice are those which are not acceptable according to the reject criteria specified.

3 REQUIREMENTS

3.1 EQUIPMENT

3.1.1 Scanning Electron Microscope

The Scanning Electron Microscope used for this inspection shall meet the following requirements:

- Resolution: 25 nm or better.
- Magnification: X50 to X20,000.
- Acceleration voltage: 1 kV to 25kV.
- The specimen holder shall be so constructed that the specimen may be examined through a tilt angle ranging from 0° to 75° (see Figure I).
- It shall be possible to rotate the specimen through 360° over the full range of tilt angle.
- The chamber for the specimen shall be so constructed that a specimen measuring at least 15mm x 15mm may be examined.
- The equipment shall be capable of taking photographs.

3.1.2 Conductive Film Deposition

There shall be a facility for the deposition of a conductive film over the sample dice by vapour deposition or sputtering, if required.

3.2 SAMPLE SELECTION

3.2.1 Wafer Sample Selection from a Metallisation Run

Wafer sample selection shall be made after the metallisation process in accordance with Figure II. The wafers of more than one SEM inspection lot shall be placed in separate sections of the wafer-holder. If one SEM inspection lot has less wafers than there are places in the wafer-holder, the wafers shall be placed symmetrically from the outside to the centre of the wafer-holder. One wafer from the edge and one nearest the centre of the wafer-holder shall be taken as samples.

In case of small SEM inspection lots, it is permissible to break wafers and to place the pieces in the designated sections of the wafer-holder provided they are big enough for die selection according to Para. 3.2.3.

Up to die selection, the selected wafers shall be handled throughout all processing steps in such a manner that they retain their traceability.

For single wafer, non-rotating (fixed) deposition systems, wafer selection is not applicable.

3.2.2 Wafer Sample Selection from a Procured Lot

Selection of wafer samples from a procured lot shall be made as follows:

- Lot size smaller than 10 wafers
  One wafer per metallisation run to be selected at random.
- Lot size of 10 wafers or more
  Two wafers per metallisation run to be selected at random.

3.2.3 Die Sample Selection

From each wafer selected in accordance with Para. 3.2.1 or 3.2.2, three dice shall be selected

(a) As in Figure III, or
(b) As in Figure IV.
(c) For single wafer non-rotating (fixed) deposition systems, when the percentage variation in metallisation thickness from the centre of the wafer does not exceed ± 10%, dice can be selected at random.

3.2.3.1 Non-glassivated Devices

Dice from non-glassivated devices shall be selected and examined in accordance with Chart I.

3.2.3.2 Glassivated Devices

For the selection of dice from glassivated devices, there are two possibilities, viz.:

(a) Selection after etching of the metallisation structure, but before glassivation.

(i) If SEM inspection lots consist of 20 or more wafers, the selection and examination shall be in accordance with Chart II. The wafers from which the dice are selected shall not be used for further processing.

(ii) If SEM inspection lots consist of less than 20 wafers, the sample dice may be selected and examined in accordance with either Chart II or III. Wafers from which segments are detached for dice selection may be used for further production.

If, during the glassivation process, the temperatures used are higher than any temperature used during the metallisation process, minus 50°C, the unglassivated sample dice shall be exposed, in a suitable atmosphere (nitrogen), to the temperature/time characteristics of the glassivation process.

(b) Selection after glassivation.

Die samples shall be selected and examined in accordance with Chart IV and the glassivation shall be etched away without damaging the metallisation of the dice. This can be done when etching away the glassivation from the contact pads of the devices.

For procured wafers (see Para. 3.2.2), sample selection and examination shall be in accordance with Chart V.

3.2.3.3 Multi-level Metallisation Systems

Each metallisation layer shall be evaluated by detaching a segment (see Figure IV) from the appropriate wafer sample (see Chart VI). The selection of wafer and die samples and die examination shall be in accordance with Chart VI. It is permitted to use the remainder of the wafer sample from which the segment is detached for further processing.

If, after breaking any segment, the temperatures used for further processing of the wafers are higher than any temperature used during the metallisation process, minus 50°C, the segments for each metallisation layer shall be exposed, in a suitable atmosphere (nitrogen), to the temperature/time characteristics of the further processing.

3.3 DIE SAMPLE PREPARATION

3.3.1 Deposition of a Conductive Film

To obtain the required resolution it may be necessary to coat the die samples with a conductive film (e.g. gold, palladium/gold or carbon). When covering the edges and sides of the die with this film, care shall be taken to ensure good electrical contact between the film and the SEM specimen holder.

3.3.2 Mounting on Specimen Holder

The die shall be fitted flat and well-grounded to the specimen holder. The mounting shall be done in such a way that contamination is reduced to a minimum. If the die is mounted by means of a conductive adhesive or other conductive material, special care shall be taken not to obscure features to be examined.

3.4 DIE SAMPLE EXAMINATION, GENERAL REQUIREMENTS

3.4.1 General

All four edge directions shall be examined on each die for each type of contact window step and for each type of other oxide step (the word "oxide" shall be interpreted as any insulating material used on the semiconductor die, whether SiO_X, SiN_X,etc.). A single window (or other type of oxide step) may be viewed if metallisation covers the entire window (or other type of oxide step) extending up to and over each edge and onto the top of the oxide at each edge. Other windows (or other type of oxide step) on the die shall be examined to meet the requirement that all four directional edges of each type of window (or other type of oxide step) shall be examined on each die. Viewing for general metallisation defects, such as peeling and voiding, shall be such as to provide for the best examination for those defects.

3.4.2 Viewing Angle

Specimens shall be viewed at whatever angle is appropriate to accurately assess the quality of the metallisation. Contact windows are normally viewed at an angle of 45 to 60°. Metallisation thickness, adhesion, and etching defects are normally viewed at an angle of 60° or greater.

3.4.3 Viewing Direction

Specimens shall be viewed at whatever direction is appropriate to accurately assess the quality of the metallisation. This shall include looking at metallisation at the edges of contact windows and other types of oxide steps (see Para. 3.4.1) in directions that provide unshadowed views of each edge. This may mean that the viewing angle is perpendicular to an edge, or in line with an edge, or at some oblique angle, whichever best resolves any question of defects at the oxide step.

3.4.4 Magnification

The magnification ranges shall be between X5,000 and X20,000 for examination of oxide steps and between X1,000 and X6,000 for examination for general metallisation defects such as peeling and voiding. When dice are subjected to re-inspection, such re-inspection shall be accomplished within the specified magnification range, but at any magnification within that range that is deemed appropriate.

3.5 DIE SAMPLE EXAMINATION, DETAILED REQUIREMENTS

3.5.1 Discrete Semiconductor Devices

3.5.1.1 Oxide steps

Inspect the metallisation at all types of oxide steps. In the case of R.F. and/or power transistors with interdigitated or mesh structures, as a minimum, each base-emitter stripe pair on each end of each pattern and every fourth base-emitter stripe pair within each pattern shall be inspected. Particular attention shall be directed to lateral etching defects and undercut etching at base and emitter oxide steps. Documentation shall be as specified in Section 4.

3.5.1.2 General Metallisation

Inspect all general metallisation on each die for defects such as peeling and voiding. Document in accordance with Section 4.

3.5.2 Integrated Circuits

3.5.2.1 Oxide Steps

Inspect the metallisation at all types of oxide steps. Document in accordance with Section 4.

3.5.2.2 General Metallisation

Inspect at least 25% of the general metallisation on each die for defects, such as peeling and voiding. Document in accordance with Section 4.

3.5.3 Multi-Layered-Metal Interconnection Systems

3.5.3.1 General

Multi-layered-metal is defined as two or more layers of metal, or any other material used for interconnections that are not isolated from each other by a grown or deposited insulating material. The term "underlying layer" shall refer to any layer below the top layer of metal. Each layer of metal shall be examined. The principal current-carrying layer shall be examined with the SEM. The other layers (e.g. barrier or adhesion) may be examined using either the SEM or an optical microscope, at the Manufacturer's option. The glassivation (if any) and each successive layer of metal shall be stripped by selective etching with suitable reagents, layer by layer, to enable the examination of each layer. Normally, each successive layer of metal will be stripped in sequence to expose the next underlying layer for examination. It may be impractical to remove the different layers on a single die, layer by layer. In this case, an additional die (dice) immediately adjacent on the slice to the original die shall be stripped to meet the requirement that all layers shall be exposed and examined. Specimen examination shall be in accordance with Para. 3.5.1 or 3.5.2, whichever is applicable.

3.5.3.2 Underlying Passive Metal Layers

When an underlying passive layer of metal is included which will, by design, conduct less than 10% of the total operating current, this layer shall be considered to perform a processing aid function only and shall not be subjected to the metallisation requirements of this specification.

Such metal layers shall be identified by the Manufacturer who will be required to provide suitable verification that the layers satisfy the above requirements. All such identified layers shall be included in the Process Identification Document (PID).

The identified layers shall not be used in current density calculations and their respective thickness(es) shall not be added to that of the principal conducting layer when calculating metallisation step coverage.

3.6 SPECIMEN AFTER EXAMINATION

No SEM-inspected specimen shall be used for further processing. The die samples of each accepted SEM inspection lot shall be stored at the Manufacturer's plant for a period of at least 24 months. They shall be delivered to the Orderer upon request.

3.7 ACCEPTANCE REQUIREMENTS

3.7.1 General

Rejection of dice shall be based upon batch process oriented defects. Rejection shall not be based upon workmanship and other type defects such as scratches, smeared metallisation, tooling marks, etc. In the event that the presence of such defects obscures the detailed features being examined, an additional die shall be examined which is immediately adjacent to the die with the obscured metallisation.

3.7.2 Single Wafer Acceptance Basis

The metallisation on a single wafer shall be judged acceptable only if all sample dice from that wafer are acceptable.

3.7.3 Lot Acceptance Basis

An entire lot shall be judged acceptable only when all sample dice from all sample wafers are acceptable. If a lot is rejected per this Para., each wafer from that lot may be individually examined. acceptance shall then be in accordance with Para. 3.7.2.

3.8 ACCEPT/REJECT CRITERIA

Further detailed examination/inspection requirements and the accept/reject criteria shall be as specified in the relevant ancillary ESCC 21400 series of specifications.

4 DOCUMENTATION

4.1 PHOTOGRAPHIC

After examination of the dice from each wafer, a minimum of three SEM photographs per SEM lot shall be taken and retained. The photographs shall be one each of the "worst case" oxide step, metallisation and contact window. Suspect features shall be examined and documented photographically at magnifications which enable a clear decision to be made as to their acceptability or rejection.

Photographs for documentation purposes shall measure, as a minimum, 6cm x 6cm and the object depicted shall fill this format as far as possible. The following magnifications shall only be used for documentation:

X20 - X50 - X100 - X200 - X500 - X1,000 - X5,000 - X10,000 and X20,000.

4.2 INFORMATION

The following information shall be traceable to each photograph:

(a) Manufacturer's name and address.
(b) Name and location of test house or laboratory.
(c) SEM operator/inspector's identification.
(d) Date of SEM inspection and photograph.
(e) Component part, type or reference number.
(f) SEM inspection lot number or code.
(g) Area forming subject of photograph.
(h) Magnification.
(i) Accelerating voltage.
(j) Viewing angle.

4.3 DISTRIBUTION OF DOCUMENTATION

The negatives of the photographs are not required as part of the documentation, but shall be retained by the Manufacturer. The Manufacturer shall submit one set of the required documentation to the Orderer and retain one set for his own records for three years.

5 ANCILLARY SPECIFICATIONS

The following ancillary specifications in the ESCC 21400 series have been issued for use in conjunction with this specification:

ESCC No. 2145000	Scanning Electron Microscope (SEM) Inspection of Semiconductor Dice for Discrete Non-Microwave Semiconductor Devices.
ESCC No. 2145010	Scanning Electron Microscope (SEM) Inspection of Semiconductor Dice for Discrete Microwave Semiconductor Devices.

TABLE 1 - EXAMINATION PROCEDURE FOR SAMPLE DICE

Device Type	Area of Examination	Examination	Min./Max. Magnification	Photographic Documentation
Discrete Semiconductors	Oxide steps (Note 1) (contact windows and other types of oxide steps)	All	X5,000 to X20,000	Two of the worst case oxide steps
	General metallisation	All	X1,000 to X6,000	Worst case general metallisation
Integrated Circuits	Oxide step (Note 1) (contact windows and other types of oxide steps)	At least one of each type of oxide step present	X5,000 to X20,000	Two of the worst case oxide steps
	General metallisation	25%	X1,000 to X6,000	Worst case general metallisation

NOTES

1. Scanning examination shall include all four directional edges of oxide steps (documentation need only show the worst case). Oxide steps include contact windows (emitters, bases, collectors, drains, sources, diffused resistors, diffused cross-unders, multi-level interconnection system contact windows, etc.) and other types of oxide steps (diffusion cuts for emitters, bases, collectors; field oxide steps; multi-level interconnection system oxide steps, etc.).

FIGURE I – VIEWING ANGLE

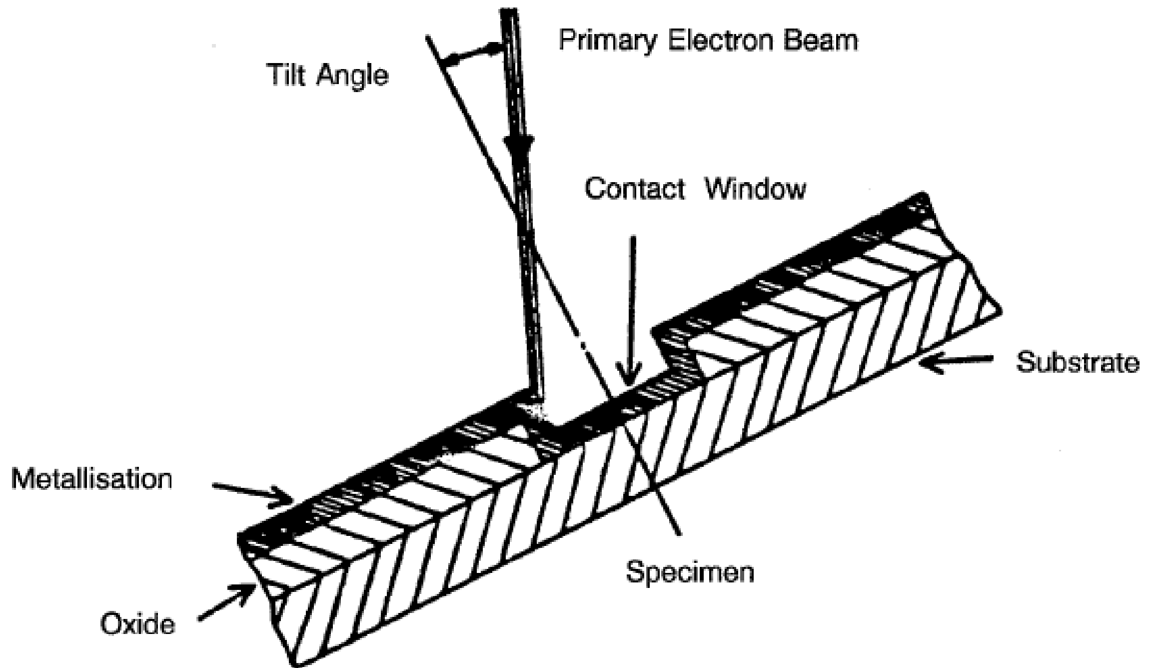


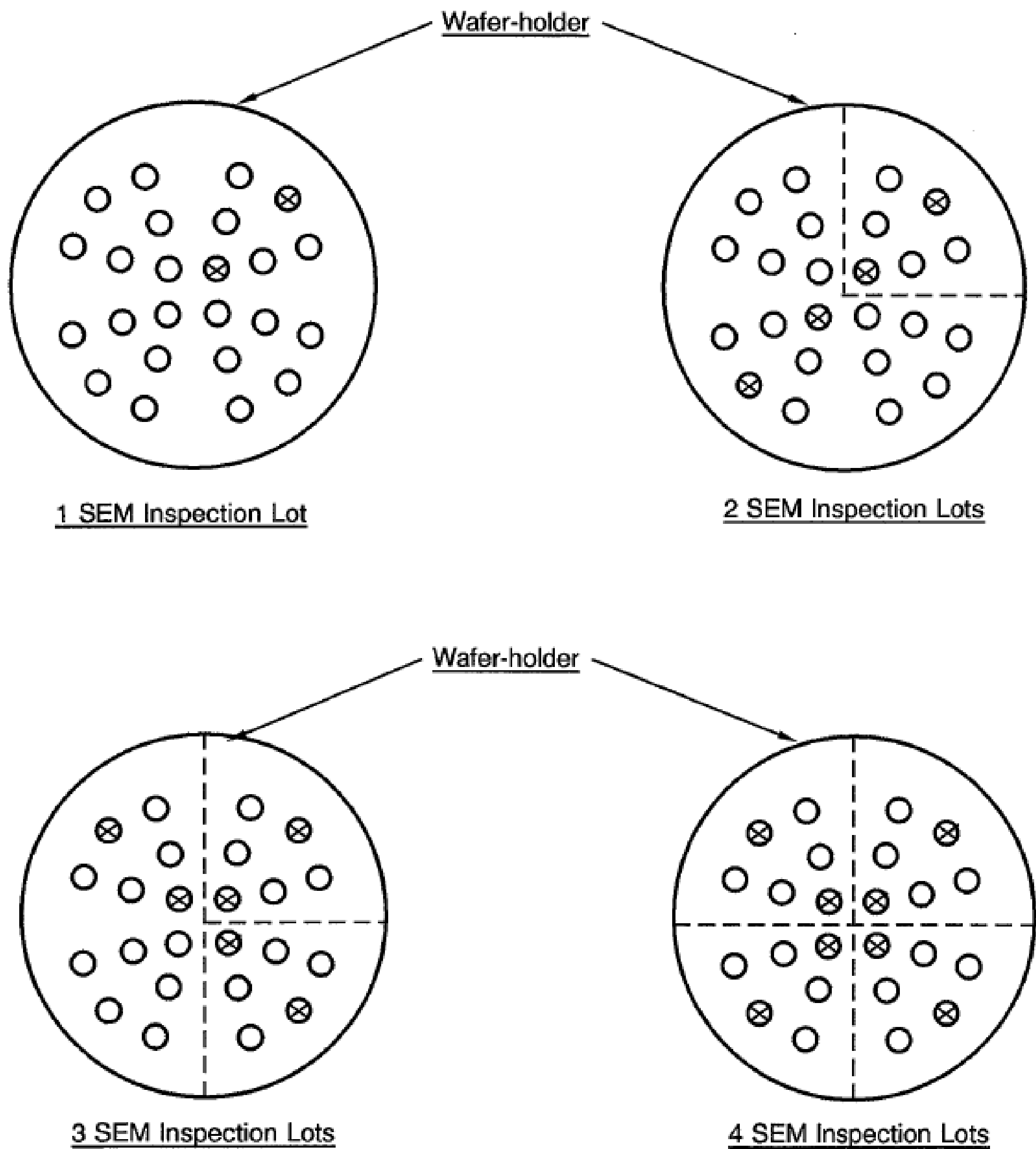
FIGURE II - WAFER SAMPLE SELECTION

Configuration of metallisation system

The wafer-holder is a planet in a rotating planetary system. Deposition source is below the wafer-holder.

Wafer sample selection plan

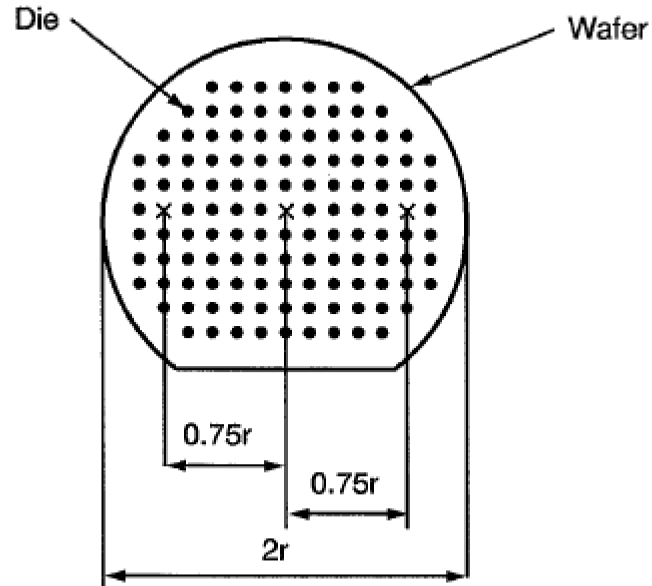
For each SEM inspection lot, one wafer from the periphery and one wafer from nearest the centre of the wafer-holder shall be selected as samples.



NOTES

1. The wafers marked X shall be selected as samples.

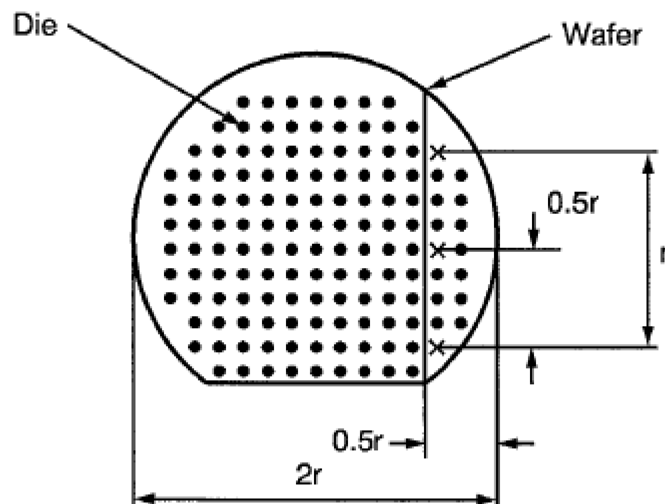
FIGURE III - DICE SELECTION ON WAFER DIAMETER



The 3 dice samples shall be situated on a wafer diameter (example shown).

The dice marked X shall be those examined.

FIGURE IV - DICE SELECTION ON WAFER SEGMENT



The 3 dice samples shall be situated on a segment of the wafer. It is permitted to detach the segment on any chord, but the dimensions of the segment shall be as shown.

The dice marked X shall be those examined.

DIE SAMPLE SELECTION CHARTS

In the charts which follow (I-VI), the legend used and abbreviations are as under:

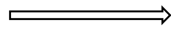
	Route for total SEM Inspection Lot.
	Route for sample wafer, wafer segment or remainder of wafer.
	Route for sample dice.
A	Dice acceptable at SEM Inspection.
R	Dice rejected at SEM Inspection.
	“resulting in”

CHART I - SAMPLE SELECTION FROM NON-GLASSIVATED DEVICES

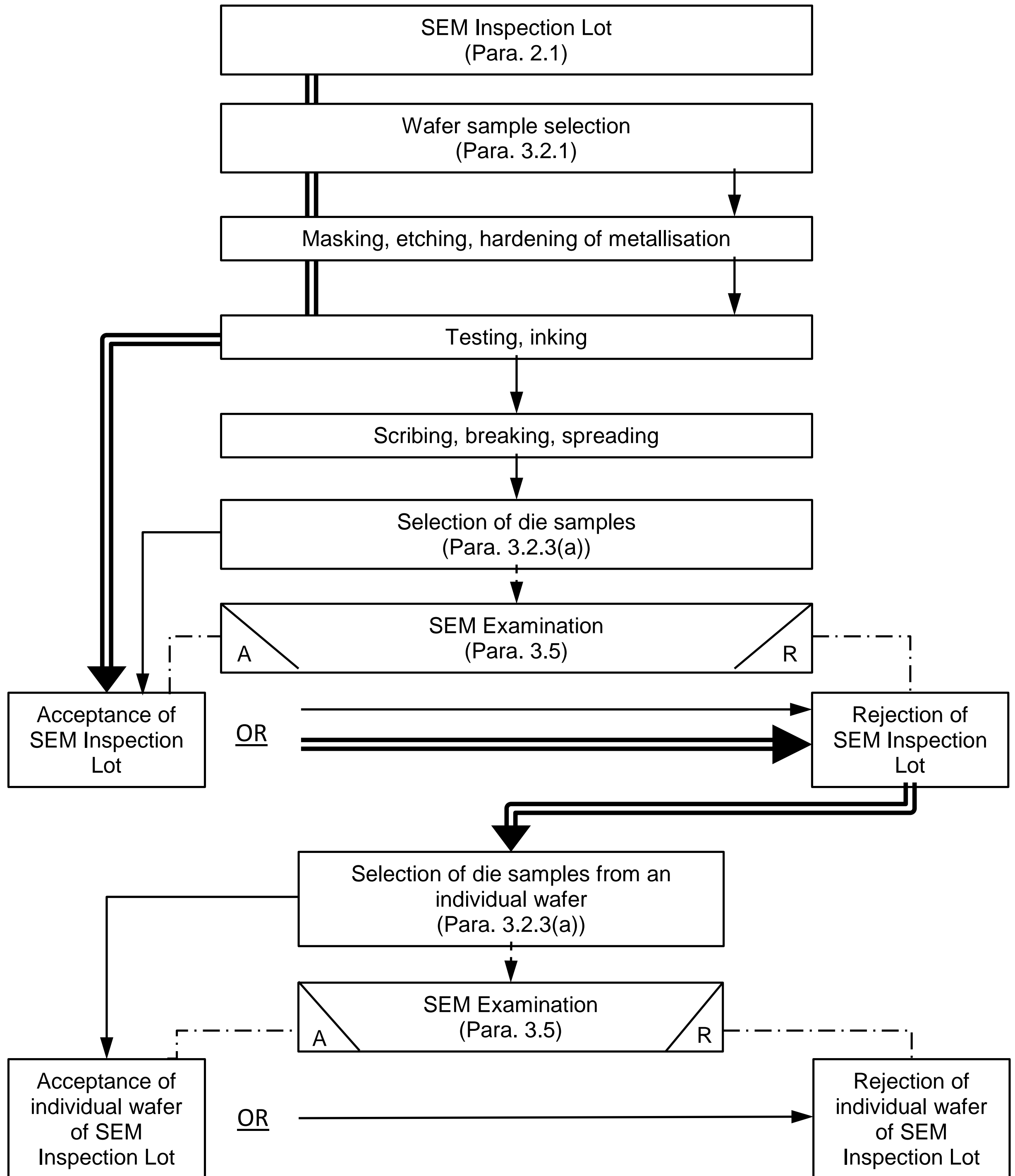


CHART II - SAMPLE SELECTION FROM GLASSIVATED DEVICES

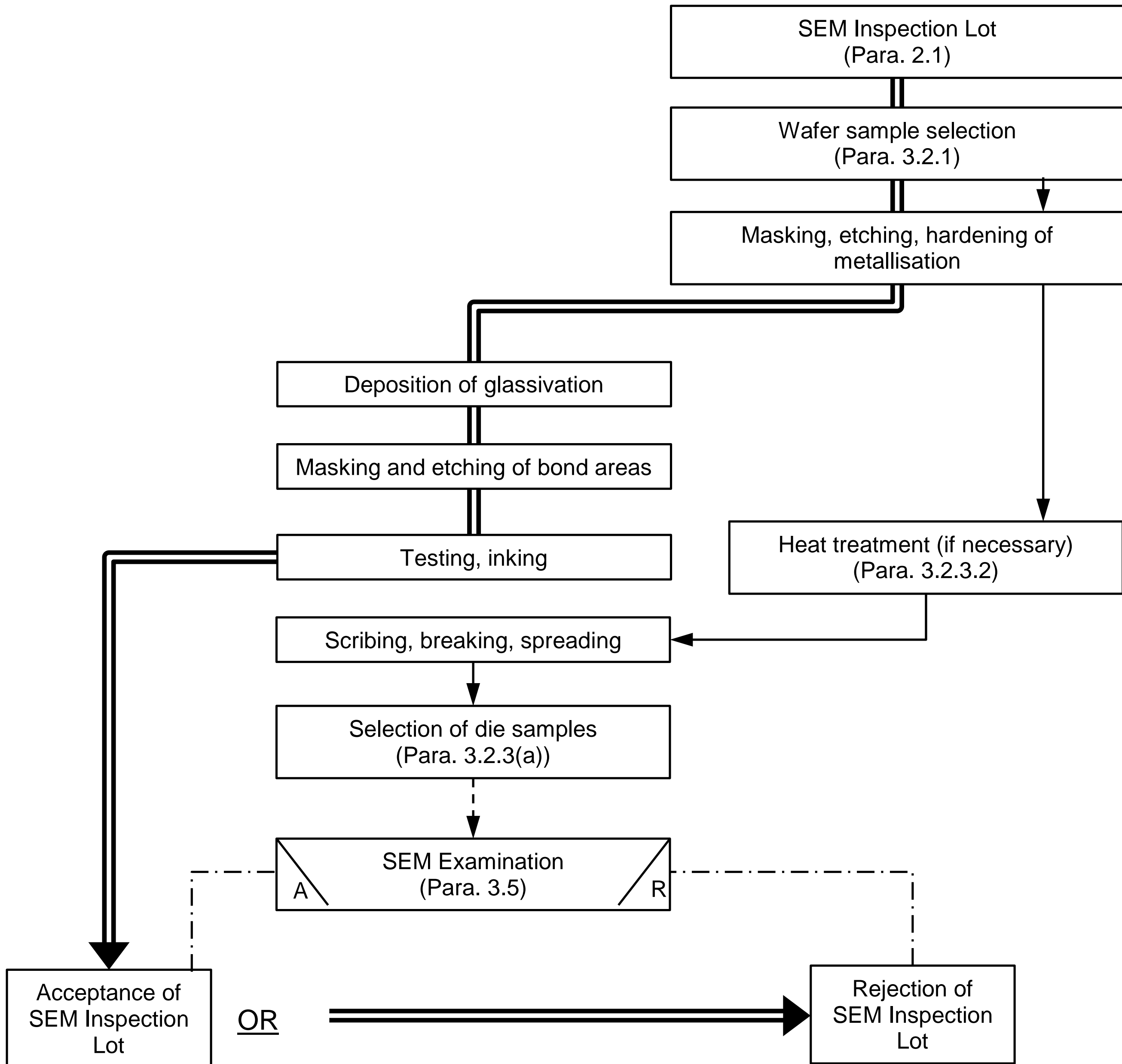


CHART III - SAMPLE SELECTION FROM GLASSIVATED DEVICES

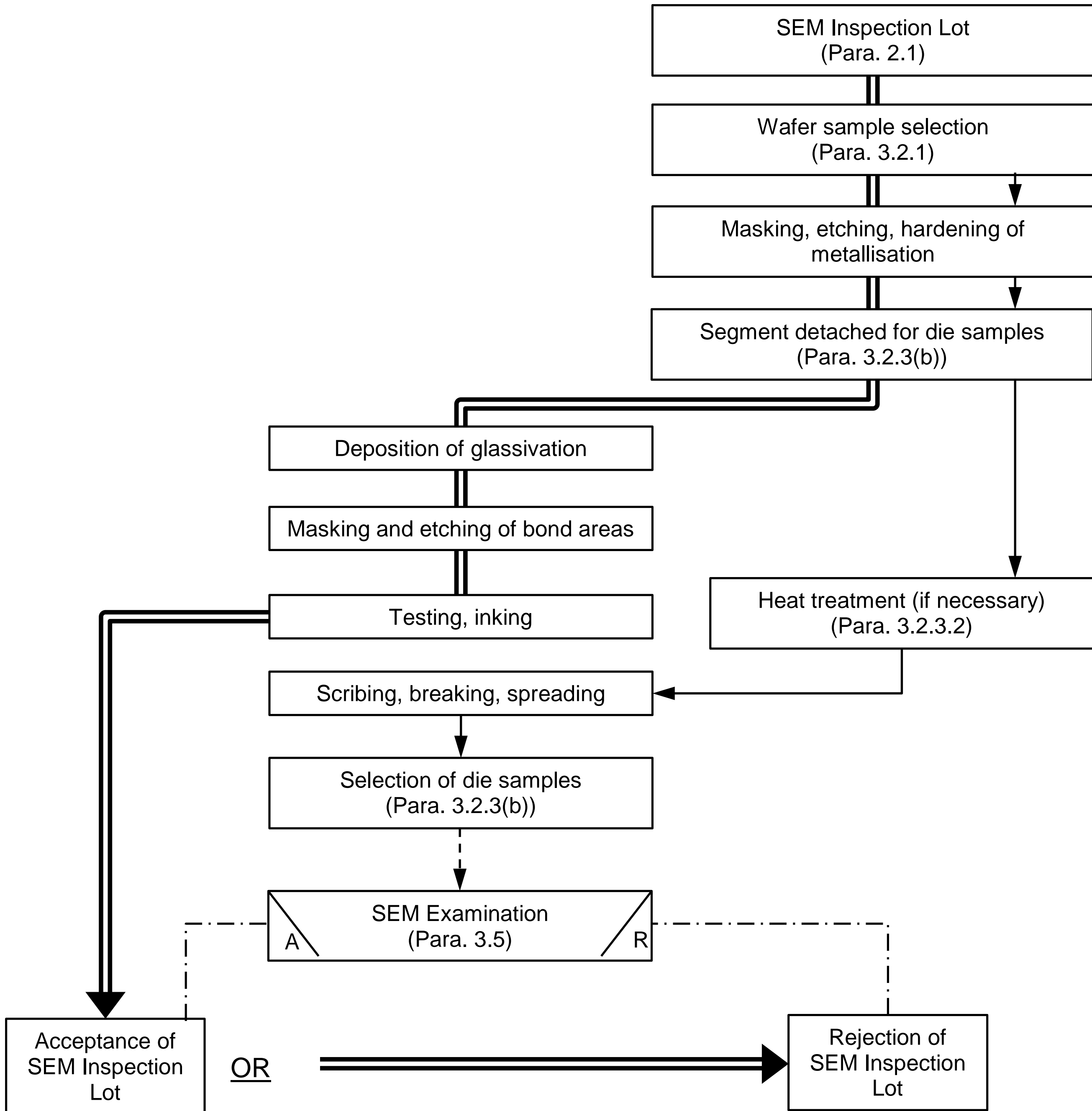


CHART IV - SAMPLE SELECTION FROM GLASSIVATED DEVICES

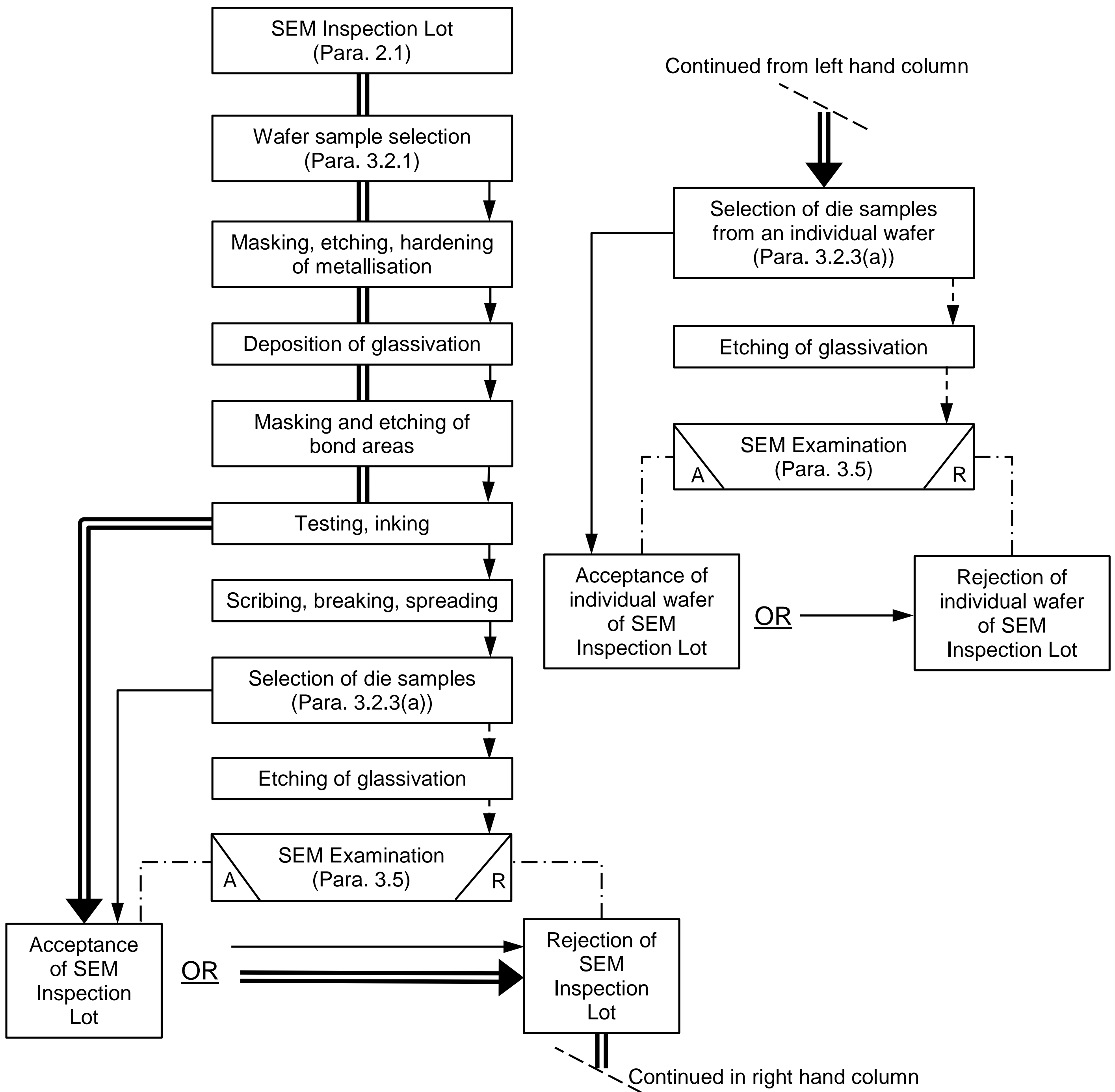


CHART V - SAMPLE SELECTION FROM GLASSIVATED DEVICES (PROCURED WAVERS)

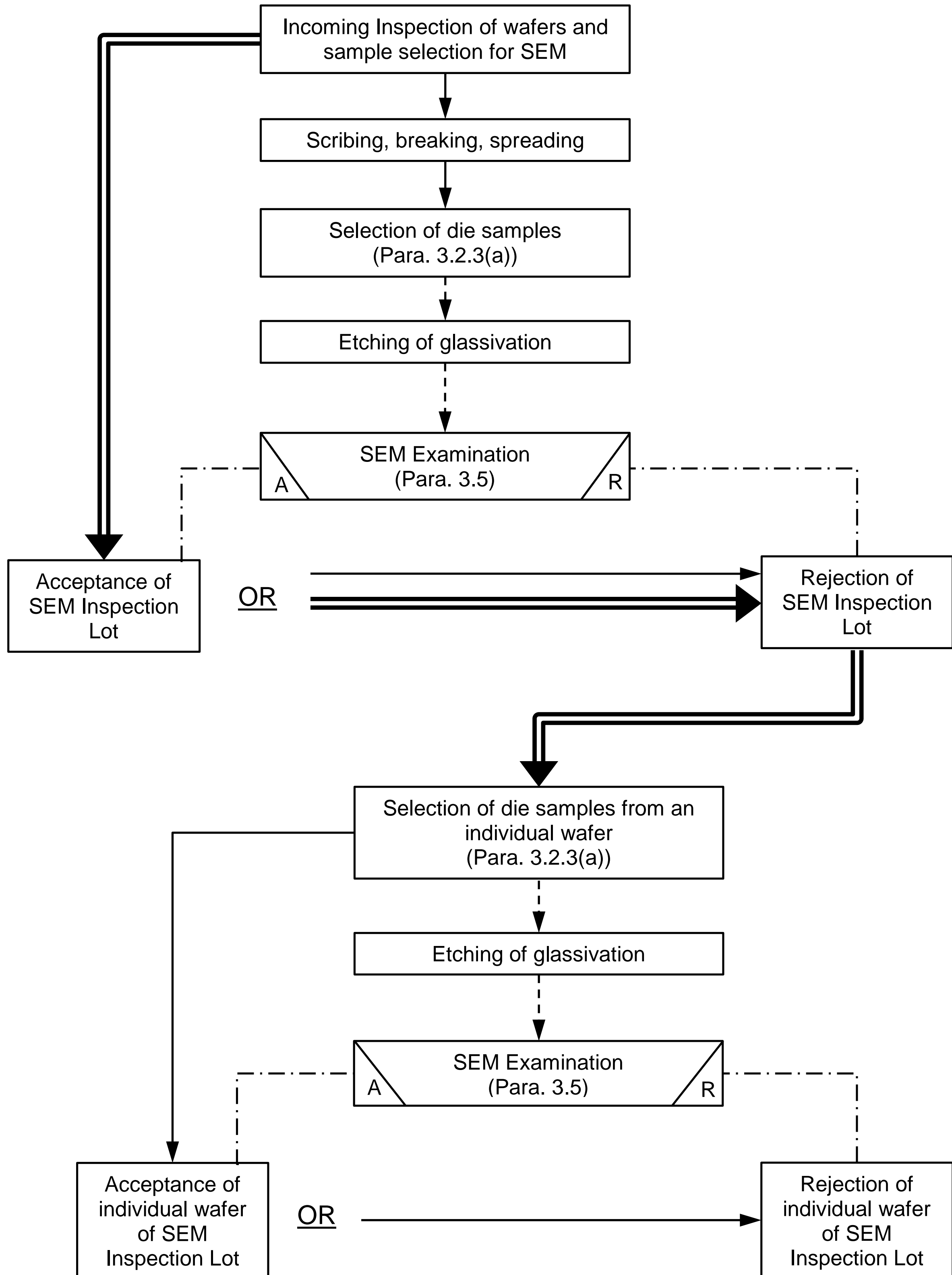


CHART VI - SAMPLE SELECTION FOR MULTI-LEVEL SYSTEMS