INTERNAL VISUAL INSPECTION OF SILICON-BASED NON-MICROWAVE INTEGRATED CIRCUITS

ESCC Basic Specification No. 2049000

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DCR No.	CHANGE DESCRIPTION
838	Specification upissued to incorporate editorial changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification, to be read in conjunction with ESCC Basic Specification No. 20400 (Internal Visual Inspection), contains additional requirements for non-microwave integrated circuits which shall be applied to each device.

Internal visual inspection means visual inspections at all stages of component fabrication, before sealing but also after re-opening of the device as part of a Destructive Physical Analysis (DPA) or Failure Analysis (FA) exercise.

2 GENERAL REQUIREMENTS

2.1 APPLICABILITY

This specification is not intended to cover all aspects of manufacturer specific features and technologies. The in-house manufacturer specification is applicable in the case where no adequate criteria can be found in this document for these specific features and technologies. Any ambiguity or proposed deviation from this specification or between the in-house manufacturer specification and this document shall be referred to the ESCC Executive (for ESCC qualified components) or the customer (for unqualified components) for resolution and approval.

2.2 PROCEDURE

All components shall be submitted to examination in an area where the level of cleanliness and ESD precautions are such that it does not interfere with the results of the intended inspection. The level of cleanliness of the assembly line should act as a guideline.

All items shall be examined in such a manner that a minimum of handling and movement of the component is involved.

Blowing with nitrogen is allowed for the removal of foreign material. All other cleaning processes shall be avoided unless qualified by the manufacturer. After blowing with nitrogen the devices must be re-inspected in order to ensure that the foreign material has been removed. After the pre-cap inspection no further assembly step is allowed, except sealing.

2.3 MOUNTING FIXTURES

Suitable fixtures may be used to assist in the inspection process provided they do not in themselves cause damage to the device.

2.4 MAGNIFICATION

"High magnification" inspection is dedicated to die inspection and shall be performed perpendicular to the die surface.

"Low magnification" inspection is dedicated to assembly inspection and shall be performed within a suitable angle with either a monocular, binocular, or stereo microscope with the device under sufficient illumination.

"High magnification" inspection should be performed prior to "Low magnification" inspection in order to ensure that no damage caused by the lens has occurred.

When necessary, SEM data on representative features of the circuit from the relevant process and wafer lot that are provided by the manufacturer may support the visual inspection.

The following magnifications are given for guidance only. For small features, or where additional verification is required, increased magnification shall be used, if considered necessary.

TABLE 1 - MAGNIFICATION GUIDANCE

Lithography dimension	HIGH MAGNIFICATION	LOW MAGNIFICATION
> 0.8 µm	100X - 200X	30X - 60X
0.5 to 0.8 µm	200X - 500X	
< 0.5 µm	200X - 1000X	

3 DETAILED REQUIREMENTS

3.1 GENERAL

The device shall be examined in a suitable sequence of inspections within the recommended magnification range to determine compliance with the requirements of this document. Where criteria are intended for a specific structure, process or technology it has been indicated.

If during pre-cap inspection, a large number of devices are rejected mainly because of a single criterion listed within this specification (repetitive cause of rejection), corrective actions have to be taken as mutually agreed between Manufacturer and Customer.

3.2 SEQUENCE OF INSPECTION

The order in which the criteria are presented is not a required order of examination and can be varied at the discretion of the Manufacturer, or Inspector.

The inspection criteria that cannot be verified after mounting shall be checked prior to attachment of the die.

3.3 DEFINITIONS

- Acceptable Observation
  The description of a visual anomaly that has no impact on reliability/functionality and/or is only of cosmetic nature and is acceptable for ICs. Acceptable Observations are listed at the end of the list of rejection criteria of each specific subsection under the header 'Acceptable Observation' and each single observation contains the word 'accept', 'acceptable' or 'accepted'.
- Active Circuit Area
  All areas of functional circuit elements, operating metallisation or any connected combinations, excluding ground planes, bare isolating substrates and test structures.
- Air Bridge
  A raised layer of metallisation used for interconnection that is isolated from the surface of the semiconductor and/or passivation material.
- Backside Pattern
  The backside metallisation often has to be structured to create sawing grids which avoid metal peeling or lifting effects during sawing. In the case of a structured backside metallisation the die attach material does not cover the whole chip area and the die attach fillet will usually not be visible during vertical visual inspection.
- Block Resistor
  A thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and which shall be identified in the relevant manufacturer documentation.
- Chip-out
  A chip-out is any section of the die which has broken away from the main body of the die.
- Conductive Material
  Any extraneous material that cannot be clearly identified to be non-conductive.
- Contact Via
  The via where dielectric material is etched away in order to expose the Under Bump Metallisation (UBM) on the bond pads or solder bump attach pads.
- Contact Window
  An opening in the passivation, usually covered by metallisation, where electrical contact is made with an underlying layer.
- Crack
  A crack is a fracture of the relevant material that can extend through or partly through the thickness of the material.
- Crazing
  The presence of numerous minute surface cracks in the referenced material.
- Crystallographic Defect
  A discontinuity of the substrate including pits, screws, mismatches and slip dislocations.
- Detritus
  Fragments of original or laser modified resistor material remaining in the kerf.
- Dielectric Isolation
  Electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolation barrier.
- Diffusion Well
  A volume (or region) formed in a semiconductor material by a diffusion process (n or p type) and isolated from the surrounding semiconductor material by a n-p or p-n junction or by dielectric material (dielectric isolation, coplanar process, SOS, SOI).

- Down-bonding
  A wire bonding operation carried out from a higher to a lower level.
- Flip Chip
  A chip that is intended to be mounted upside down with the contact pads directly connected to the package posts by means of solder bumps.
- Foreign Material
  Any material that is foreign to the microcircuit or package, or any non-foreign material that is displaced from its original or intended position within the microcircuit package. Foreign material shall be considered as attached when a gas blow of nitrogen cannot remove it. Foreign material shall be considered as embedded in the glassivation when there is evidence of colour fringing around the periphery of the foreign material and it cannot be removed by a gas blow of nitrogen.
- Functional Circuit Elements
  Diodes, transistors, cross-unders, capacitors, and resistors.
- Gate Metallisation Length
  Smallest dimension of the gate metallisation (in the direction from source to drain).
- Gate Oxide
  The oxide, or other dielectric, that separates gate metallisation (or other material used for the gate electrode) from the channel of MOS structures.
- Glassivation
  The top layer(s) of insulating material that covers the active circuit area including metallisation, except bonding pad areas.
- Glassivation/Passivation Cracks
  Fissures in the glassivation/passivation layer resulting from stress release, poor adhesion, mechanical and thermal stress.
- Hybrid Microcircuit
  A microcircuit consisting of elements which are a combination of film microcircuit and semiconductor types, or a combination of one or both types with discrete parts. Hybrids do not fall within the scope of this specification but are defined to clarify the limits of the document.
- Inverted Mounting
  A technique whereby thickened and/or extended bonding pads enable upside down mounting on a suitable substrate, such as thin or thick film circuit.
- Junction
  The outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material. An active junction is any p-n junction intended to conduct current during normal operation of the circuit element (i.e. collector to base).
- Junction Area
  The core region of transistors and diodes (i.e. FET: the gate channel; bipolar transistor: region between emitter finger and base/collector contact; diode: region between p and n contact).
- Kerf
  Test pattern onto the scribe line that can be removed by trimming or scribing or for laser trimmed test resistors the pattern resulting from laser trimming.
- Line of Separation
  The visible distance or space between two features that are observed not to touch at the magnification in use.

- Metallisation Non-adherence
  Unintentional separation of material from an underlying substance, excluding air bridges, and undercutting by design.
- Metal Plug
  Feature which allows the interconnection of two consecutive metallisation levels and patterned separately from these metal layers during an intermediate step.
- Metal Via
  Feature which allows the interconnection of two consecutive metallisation levels and patterned simultaneously with the second metal layer.
- Multilayered Metallisation (Conductors)
  A metal layer which for technological reasons (adhesion, diffusion barrier...) is formed by the superposition of two or more different material layers (such as Ti/Al) not isolated from each other by insulating material. The term sandwiched metal layer is commonly used to describe such a structure.
- Multilevel Metallisation (Conductors)
  Two or more layers of metal or any other material used for interconnections that are isolated from each other by insulating material (also referred to as interlevel dielectric).
- Narrowest Resistor Width
  The narrowest portion of a given resistor prior to trimming.
- Operating Metallisation (Conductors)
  All metal or any other material used for interconnection except metallised scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.
- Original Width
  The width dimension or distance that is intended by design (e.g. original metal width, original diffusion width, original beam width, etc.).
- Package Post
  A generic term used to describe the bonding location on the package.
- Passivation
  A layer of insulating material that covers the active circuit area including metallisation.
- Passivation Step
  An abrupt change of level of the passivation, such as a contact window, or operating metallisation cross-over.
- Peripheral Metal
  All metal that lies immediately adjacent to, or over, the scribe grid.
- Pit
  Hole, crater or depression affecting the surface of a layer.
- Probemark
  Scratch on the surface of the metallisation as a result of electrical testing of the die.
- Rebond
  Rebond refers to a second bond made to replace the original bonded wire.
- Redistribution Layer (RDL)
  Layer added to original wafer/die surface to allow for the redistribution of bond pads into a format more suitable to flip chip.
- Scratch
  Any mechanical defect, discontinuity or tooling mark in or on the metallisation or glassivation/passivation.

- Scribe Line
  Area that is intended for scribing the dies.
- Shooting Metal
  Defined as metal (e.g. Aluminium) expulsion of various shapes and lengths from under the wire bond at the bonding pad interface.
- Shunt Link
  One path of a resistor adder network implementing optional resistor values by open trimming of selected resistor paths.
- Solder ball
  Solder ball or sphere attached to the UBM through the contact via after a re-flow process.
- Solder Bump
  Solder that is either electroplated or screened into the photo resist opening. After the photo resist is removed the solder resembles a bump before it is reflowed into ball or sphere.
- Substrate
  The supporting structural material into and/or upon which the passivation, metallisation and circuit elements are placed.
- Substrate Crack
  A crack is a fracture of a die that can extend through or partly through the thickness of the die or remain parallel to the surface of the die.
- Thick Film
  A thick film is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.
- Thin Film
  A thin film is conductive, resistive or dielectric material, 5µm or less in thickness, that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.
- Under Bump Metallisation (UBM)
  Metals deposited on top of the aluminium bond pads or on the solder bump pads that enhance wetting and protect against intermetallic reactions between the solder and the original metal on the pads.
- Up-bonding
  A wire bonding operation carried out from the die up to the post.
- Void
  Any region in the metallisation, glassivation / passivation or die attach material not caused by a scratch, where there is a complete absence of the relevant material within the designed areas and underlying material is exposed.
- Whisker
  A wire residue resulting from the friction of wire bonding equipment.

4 INSPECTION CRITERIA

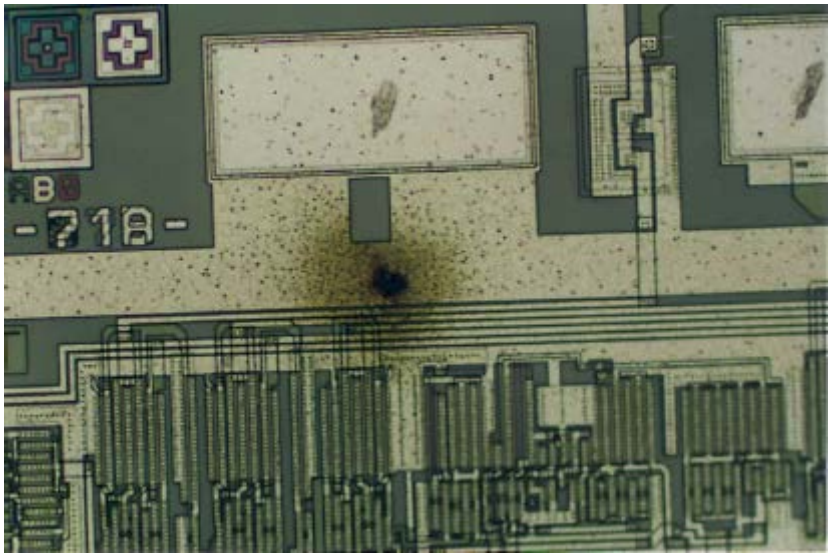
A component shall be rejected if it exhibits one or more of the defects listed within this specification.

4.1 METALLISATION CRITERIA

4.1.1 General Metallisation Defects

(a) Evidence of metallisation corrosion.

FIGURE 1 - EVIDENCE OF METAL CORROSION



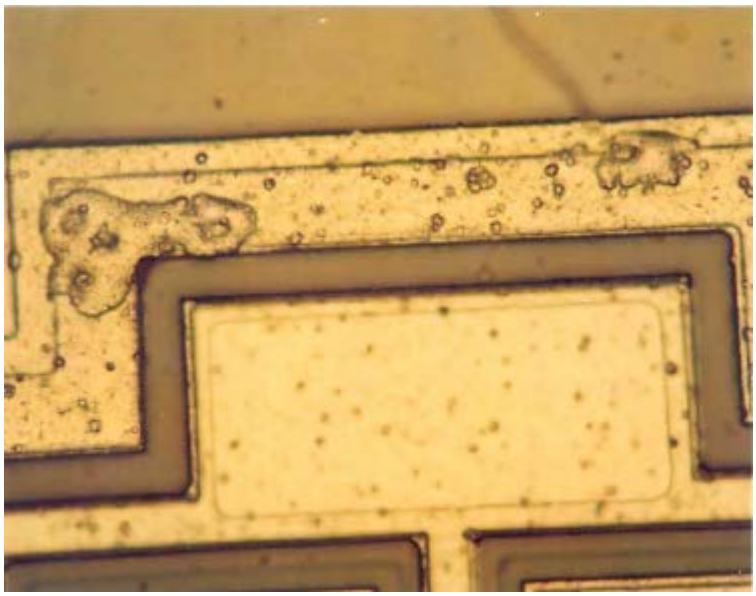
NOTE TO FIGURE 1

1. REJECT: Evidence of metal corrosion. Para. 4.1.1(a) refers.

(b) Metallisation having any discoloured localised area (electroplated metal lines excluded) shall be closely examined and shall be rejected unless the manufacturer can present during the inspection an investigation result demonstrating that the observations have only a harmless effect.

(c) Evidence of metallisation lifting, peeling or blistering.

FIGURE 2 - EVIDENCE OF METALLISATION BLISTERING



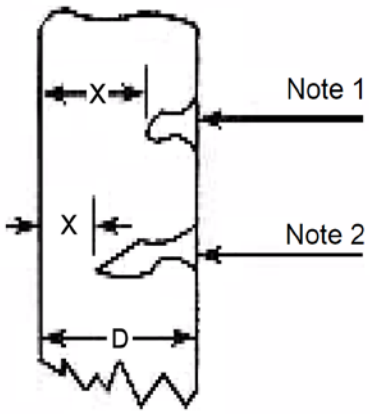
NOTE TO FIGURE 2

1. REJECT: Evidence of metallisation blistering. Para. 4.1.1(c) refers.

4.1.2 Metallisation Scratches

(a) Scratch in the metallisation excluding bonding pads and passivation step coverage that does not expose any underlying layer, passivation or substrate and leaves <50% of the original metal width undisturbed.

FIGURE 3 - SCRATCH CRITERIA FOR METALLISATION LAYERS

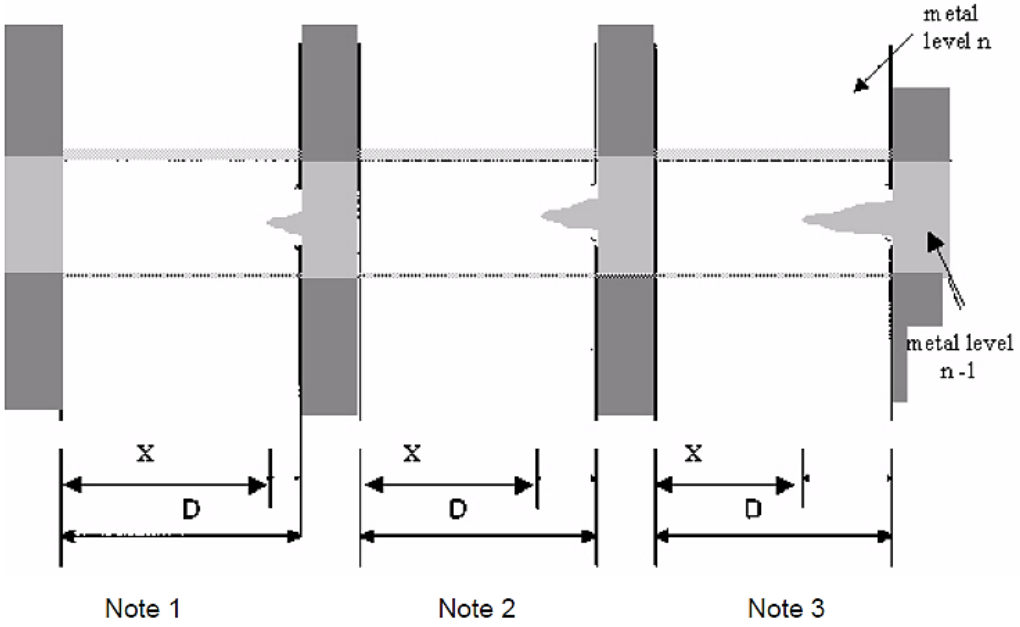


NOTES TO FIGURE 3

1. ACCEPT: Scratch not exposing any underlying layer where the remaining undisturbed metal width X is >50% of the original metal width D. Para. 4.1.2(a) refers.
2. REJECT: Scratch not exposing any underlying layer where the remaining undisturbed metal width X is <50% of the original metal width D. Para. 4.1.2(a) refers.

(b) Scratch in the metallisation over a passivation step that leaves <75% of the original metal width at the step undisturbed.

FIGURE 4 - METALLISATION SCRATCH OVER PASSIVATION STEP

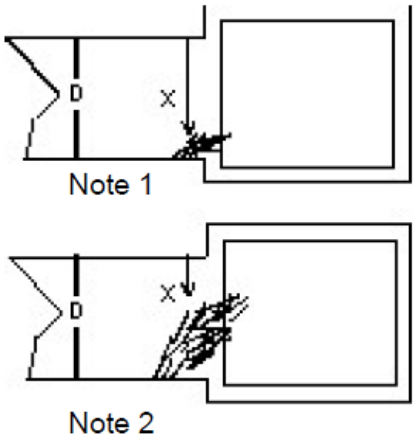


NOTES TO FIGURE 4

1. ACCEPT: Scratch leaving >75% of original metal width undisturbed. Para. 4.1.2(b)) refers.
2. ACCEPT: minimum acceptable scratch leaving 75% of original metal width undisturbed. Para. 4.1.2(b) refers.
3. REJECT: Scratch leaving <75% of original metal width undisturbed. Para 4.1.2(b) refers.

(c) Scratch in the bonding pad or fillet area that does not expose underlying layer, passivation or substrate and reduces the metallisation path width connecting the bond to the interconnecting metallisation to <50% of the narrowest entering interconnect metallisation stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

FIGURE 5 - SCRATCH IN BOND PAD INTERCONNECTION AREA

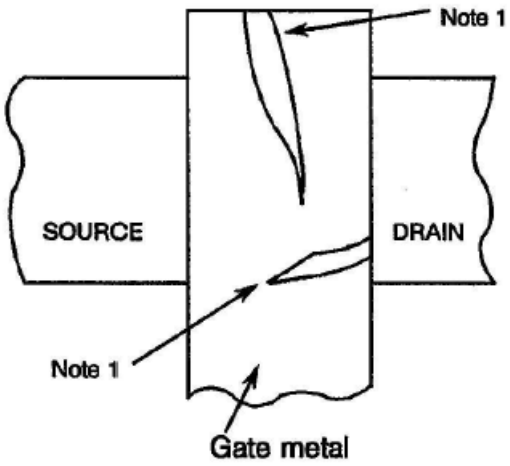


NOTES TO FIGURE 5

1. ACCEPT: Scratch where the remaining undisturbed metal width X is >50% of the original metal width D. Para. 4.1.2(c) refers.
2. REJECT: Scratch where the remaining undisturbed metal width X is <50% of the original metal width D. Para. 4.1.2(c) refers.

(d) Scratch in the metallisation, over the gate oxide.

FIGURE 6 - MOS SCRATCH CRITERIA

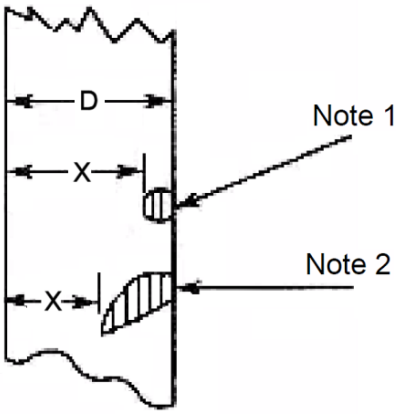


NOTE TO FIGURE 6

1. REJECT: Scratch in the metallisation, over the gate oxide. Para. 4.1.2(d) refers.

(e) Scratch in single or multi-layered metallisation excluding bonding pads but including fillet area that exposes underlying metal or passivation anywhere along its length and leaves <75% of the original metal width undisturbed.

FIGURE 7 - SCRATCH EXPOSING UNDERLYING MATERIAL



NOTES TO FIGURE 7

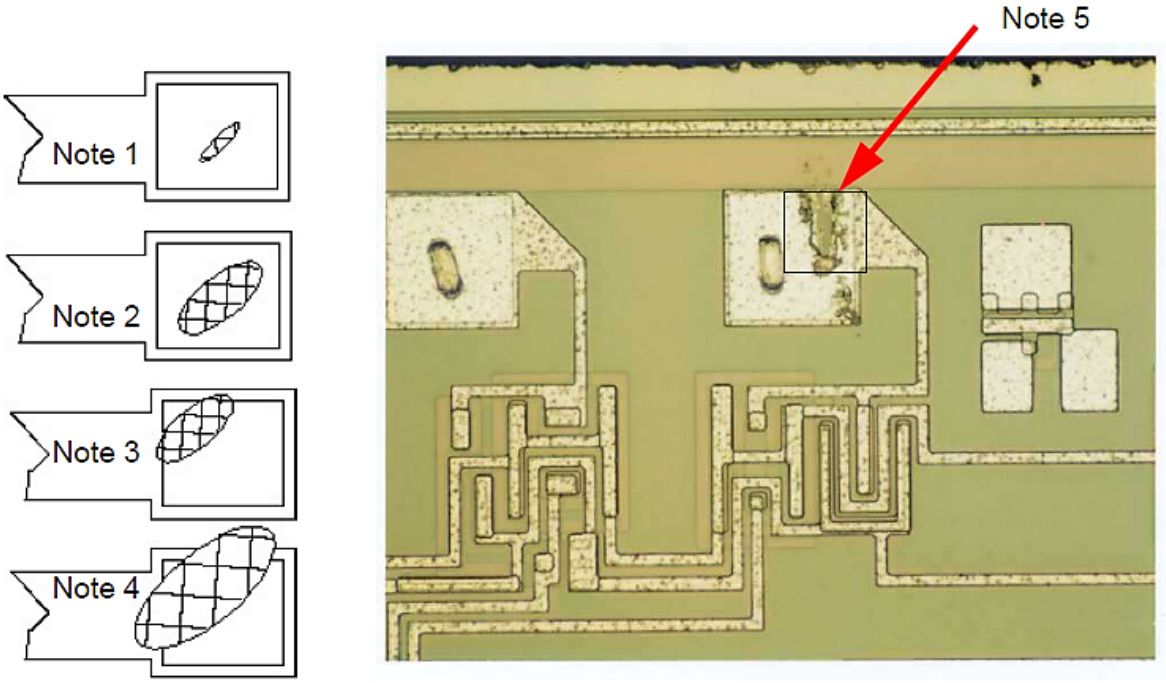
1. ACCEPT: Scratch exposing underlying metal or passivation where the remaining undisturbed metal width X is >75% of the original metal width D. Para. 4.1.2(e) refers.
2. REJECT: Scratch exposing underlying metal or passivation where the remaining undisturbed metal width X is <75% of the original metal width D. Para. 4.1.2(e) refers.

(f) Scratch, probe marks, etc., in the bonding pad area exposing underlying layer material leaving <75% of the unglassivated metallisation area undisturbed.

NOTES:

1. A centred scratch should be regarded as more severe and shall be rejected if >1/8 (12.5%) of the unglassivated bond pad area is disturbed.
2. A reduction of the interconnection path shall be considered according to Para. 4.1.2(c).

FIGURE 8 - SCRATCH, PROBE MARKS IN THE BONDING PAD AREA



NOTES TO FIGURE 8

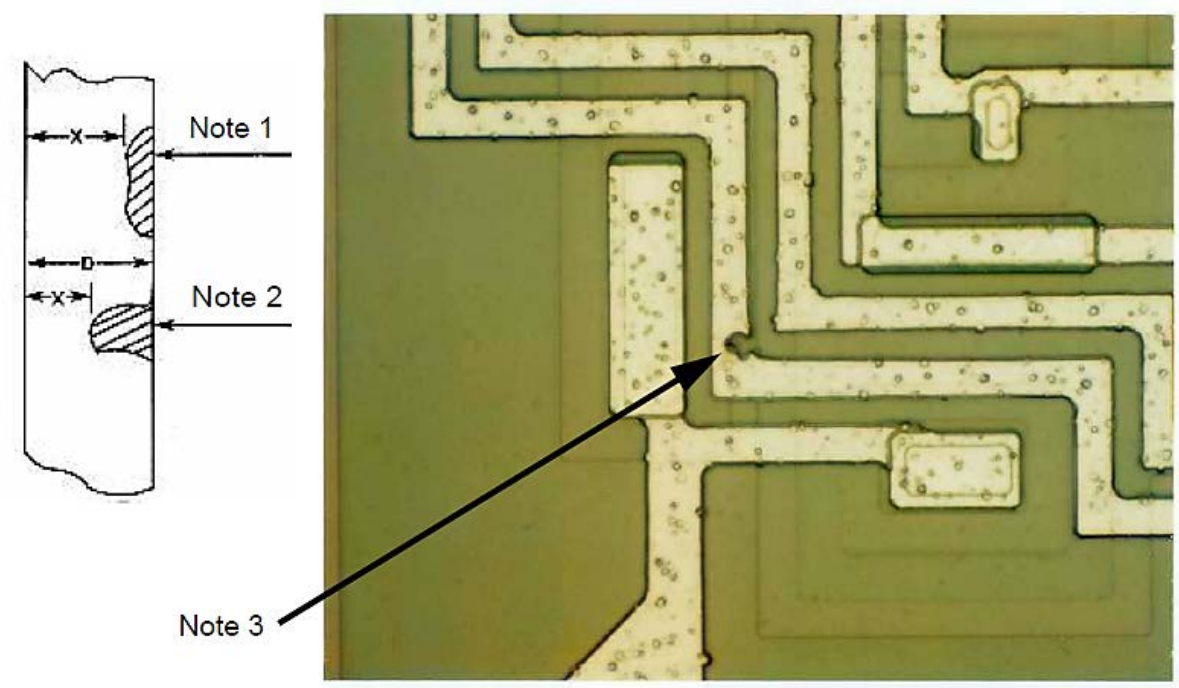
1. ACCEPT: Centred scratch exposing underlying passivation or substrate where <1/8 (12.5%) of the unglassivated bond pad area is disturbed. Para. 4.1.2(f) refers.
2. REJECT: Centred scratch exposing underlying passivation or substrate where >1/8 (12.5%) of the unglassivated bond pad area is disturbed. Para. 4.1.2(f) refers.
3. ACCEPT: Non-centred scratch exposing underlying passivation or substrate where the remaining undisturbed metallisation area is >75% of the pad area. Para. 4.1.2(f) refers.
4. REJECT: Non-centred scratch exposing underlying passivation or substrate where the remaining undisturbed metallisation area is <75% of the pad area. Para. 4.1.2(f) refers.
5. REJECT: Non-centred scratch exposing underlying passivation or substrate where the remaining undisturbed metallisation area is >75% of the pad area but reducing the metallisation path width connecting the bond to the interconnecting metallisation to <50% of the narrowest entering interconnect metallisation stripe width. Para. 4.1.2(c)+(f) refer.

4.1.3 Metallisation Voids

In the case where the defect is generic to the lot, the lot may be accepted if an analysis has been performed on the worst case devices and a report is available during the inspection demonstrating that the current density rules are not compromised.

(a) Void(s) in the metallisation that leaves <75% of the original metal width undisturbed.

FIGURE 9 - METALLISATION VOIDS

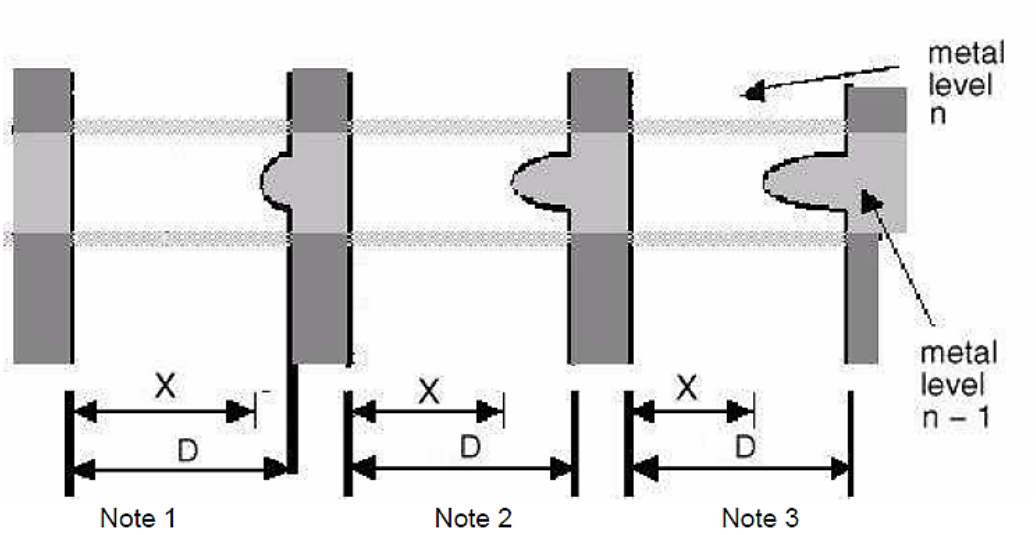


NOTES TO FIGURE 9

1. ACCEPT: Void where the remaining undisturbed metal width X is >75% of the original metal width D. Para. 4.1.3(a) refers.
2. REJECT: Void where the remaining undisturbed metal width X is <75% of the original metal width D. Para. 4.1.3(a) refers.
3. REJECT: Void where the remaining undisturbed metal width is <75% of the original metal width. Para. 4.1.3(a) refers.

(b) Void(s) in the metallisation over a passivation step that leaves <75% of the original metal width, at the step, undisturbed.

FIGURE 10 - METALLISATION VOID OVER PASSIVATION STEP

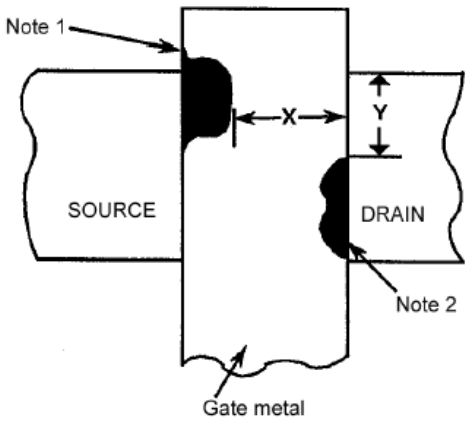


NOTES TO FIGURE 10

1. ACCEPT: Void where the remaining undisturbed metal width X is >75% of the original metal width D. Para. 4.1.3(b) refers.
2. ACCEPT (minimum): Void where the remaining undisturbed metal width X is about 75% of the original metal width D. Para. 4.1.3(b) refers.
3. REJECT: Void where the remaining undisturbed metal width is <75% of the original metal width. Para. 4.1.3(b) refers.

(c) Void(s) that leave <75% of the metallisation area over the gate oxide undisturbed.
(d) Void(s) in the metallisation over the gate oxide that leaves <75% of the gate metallisation length (X) or width (Y) between source and drain diffusions undisturbed.

FIGURE 11 - MOS VOID CRITERIA



NOTES TO FIGURE 11

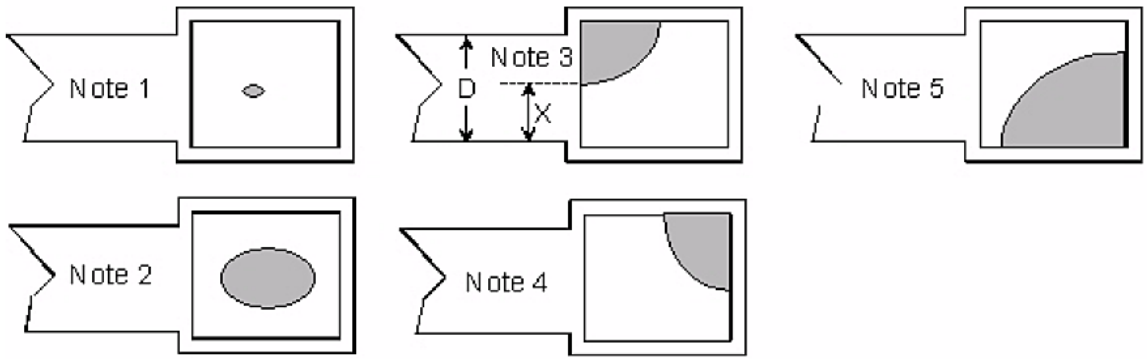
1. REJECT: Void in the metallisation over the gate oxide where the remaining undisturbed gate metal length X is <75% of the original gate metallisation length. Para. 4.1.3(d) refers.
2. REJECT: Void in the metallisation over the gate oxide where the remaining undisturbed gate metal width Y is <75% of the original gate metallisation width. Para. 4.1.3(d) refers.

(e) Void(s) in the bonding pad area that leaves <75% of its original unglassivated metallisation area undisturbed.

NOTES:

1. A centred void should be regarded as more severe for bonding opportunity and shall be rejected if >1/8 (12.5%) of the unglassivated bond pad area is disturbed.
2. Reduction of the interconnection path shall be considered according to Para. 4.1.3(f).

FIGURE 12 - VOIDS IN BONDING PAD AREA

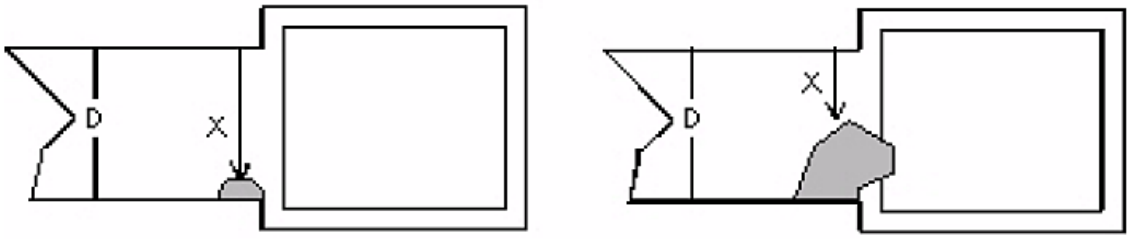


NOTES TO FIGURE 12

1. ACCEPT: Centred void where <1/8 (12.5%) of the unglassivated bond pad area is disturbed. Para. 4.1.3(e) refers.
2. REJECT: Centred Void where >1/8 (12.5%) of the unglassivated bond pad area is disturbed. Para. 4.1.3(e) refers.
3. REJECT: Void where the remaining undisturbed metallisation area is >75% of the pad area but the remaining undisturbed interconnecting metal width X is <75% of the original metal width D. Para. 4.1.3(e) + (f) refer.
4. ACCEPT: Void where the remaining undisturbed metallisation area is >75% of the pad area. Para. 4.1.3(e) refers.
5. REJECT: Void where the remaining undisturbed metallisation area is <75% of the pad area. Para. 4.1.3(e) refers.

(f) Void(s) in the bonding pad or fillet area that reduces the metallisation path width connecting the bond to the interconnecting metallisation to <75% of the narrowest entering metallisation stripe width. If two or more stripes enter a bonding pad, each shall be considered separately. When a fillet area exists, it is considered as part of the entering/exiting metallisation stripe.

FIGURE 13 - VOIDS ON BOND PAD INTERCONNECTING METALLISATION



NOTES TO FIGURE 13

1. ACCEPT: Void where the remaining undisturbed metal width X is >75% of the original metal width D. Para. 4.1.3(f) refers.
2. REJECT: Void where the remaining undisturbed metal width X is <75% of the original metal width D. Para. 4.1.3(f) refers.

4.1.4 Metallisation Probing

Multiple probe marks on a bond pad area are accepted if the criteria contained in Para 4.1.2 are met.

4.1.5 Metallisation Separation

The minimum acceptable separation between two metallisation areas from the same level of metallisation shall be 50% of the original design width at any point, whether caused by smears, photo-lithographic defects or other defects. This criteria is also applicable where the defect is separated from both metallisation areas.

FIGURE 14 - METALLISATION SEPARATION

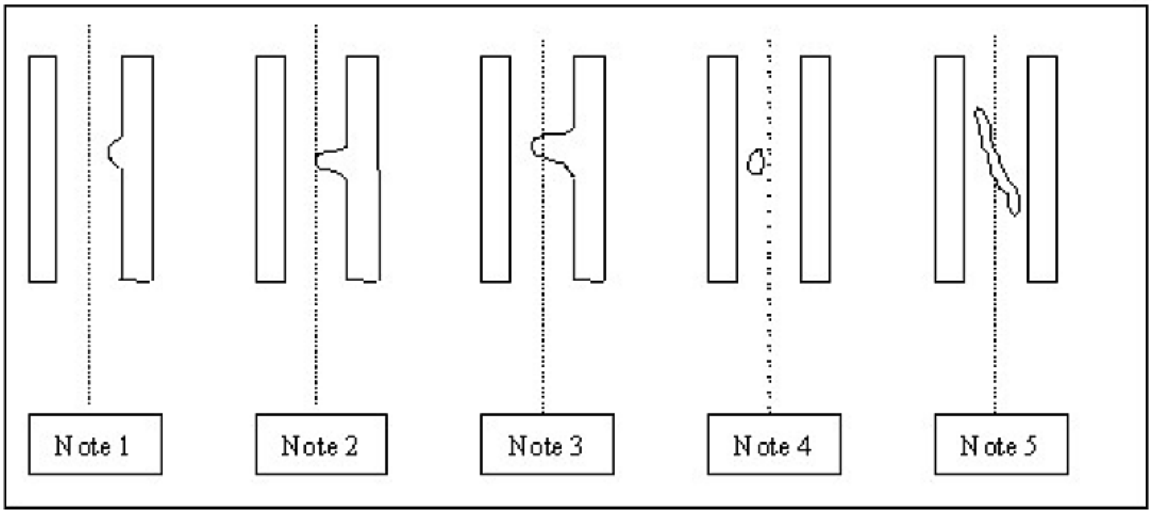
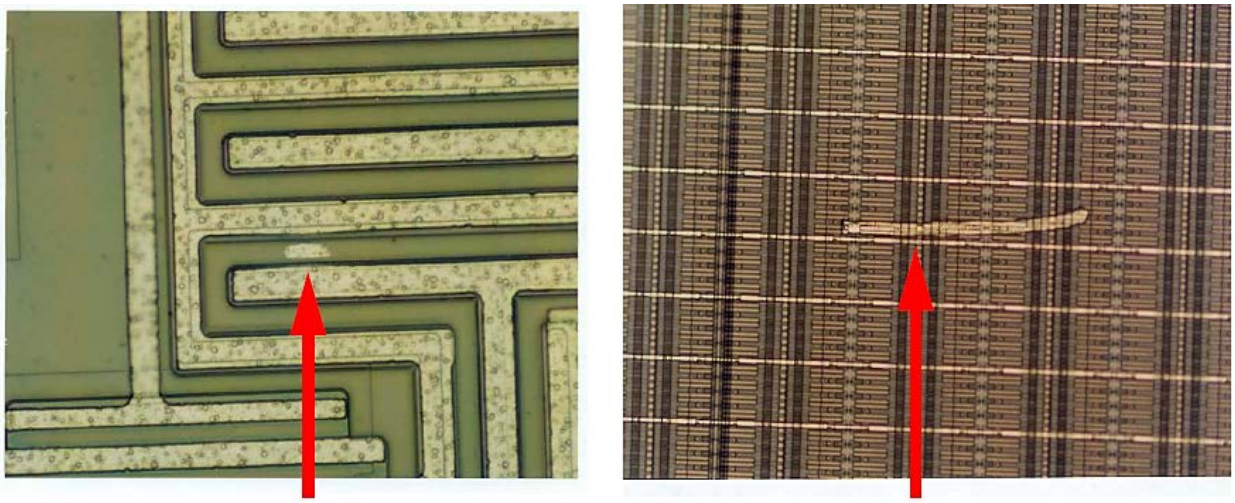


FIGURE 14 – METALLISATION SEPARATION (CONTINUED)



Note 5 Note 5

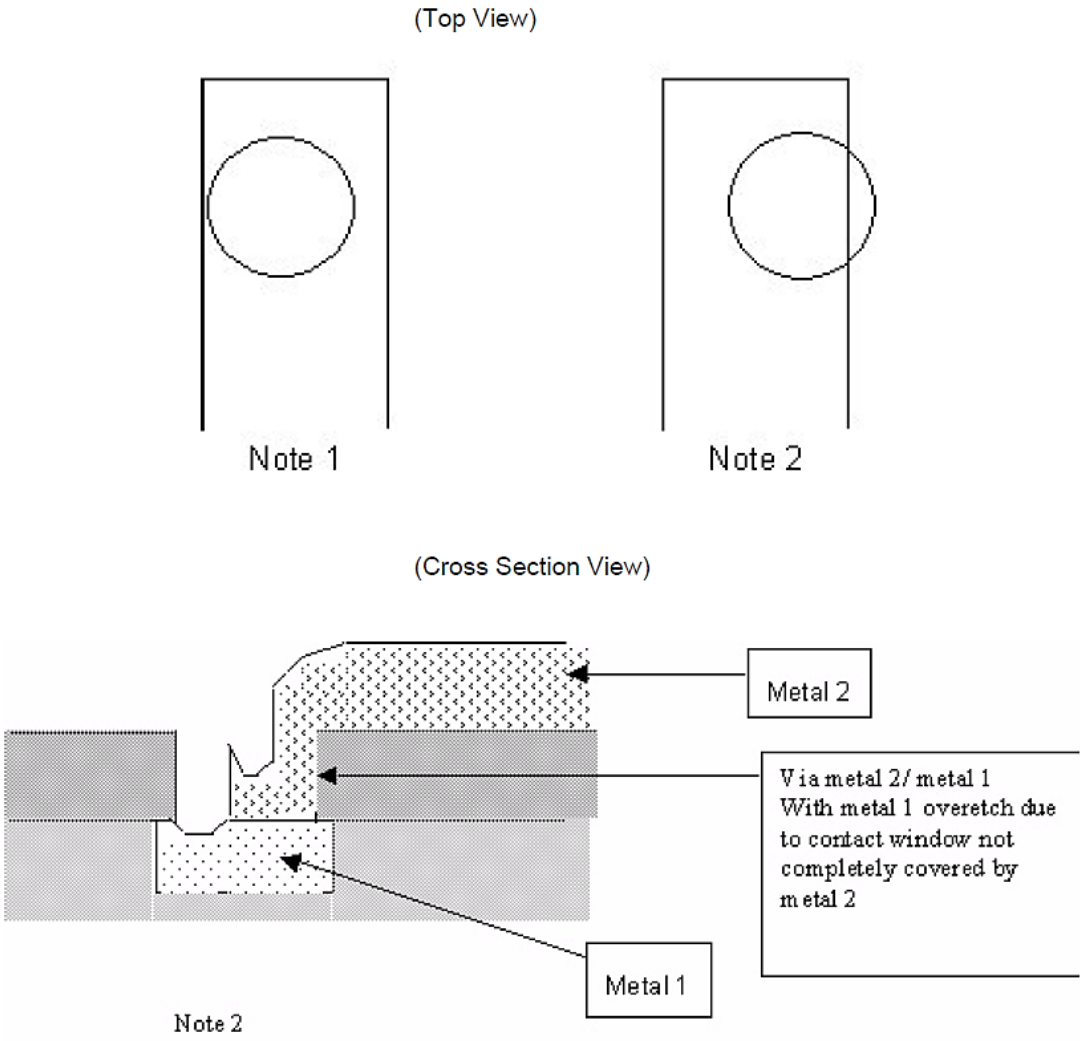
NOTES TO FIGURE 14

1. ACCEPT: remaining separation is >50% of original design width. Para. 4.1.5 refers.
2. ACCEPT: minimum acceptable separation of 50% of original design width. Para. 4.1.5 refers.
3. REJECT: remaining separation is <50% of original design width. Para. 4.1.5 refers.
4. ACCEPT: remaining separation is >50% of original design width. Para. 4.1.5 refers.
5. REJECT: remaining separation is <50% of original design width. Para. 4.1.5 refers.

4.1.6 Metallisation Alignment

(a) Alignment fault such that a contact window opening through passivation is not completely (100%) covered by metallisation where a metal via is applied, except if the Manufacturer has performed an analysis on the worst case devices and provides a report during the inspection demonstrating that the current density rules are not compromised.

FIGURE 15 - METALLISATION ALIGNMENT (METAL VIA)

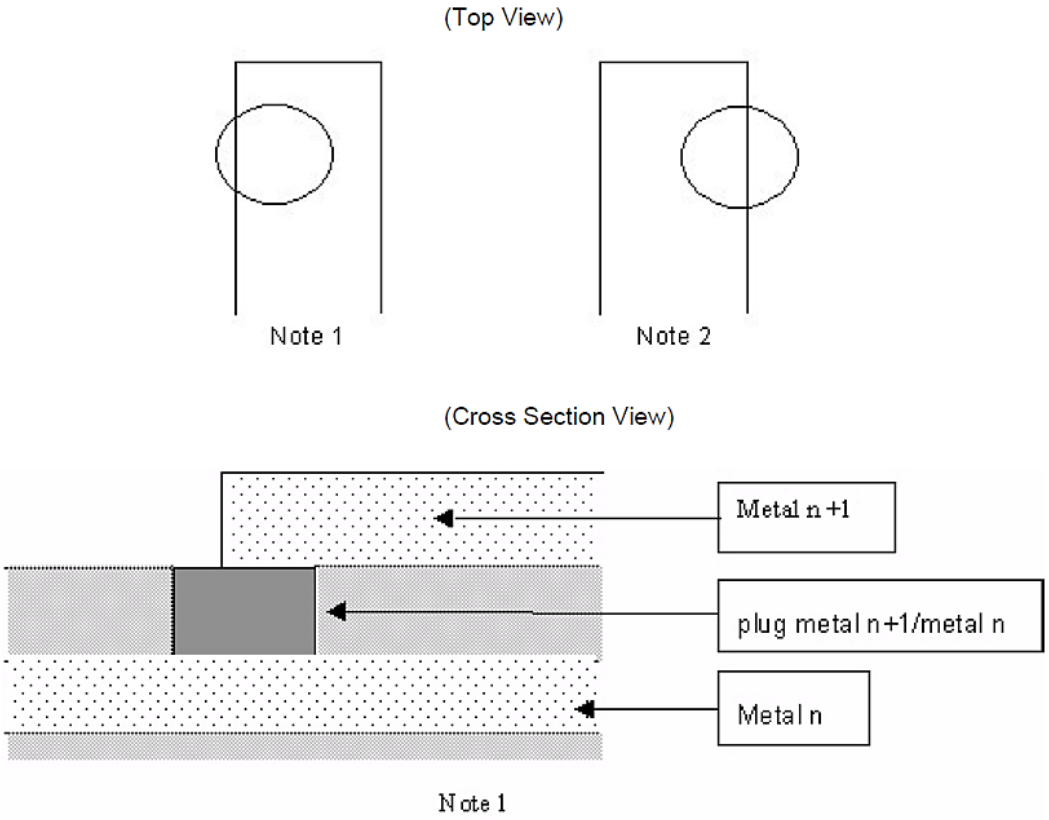


NOTES TO FIGURE 15

1. ACCEPT: Contact window completely covered by metallisation. Para. 4.1.6(a) refers.
2. REJECT: Contact window not completely covered by metallisation. Para. 4.1.6(a) refers.

(b) Alignment fault such that a contact window opening through passivation is <75% covered by metallisation where a metal plug is applied, except if the Manufacturer has performed an analysis on the worst case devices and provides a report during the inspection demonstrating that the current density rules are not compromised.

FIGURE 16 - METALLISATION ALIGNMENT (METAL PLUG)

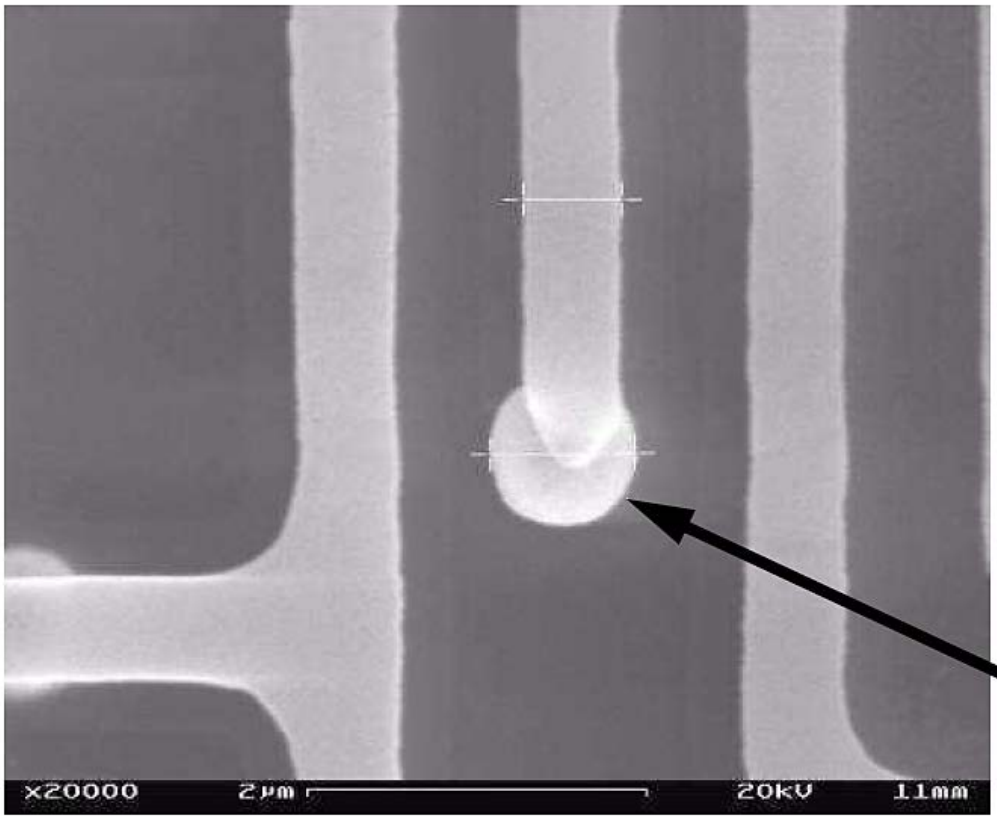


NOTES TO FIGURE 16

1. ACCEPT: Contact window >75% covered by metallisation. Para. 4.1.6(b) refers.
2. REJECT: Contact window <75% covered by metallisation. Para. 4.1.6(b) refers.

(c) Alignment fault such that a contact window opening through passivation is <75% covered by the first level metallisation, except if the Manufacturer has performed an analysis on the worst case devices and provides a report during the inspection demonstrating that the current density rules are not compromised.

FIGURE 17 - METALLISATION ALIGNMENT (FIRST LEVEL METALLISATION)

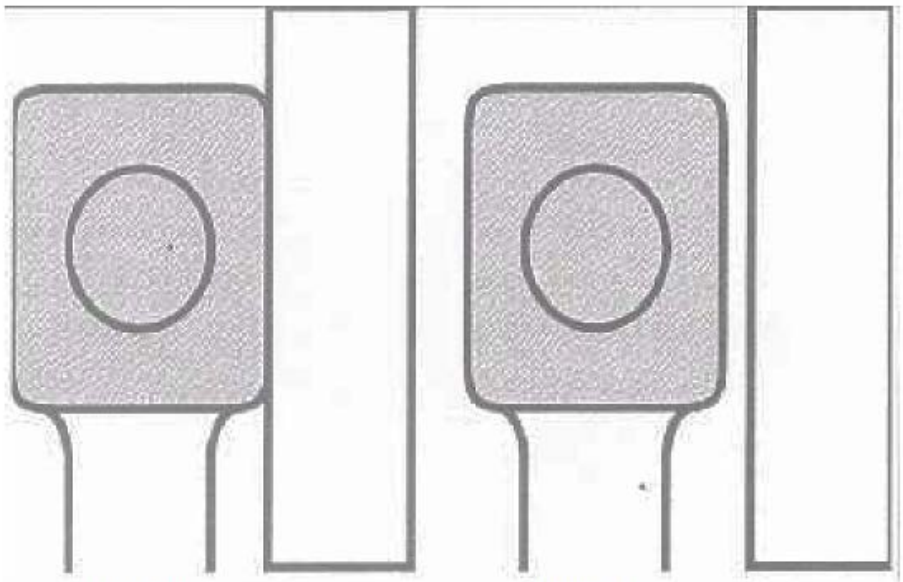


NOTE TO FIGURE 17

1. REJECT: Contact window <75% covered by metallisation. Para. 4.1.6(c) refers.

(d) A metallisation path not intended to cover a contact window and that is not separated from the contact window by a line of separation.

FIGURE 18 - METALLISATION PATH ADJACENT TO A CONTACT WINDOW

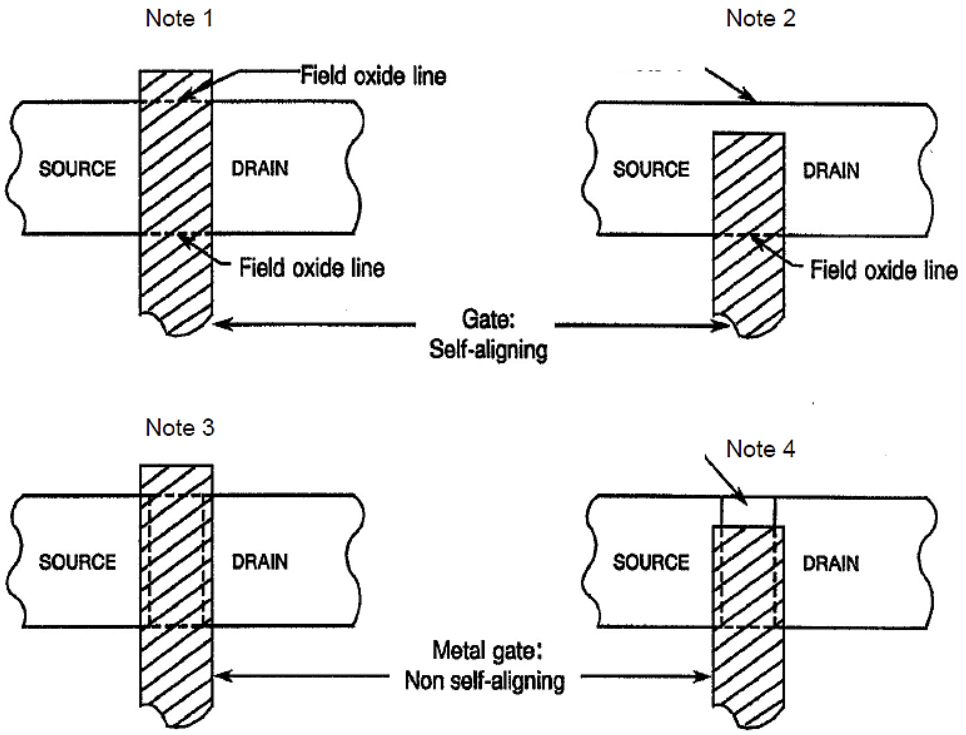


NOTES TO FIGURE 18

1. REJECT: No visible line of separation. Para. 4.1.6(d) refers.
2. ACCEPT: Metallisation path separated from contact window. Para. 4.1.6(d) refers.

(e) Any exposure of the gate oxide, i.e. oxide not covered by gate electrode in the area between source to drain diffusions. Not applicable to sub-micron technology.

FIGURE 19 - MOS GATE ALIGNMENT

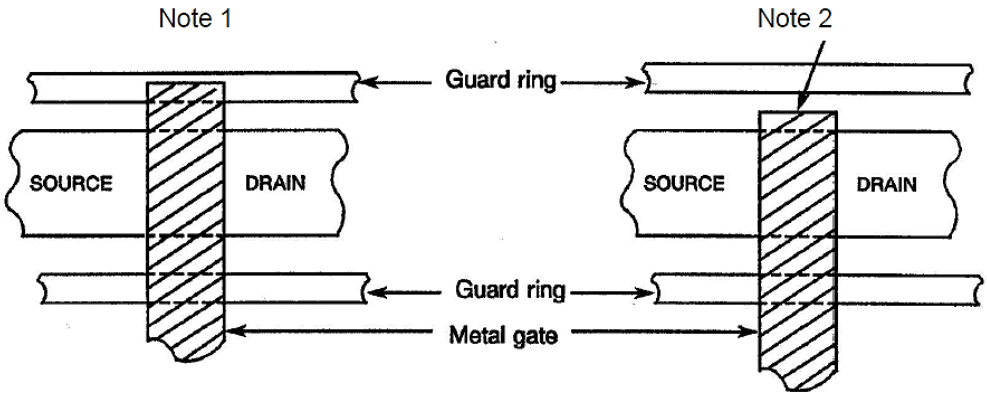


NOTES TO FIGURE 19

1. ACCEPT: Self-aligned Gate well aligned. Para. 4.1.6(e)refers.
2. REJECT: Self-aligned Gate with misalignment. Para. 4.1.6(e) refers.
3. ACCEPT: Non Self-aligned Gate well aligned. Para. 4.1.6(e) refers.
4. REJECT: Non Self-aligned Gate with misalignment. Para. 4.1.6(e) refers.

(f) For MOS structures containing a diffused guard ring, gate metallisation not coincident with, or extending over, the diffused guard ring. Not applicable to sub-micron technology.

FIGURE 20 - MOS GATE ALIGNMENT FOR GUARD RING STRUCTURE



NOTES TO FIGURE 20

1. ACCEPT: Gate coincide with, or extend over, the guard ring. Para. 4.1.6(f)
2. REJECT: Gate does not coincide with, or does not extend over the guard ring. Para. 4.1.6(f) refers.

4.1.7 Backside Metallisation

(a) Evidence of metallisation corrosion.

(b) Metallisation having any discoloured localised area shall be closely examined and shall be rejected unless the manufacturer can present during the inspection an investigation result demonstrating that the observations have only a harmless effect.

(c) Any evidence of metallisation lifting, peeling or blistering.
Note: A saw damaged region of 25µm from the die edge needs to be excluded.

(d) Void(s), or missing metallisation on the backside metallisation (unless by design, die edge excluded), where the defective area is >50% of total backside area or a single void traverses either the length or the width of the semiconductor element and >10% of total backside area.

4.2 DIFFUSION DEFECTS

(a) A diffusion fault that allows bridging between any two diffused areas, any two metallisation areas or any combination thereof not intended by design (See Figure 21).

(b) A diffused resistor path exhibiting a path width reduction with <50% of the original diffusion width remaining (See Figure 21).

(c) Any isolation diffusion that is discontinuous (except isolation walls around unused areas or unused bonding pads) or any other diffused area with <25% of the original diffusion width remaining.

FIGURE 21 - DIFFUSION FAULT

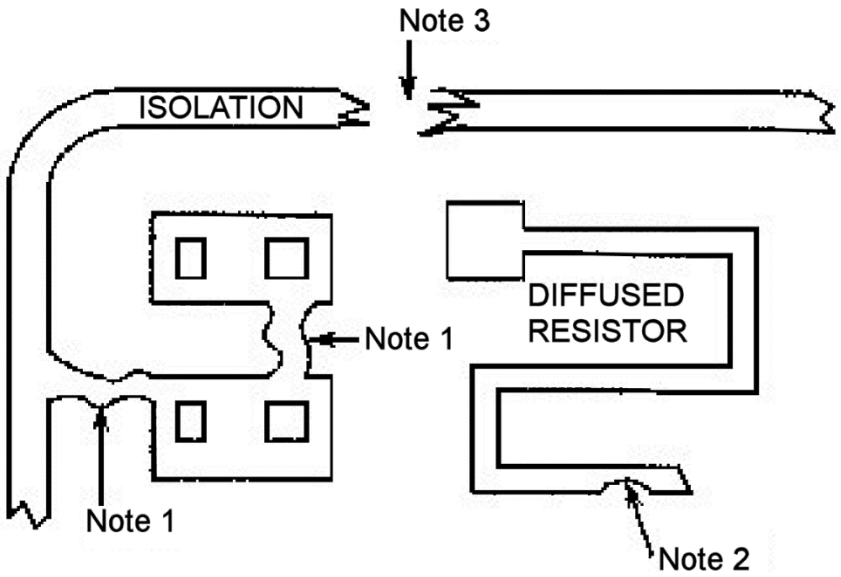
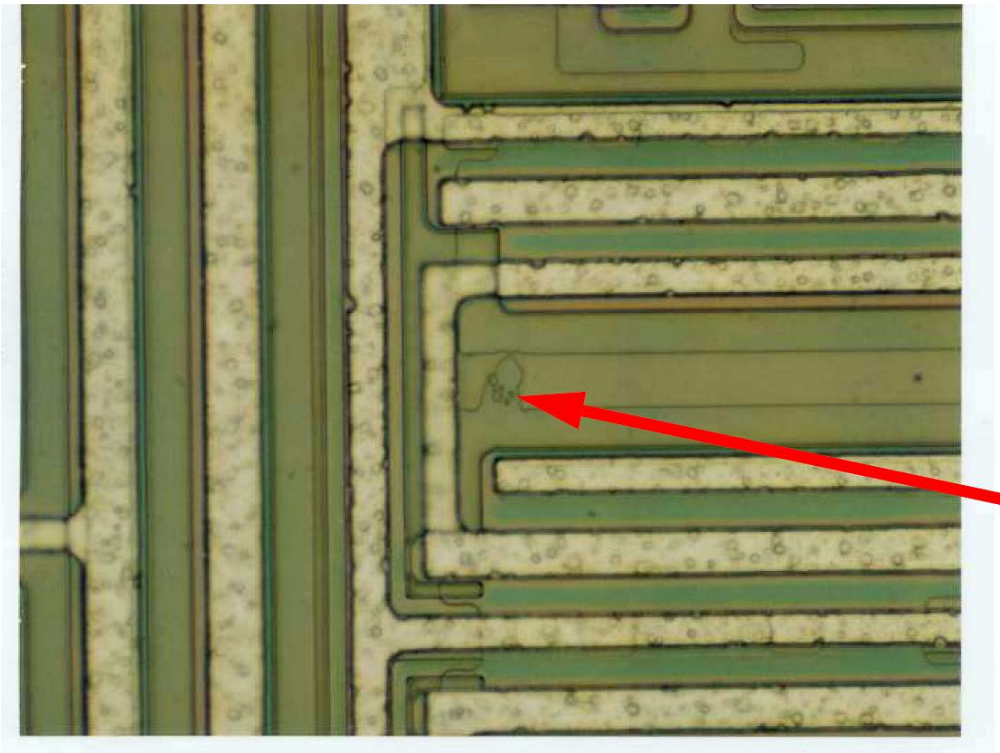


FIGURE 21 – DIFFUSION FAULT (CONTINUED)



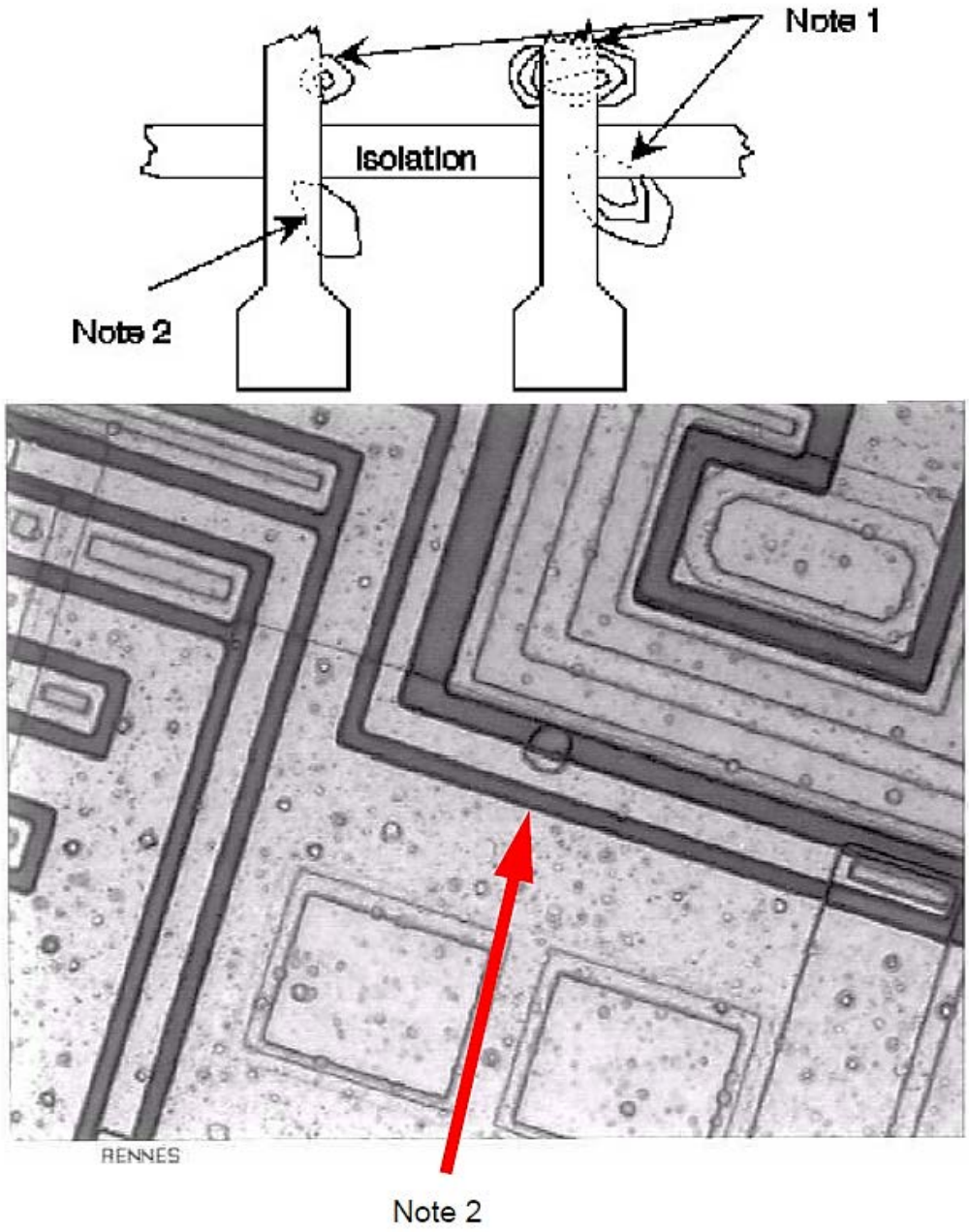
NOTES TO FIGURE 21

1. REJECT: Unexpected bridging between diffused areas. Para. 4.2(a) refers.
2. REJECT: Diffused Resistor with <50% of the original width remaining. Para. 4.2(b) refers.
3. REJECT: Discontinuous isolation diffusion. Para. 4.2(c) refers.

4.3 PASSIVATION DEFECTS

(a) Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallisation. Multiple lines indicate that the fault can have sufficient depth to penetrate down to bare semiconductor material.

FIGURE 22 - PASSIVATION DEFECT



NOTES TO FIGURE 22

1. REJECT: Passivation defect under metallisation, exhibiting multiple lines. Para. 4.3(a) refers.
2. ACCEPT: Evidence of passivation hollow. Para. 4.3(1) refers.

(b) A passivation fault which may cause unintentional opens or shorts in the active area.
(c) Pinholes on any junction or active area.
(d) A break which causes a discontinuous annular stopper, isolation or guard ring.

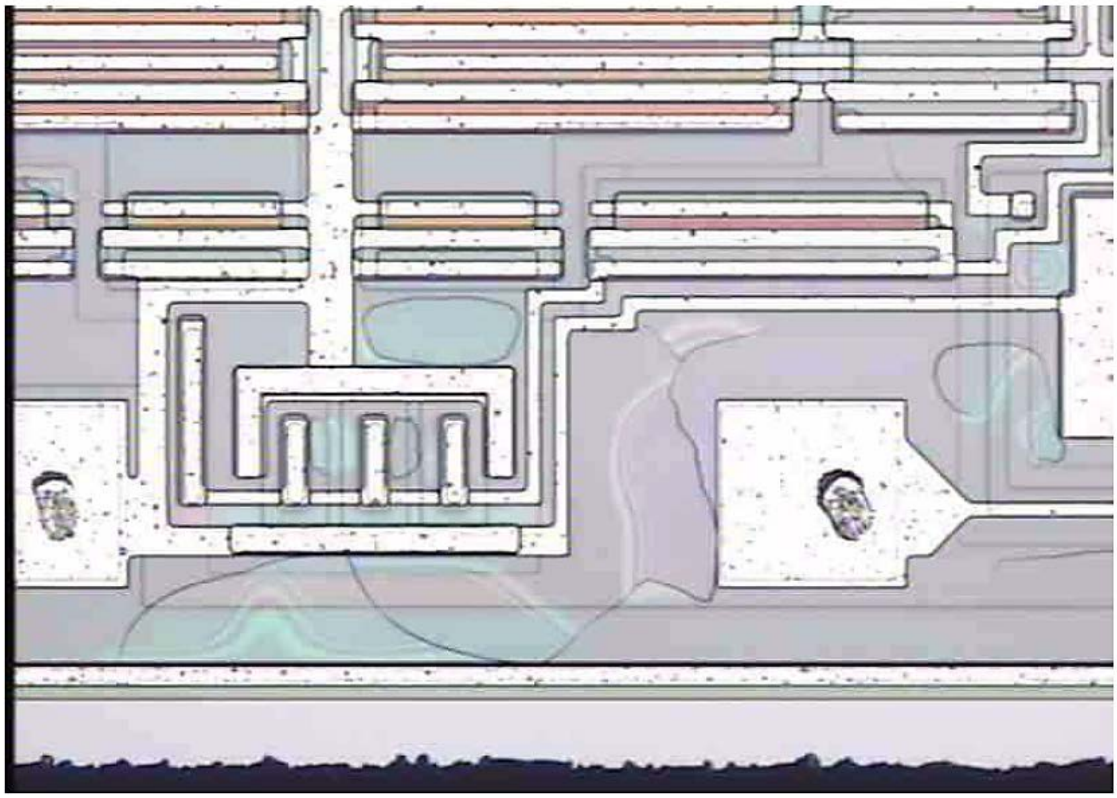
Acceptable Observation

(1) With respect to criteria (a), a simple line under several metallisation paths, showing no colour change is most likely to be considered as a passivation hollow which is not regarded as a passivation fault and is acceptable (see Figure 22).

4.4 GLASSIVATION DEFECTS

(a) Glass crazing that prevents detection of visual criteria contained underneath.

FIGURE 23 - GLASS CRAZING



NOTE TO FIGURE 23

1. REJECT: Glass Crazing prevents detection of visual criteria contained underneath. Para. 4.4(a) refers.

(b) Any lifting or peeling of the glassivation in the active area.

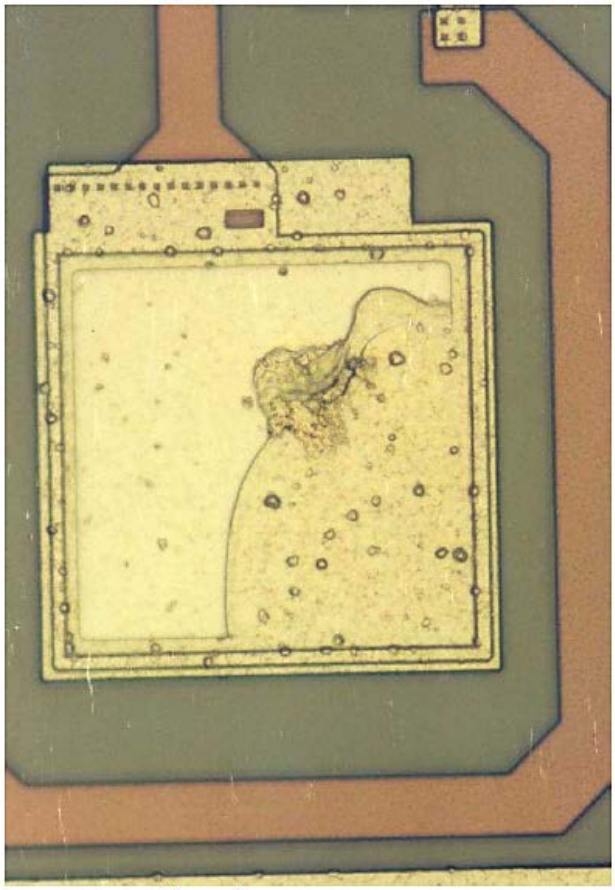
(c) A glassivation void that exposes any active metallisation area by >50% of its original width, unless in accordance with the design specification.

(d) Scratch(es) in the glassivation that disturbs metal, and bridges metallisation paths.

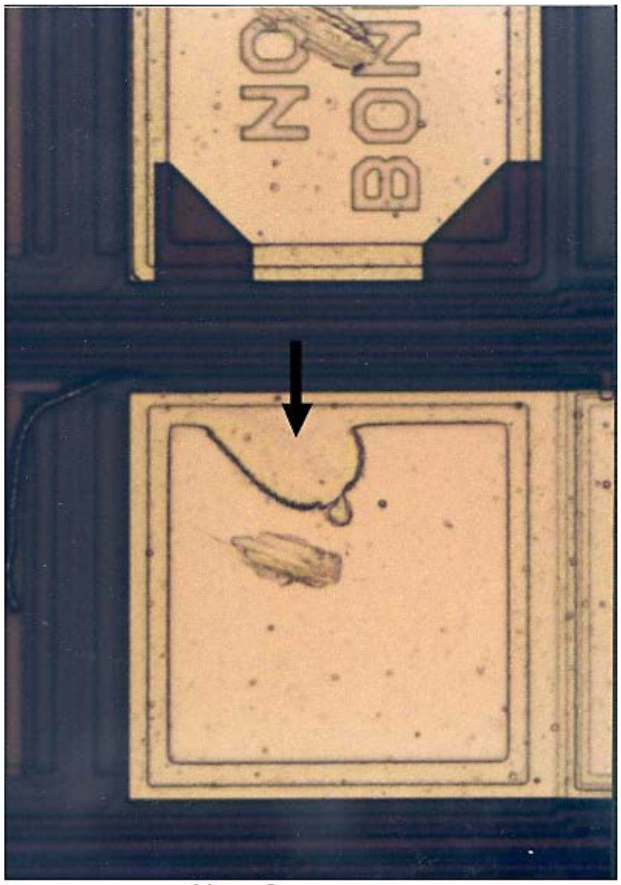
(e) Cracks (not crazing) in the glassivation that form a closed loop over adjacent metallisation paths.

(f) Glassivation which covers the designed open contact or bonding pad area and leaves <75% unglassivated.

FIGURE 24 - GLASSIVATION COVERING BONDING PAD AREA



Note 1



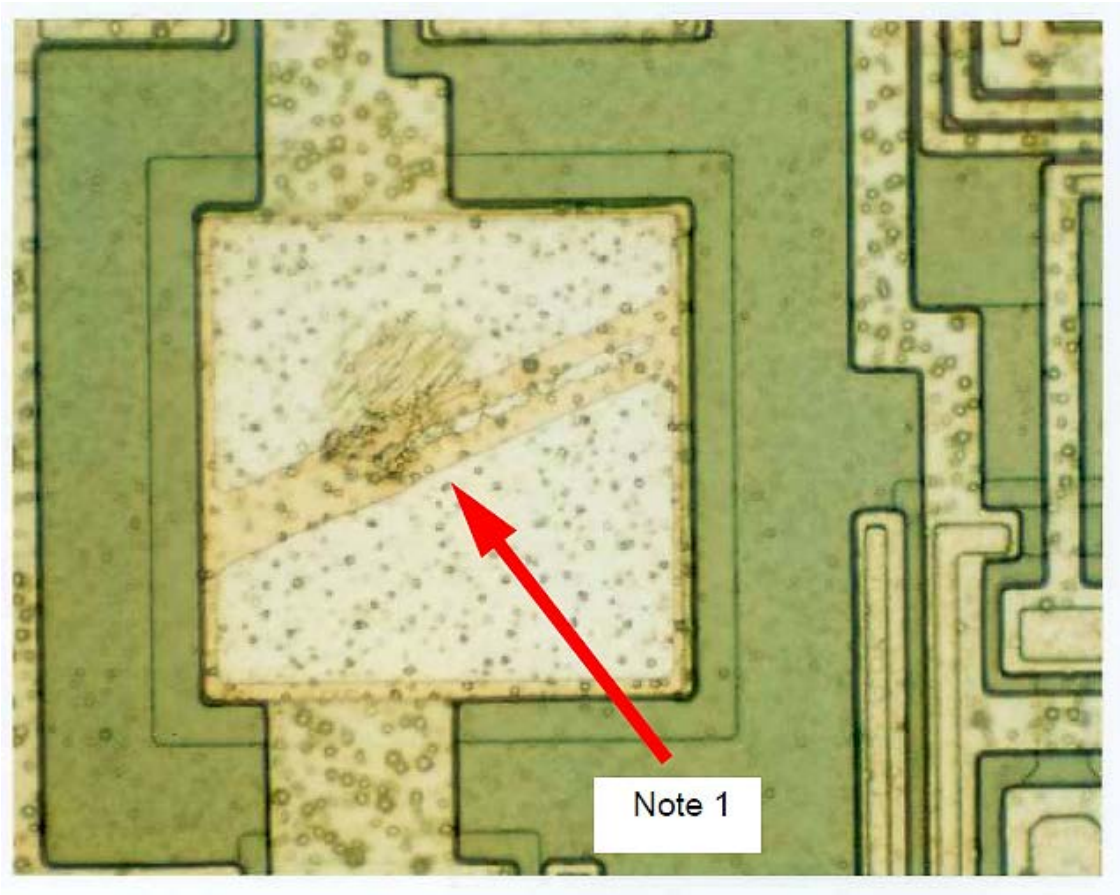
Note 2

NOTES TO FIGURE 24

1. REJECT: Glassivation fault leaving <75% open contact of bond pad area. Para. 4.4(f) refers.
2. ACCEPT: Glassivation fault leaving >75% open contact of bond pad area. Para. 4.4(f) refers.

(g) Centred glassivation residue on a bonding pad area where the distorted metallisation area is >1/8 (12.5%) of the bonding pad area unglassivated. (compare the similar criteria for scratches and voids Paras. 4.1.2(f) and 4.1.3(e).)

FIGURE 25 - CENTERED GLASSIVATION RESIDUE ON BOND PAD AREA



NOTE TO FIGURE 25

1. REJECT: Glassivation residue >1/8 (12.5%) of bond pad area. Para. 4.4(g) refers.

(h) Glassivation void(s) that expose any portion of a thin film resistor or fusible link except where the glassivation is opened by design.

4.5 DIELECTRIC ISOLATION

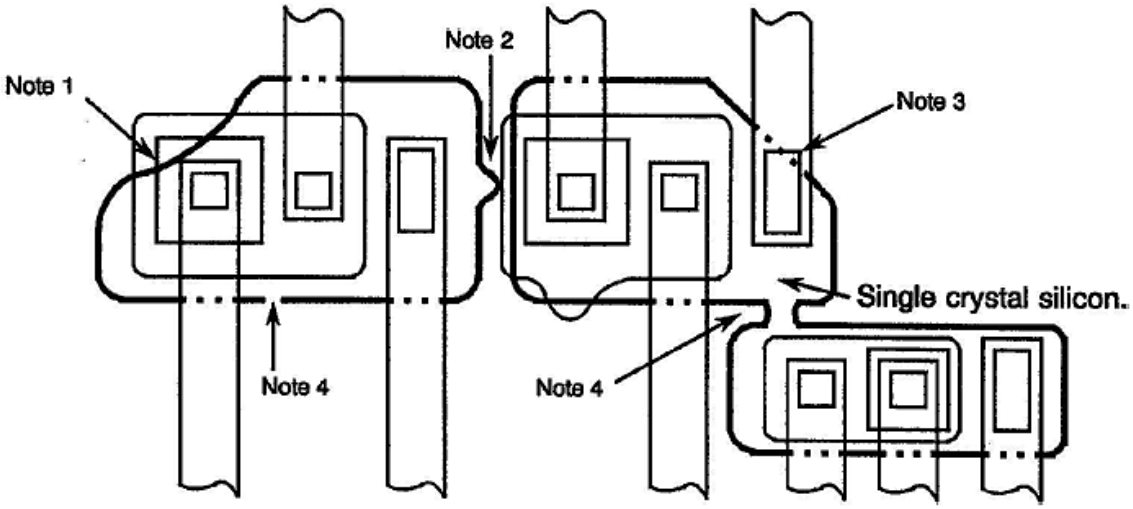
(a) A diffused area which overlaps dielectric isolation material and does not exhibit a line of separation to an adjacent diffusion well; or an overlap of more than one diffusion area into the dielectric isolation material (See Figure 26).

(b) Absence of a continuous isolation line between any adjacent wells, containing functional circuit elements (See Figure 26).

(c) A contact window that touches or overlaps dielectric material, unless in accordance with the design specification (See Figure 26).

(d) A discontinuous isolation line (typically a black line) around each diffusion well containing functional circuit elements.

FIGURE 26 - DIELECTRIC ISOLATION DEFECTS



NOTES TO FIGURE 26

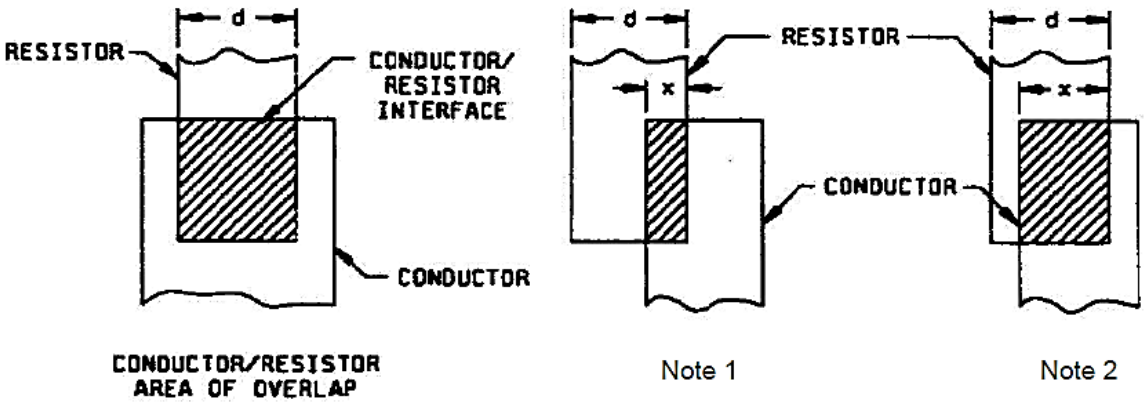
1. REJECT: Overlap of more than one diffusion. Para. 4.5(a) refers.
2. REJECT: Dielectric Isolation line without a line of separation to the adjacent well. Para. 4.5(b) refers.
3. REJECT: Contact window overlap. Para. 4.5(c) refers.
4. REJECT: Discontinuous isolation line. Para. 4.5(d) refers.

4.6 RESISTORS

Rejection shall be based on defects found within the actively used portions of the film resistor. Metallisation, Diffusion, Passivation and Glassivation defect criteria of para 4.1 to 4.4 shall apply.

(a) Any misalignment between the conductor/resistor in which the actual width x of the overlap is <50% of the original resistor width d.

FIGURE 27 - LATERAL MISALIGNMENT OF FILM RESISTORS

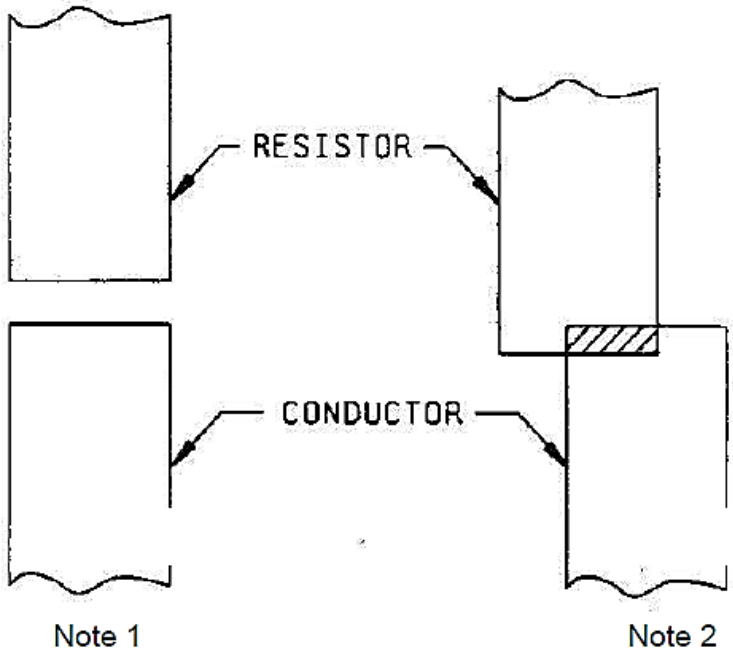


NOTES TO FIGURE 27

1. REJECT: Overlap is <50% of the resistor width d. Para. 4.6(a) refers.
2. ACCEPT: Overlap is >50% of the resistor width d. Para. 4.6(a) refers.

(b) No visible line of contact overlap between the metallisation and film resistor.

FIGURE 28 - AXIAL MISALIGNMENT OF FILM RESISTORS



NOTES TO FIGURE 28

1. REJECT: No visible line of contact overlap. Para. 4.6(b) refers.
2. ACCEPT: An overlap is encountered. Para. 4.6(b) refers.

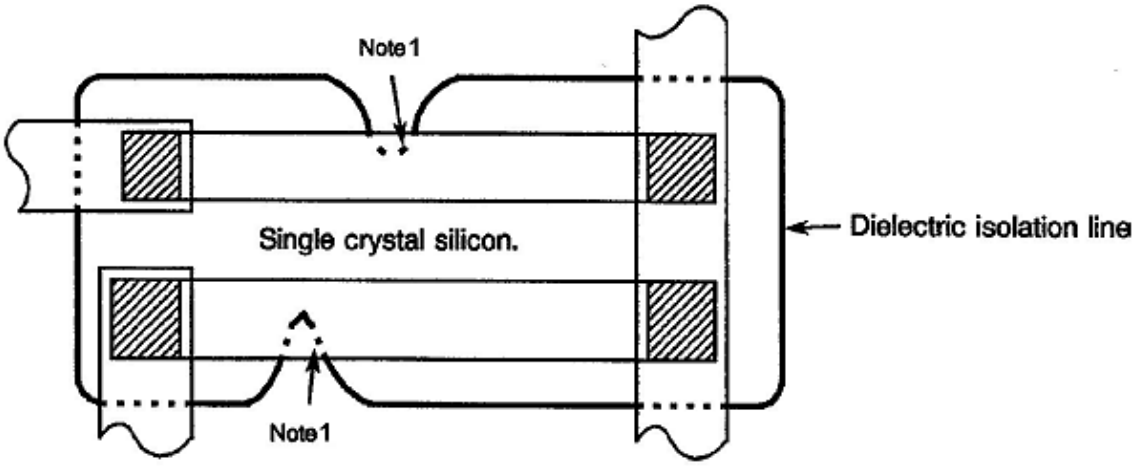
(c) Void or necking down that leaves <75% of the film resistor width undisturbed at a terminal.

(d) Any sharp change in colour of resistor material within 25µm from resistor/connector termination unless the manufacturer can present during the inspection an investigation result demonstrating that the observations have only a harmless effect.

(e) Separation between any two resistors, or a resistor and a metallisation path, that is <5µm, or 50% of the design specification, whichever is less.

(f) Any thin film resistor that crosses a substrate irregularity (i.e. dielectric isolation line, oxide/diffusion step). This criterion does not apply to square isolated islands of single crystal silicon in the polysilicon area.

FIGURE 29 - FILM RESISTORS CROSSING DIELECTRIC ISOLATION LINE



NOTE TO FIGURE 29

1. REJECT: Dielectric material extending under thin film resistor. Para. 4.6(f) refers.

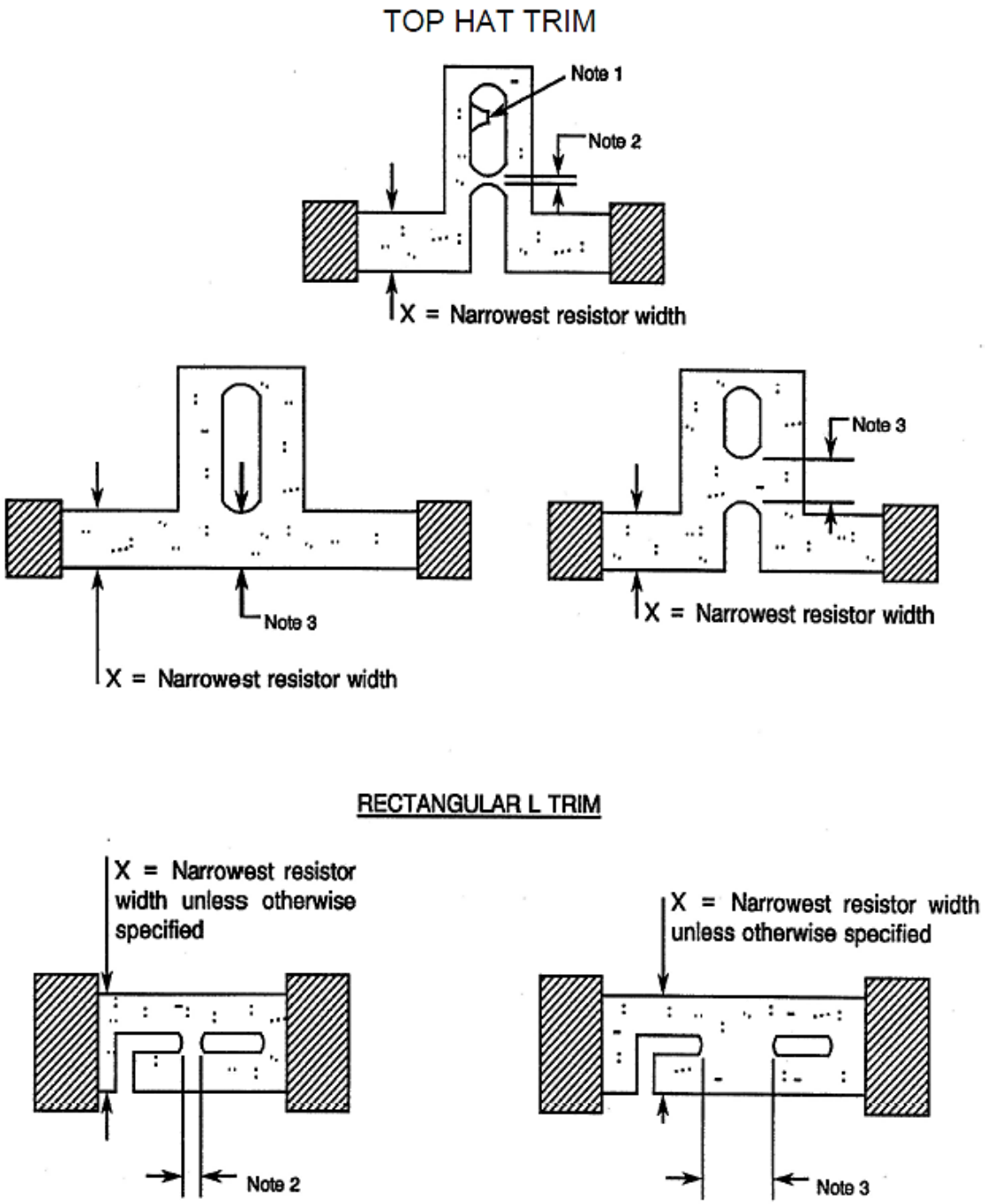
4.7 LASER TRIMMED THIN FILM RESISTORS

(a) A kerf <2.5µm in width, unless in accordance with the design specification.

(b) A kerf containing foreign materials or detritus.

(c) A kerf containing untrimmed resistor material, unless that material is continuous across the kerf, and is undisturbed for a width >0.5X the narrowest resistor width, unless by design.
Note: Maximum allowable current density requirements shall not be exceeded. The investigation results should be available during the pre-cap inspection.

FIGURE 30 - LASER TRIMMED THIN FILTER RESISTOR

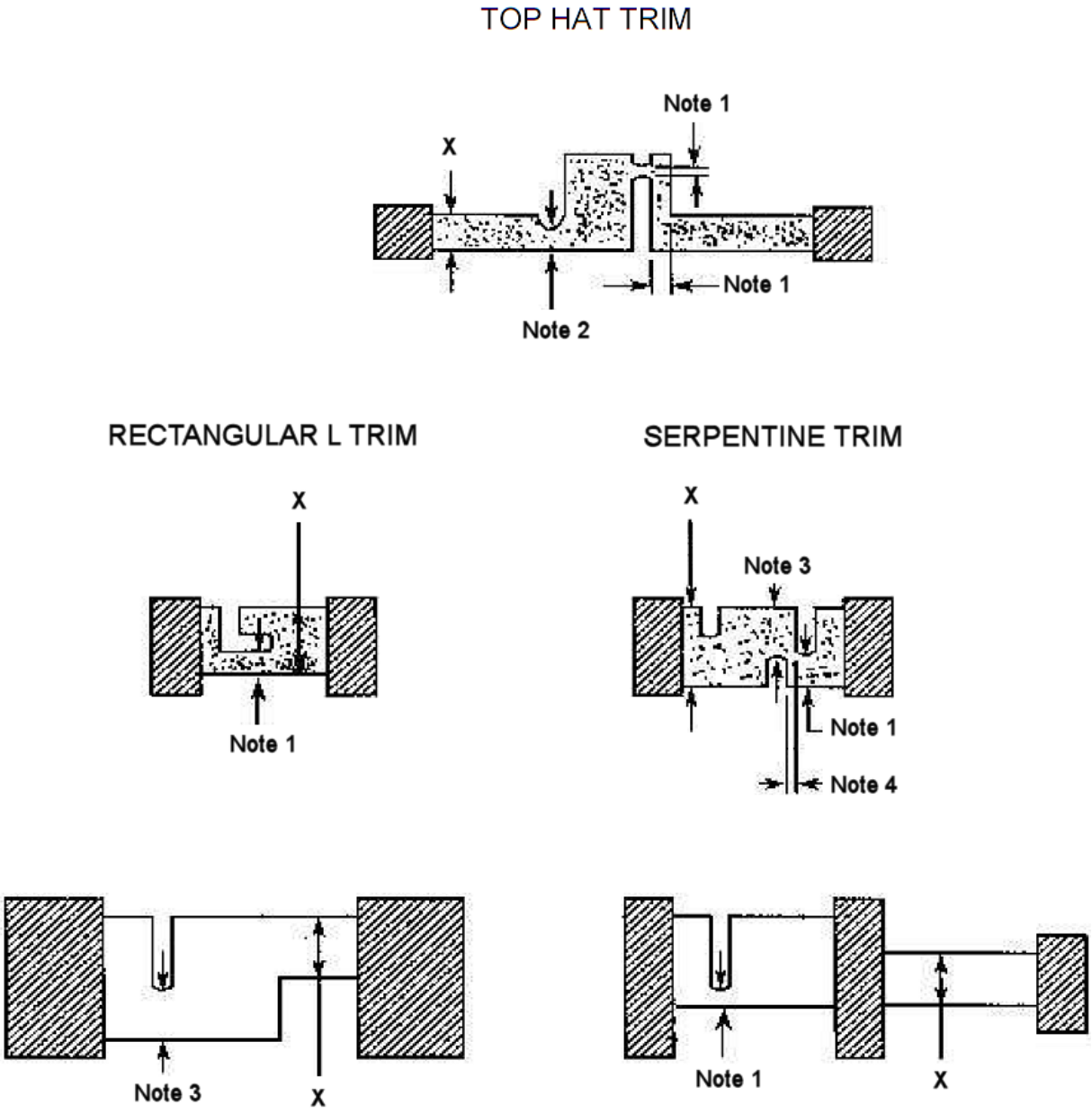


NOTES TO FIGURE 30

1. REJECT: Untrimmed resistor material. Para. 4.7(c) refers.
2. REJECT: Undisturbed width <0.5X narrowest resistor width. Para. 4.7(c) refers.
3. ACCEPT: Undisturbed width >0.5X narrowest resistor width. Para. 4.7(c) refers.

(d) Resistor width that has been reduced by trimming, leaving <50% of the narrowest resistor width X undisturbed, including voids, scratches, or a combination thereof, in the trim area.

FIGURE 31 - SCRATCH AND VOID CRITERIA FOR TRIMMED RESISTORS



NOTES TO FIGURE 31

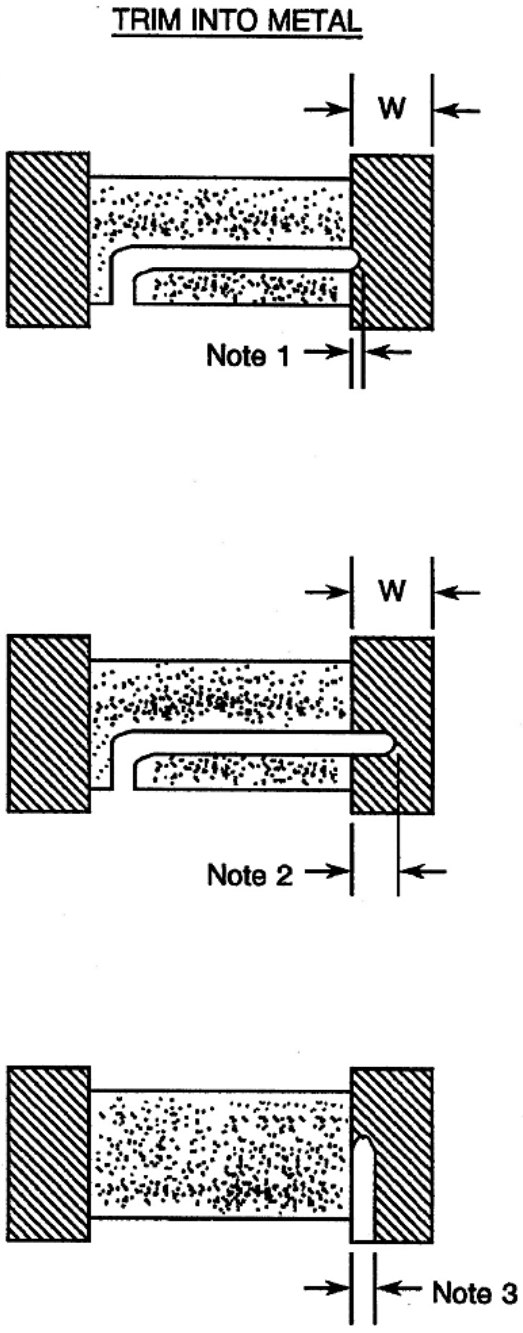
1. REJECT: Trim leaving <50% of the narrowest resistor width X undisturbed. Para. 4.7(d) refers.
2. ACCEPT: Void or scratch leaving >50% of the narrowest resistor width X undisturbed. Para. 4.7(d) refers.
3. ACCEPT: Trim leaving >50% of the narrowest resistor width X undisturbed. Para. 4.7(d) refers.
4. REJECT: Serpentine trim leaving a resistor width <50% of the narrowest resistor width X undisturbed. Para. 4.7(d) refers.

(e) Trim path into the metallisation except block resistors.

(f) Trim for block resistors which extends into the metallisation (excluding bonding pads) >25% of the original metal width W (See Figure 32).

(g) Trim for block resistors that exhibit no laser trim into the resistor film.

FIGURE 32 - BLOCK RESISTORS CRITERIA



NOTES TO FIGURE 32

1. ACCEPT: Trim into metallisation <25% of original metal width W. Para. 4.7(f) refers.
2. REJECT: Trim into metallisation >25% of original metal width W. Para. 4.7(f) refers.
3. REJECT: No laser trim into resistor film. Para. 4.7(g) refers.

(h) Pits into the silicon dioxide in the kerf which do not exhibit a line of separation between the pit and the resistor material.

Acceptable Observation

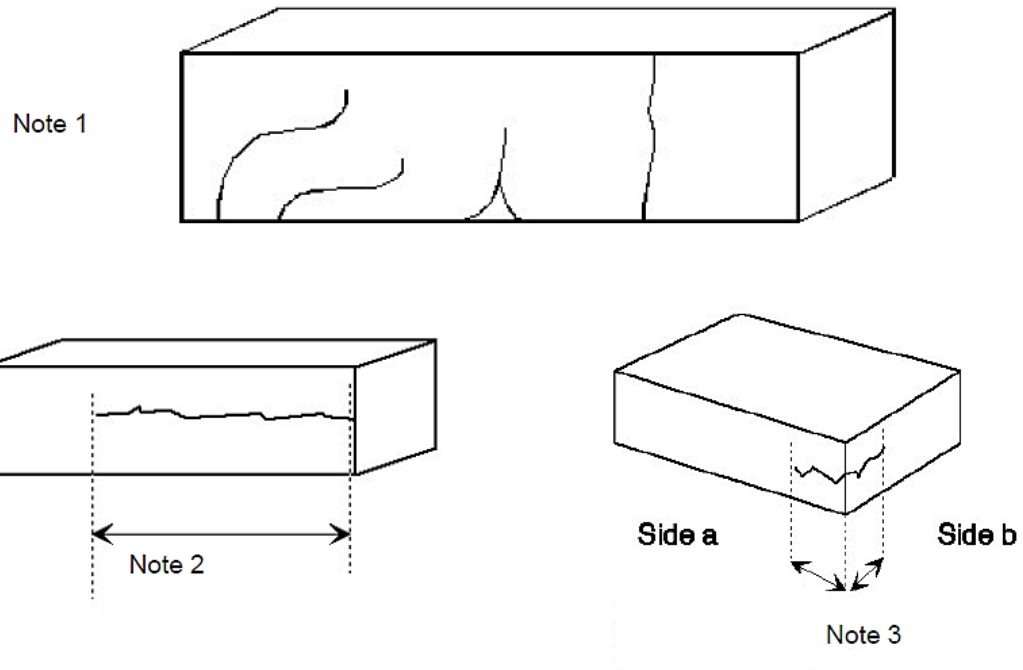
(1) Trimming of >50% of a given resistor shunt link is acceptable by design providing that the last shunt link of the resistor adder network is not trimmed >60%. All trimmable resistor shunt links shall be defined on the design layout drawing.
(2) Trim path into the metallisation can be accepted for trim paths into terminator ends of metallisation runs. Conductors or resistors may be trimmed open for link trims by design.

4.8 SCRIBING AND DIE DEFECTS

4.8.1 General

(a) <5µm of passivation visible between operating metallisation or bond periphery and bare semiconductor material.
Note: These criteria can be excluded for peripheral metallisation including bonding pads where the metallisation is at the same potential as the die.
(b) Die having attached portions of the active circuit area of another die.
(c) Cracks in the substrate visible on the side of the die pointing towards the top surface of the die (See Figure 33).
(d) Cracks located on the side of the die and parallel to the surface of the die that extend beyond 50% of the relevant edge of the die (See Figure 33).
(e) In the case of two cracks located on adjacent sides parallel to the surface of the die, where the cumulative length of the two cracks is >50% of the smaller side of the die.

FIGURE 33 - CRACKS ON THE SIDE OF THE DIE



NOTES TO FIGURE 33

1. REJECT: Cracks on the side of the die pointing towards the top surface of the die. Para. 4.8.1(c) refers.
2. REJECT: Crack parallel to the surface extending beyond 50% of the relevant edge of the die. Para. 4.8.1(d) refers.
3. REJECT: Two cracks on adjacent sides parallel to the surface with a cumulative length that is >50% of side b. Para. 4.8.1(e) refers.

Acceptable Observation

(1) Chip-outs on the side of the die are accepted regardless of their shape as long as they also verify all criteria applicable on the top of the die.

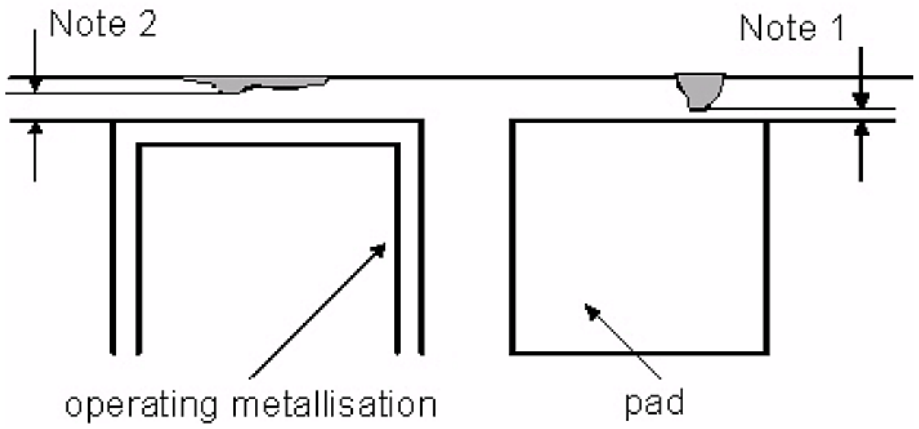
4.8.2 Die Defects in Active Circuit Area

(a) A chip-out or crack in the active circuit area.
Note: This criterion can be excluded for peripheral metallisation that is at the same potential as the substrate. ≥50% of the metallisation width at the chipout shall remain undisturbed.

4.8.3 Die Defects in Non-active Circuit Area

(a) Chip-out or offset scribe lines/breaks into the non-active circuit area where the distance remaining between the active area and the edge of the fault is <5µm.

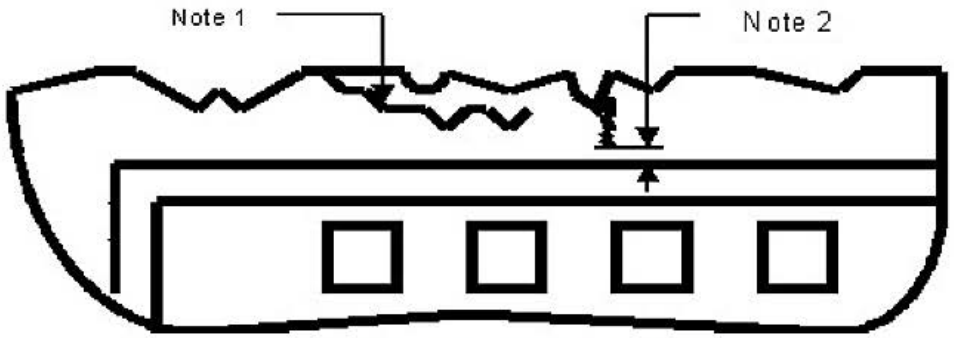
FIGURE 34 - SEPARATION TO DIE DEFECT

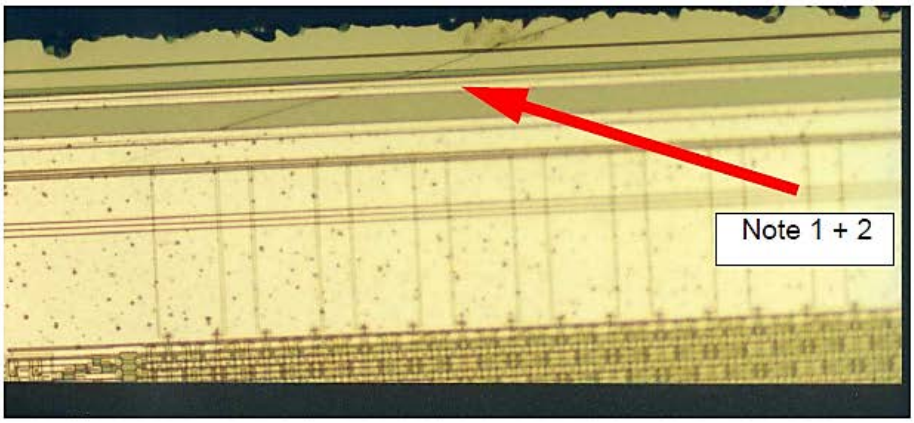


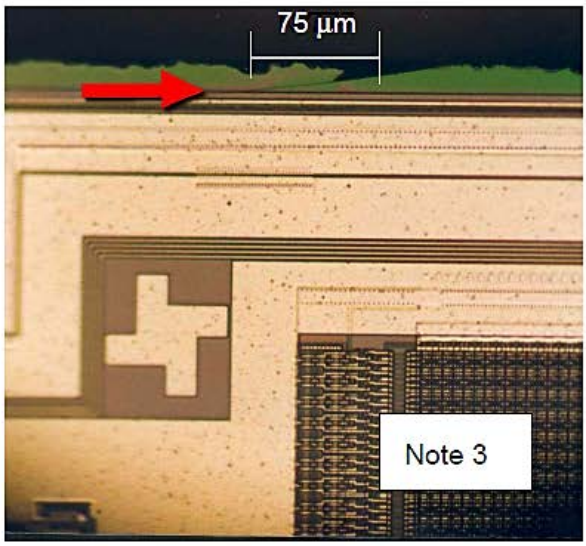
NOTES TO FIGURE 34
1. REJECT: Separation <5µm. Para. 4.8.3(a) refers.
2. ACCEPT: Separation >5µm. Para. 4.8.3(a) refers.

(b) A crack or crystallographic defect >75µm in length or comes closer than 5µm to any operating metallisation (except for substrate potential peripheral metal), or functional circuit element.

FIGURE 35 - DIE CRACKS





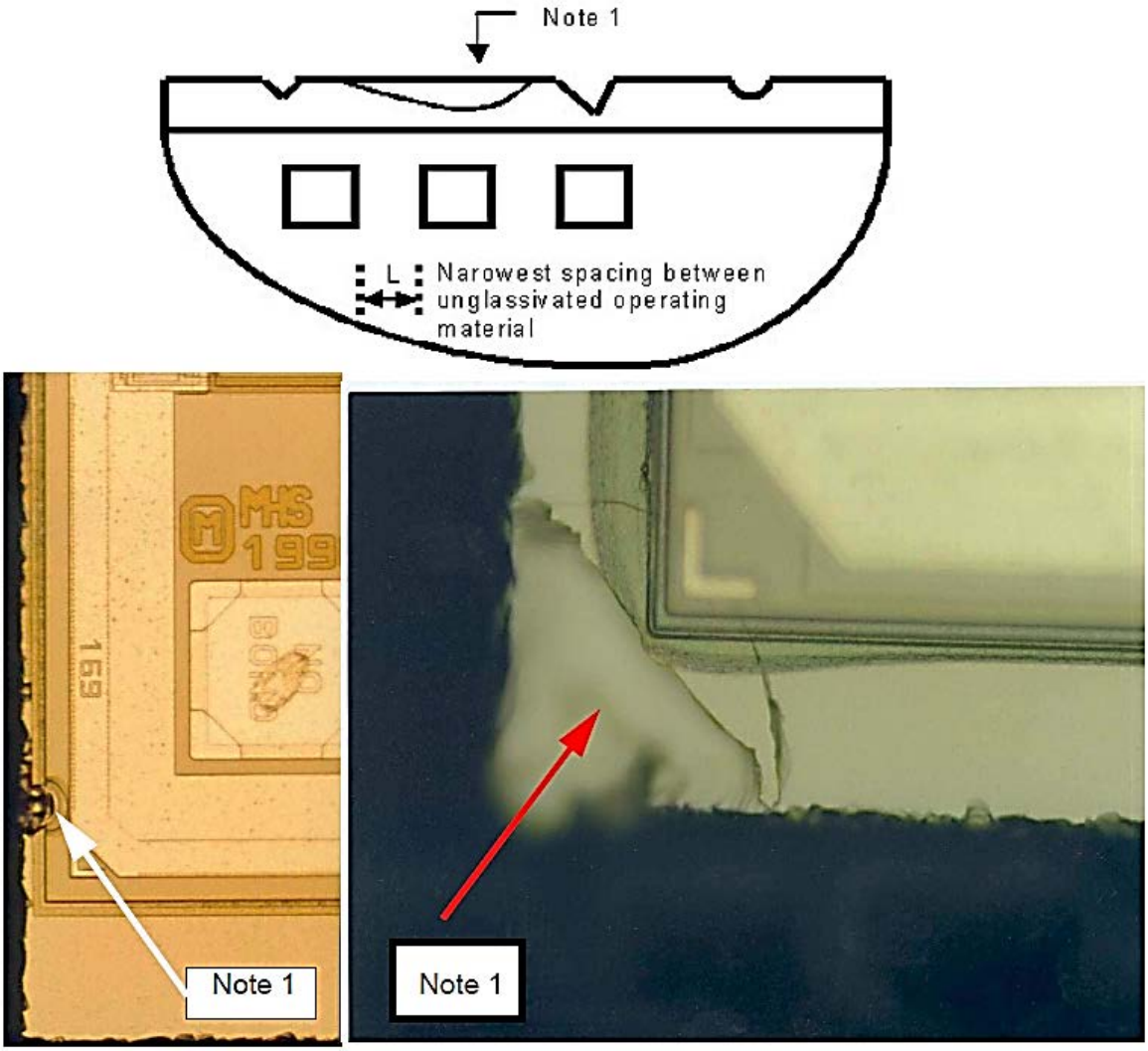


NOTES TO FIGURE 35

1. REJECT: Crack length >75µm. Para. 4.8.3(b) refers.
2. REJECT: Separation to operating metallisation <5µm. Para. 4.8.3(b) refers.
3. ACCEPT: Crack length <75µm. Para. 4.8.3(b) refers.

(c) Semicircular crack(s), whose chord is long enough to bridge the narrowest spacing between unglassivated operating material L in the case of detachment (e.g. metallisation, bare semiconductor material, mounting material, bonding wire, etc.).

FIGURE 36 - SEMICIRCULAR CRACK

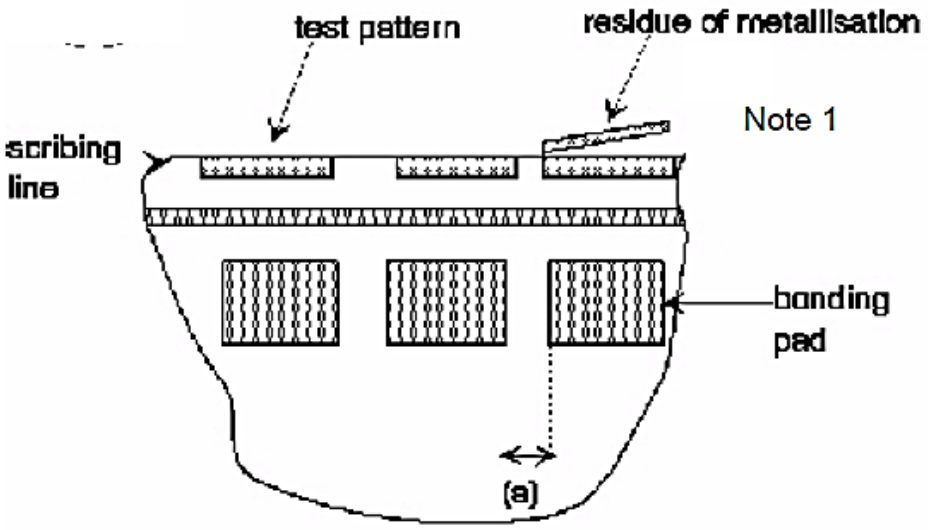


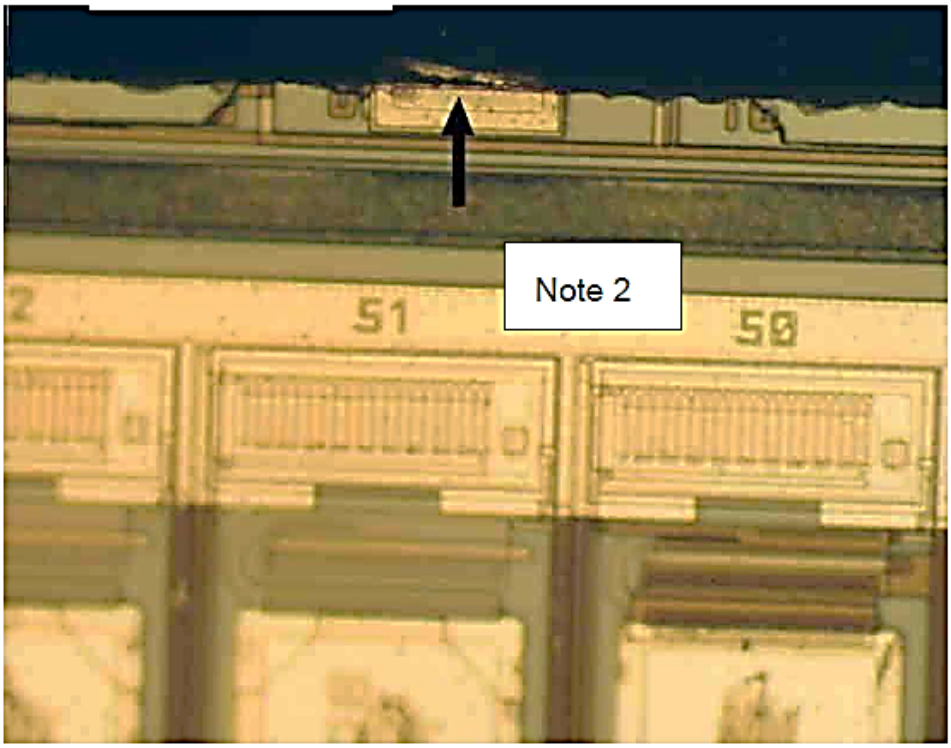
NOTE TO FIGURE 36

1. REJECT: Semicircular crack long enough to bridge the narrowest spacing between unglassivated operating material L. Para. 4.8.3(c) refers.

(d) Displaced residue of metallisation on the die after die scribe, due to the practice of printing test patterns onto the scribing line, that are large enough to bridge the spacing between unglassivated operating material, pad, bond, bond wire, etc.

FIGURE 37 - RESIDUE OF METALLISATION





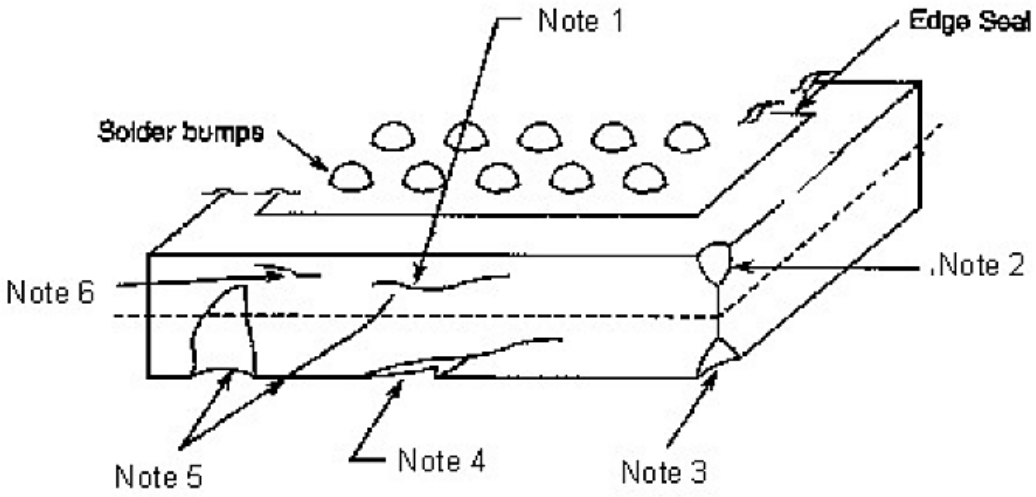
NOTES TO FIGURE 37

1. REJECT: Residue long enough to bridge the narrowest spacing between unglassivated operating material. Para. 4.8.3(d) refers.
2. ACCEPT: Residue smaller than narrowest distance between unglassivated operating material and there is no risk of detachment. Para. 4.8.3(d) refers.

4.8.4 Flip Chip Die Defects

(a) For flip chip, cracks or chip-outs in the substrate material that extends beyond 50% of the substrate thickness, or a crack >125µm in length in the substrate material.

FIGURE 38 - SCRIBING AND DIE DEFECTS (FLIP CHIPS)

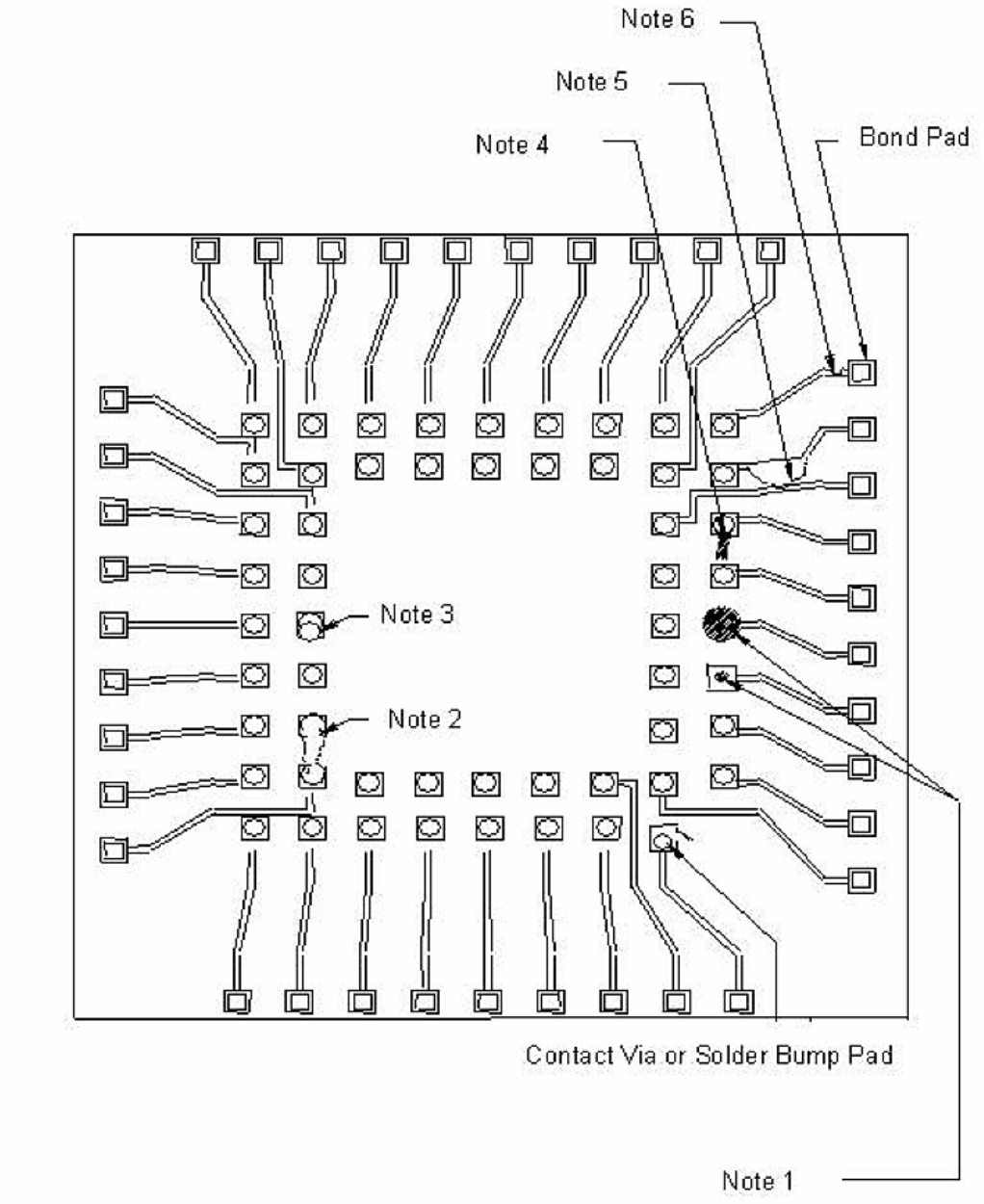


NOTES TO FIGURE 38

1. REJECT: Crack length >125µm. Para. 4.8.4(a)refers.
2. ACCEPT: Chip-out not extending beyond 50% of die thickness. Para. 4.8.4(a) refers.
3. ACCEPT: Chip-out not extending beyond 50% of die thickness. Para. 4.8.4(a) refers.
4. ACCEPT: If chip-out and crack are <50% of die thickness. Para. 4.8.4(a) refers.
5. REJECT: Chip-out and crack extending beyond 50% of die thickness. Para. 4.8.4(a) refers.
6. ACCEPT: Crack length <125µm. Para. 4.8.4(a) refers.

(b) Missing solder ball from original design position.
(c) Solder ball 20% smaller, or larger than design size (nominal).
(d) Solder balls bridging.
(e) Misaligned solder ball which exposes the UBM on the contact via.
(f) Any attached or embedded foreign material bridging balls, or redistribution metallisation.
(g) Any redistribution metallisation bridging.
(h) Voids in redistribution metallisation >50% of the design width.
(i) Any residual unetched UBM bridging balls or redistribution metallisation.
(j) Mechanical damage to the ball which reduces the original height or diameter >20%.
Note: Minor damage to the solder ball and bump misalignment can be reworked by performing a reflow/ refresh of the solder balls.
(k) Lifting, or peeling of the RDL or dielectric material.

FIGURE 39 - BUMPS/SOLDER BALLS ON FLIP CHIP DICE



NOTES TO FIGURE 39

1. REJECT: Solder ball 20% larger or smaller than designed Para. 4.8.4(c) refers.
2. REJECT: Bridging of solder balls Para. 4.8.4(d) refers.
3. REJECT: Misaligned ball exposing UBM Para. 4.8.4(e) refers.
4. REJECT: Attached or embedded foreign material (bridging). Para. 4.8.4(f) refers.
5. REJECT: Bridging of redistribution traces. Para. 4.8.4(g) refers.
6. REJECT: Void in redistribution >50% of design width. Para. 4.8.4(h) refers.

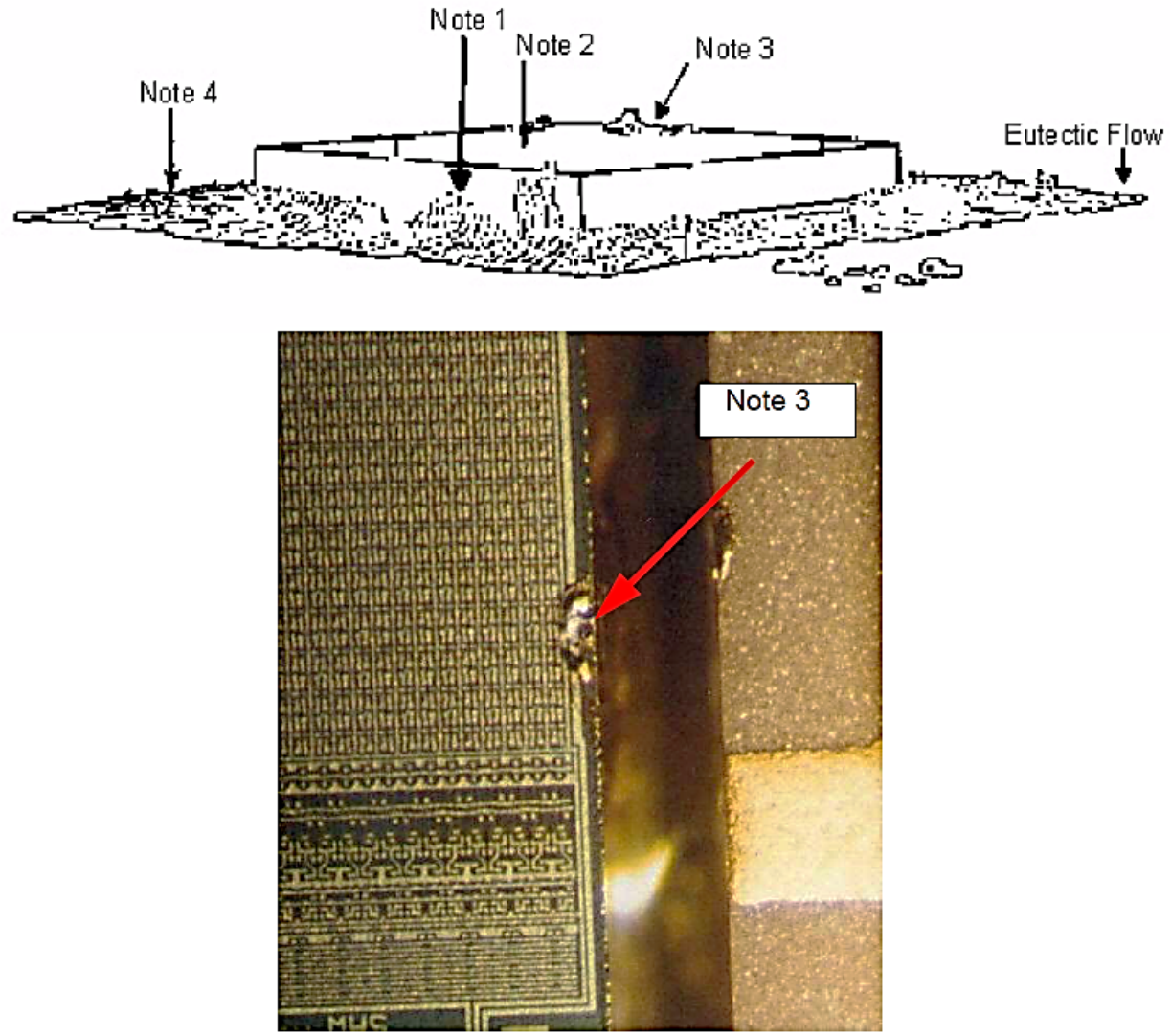
4.9 DIE MOUNTING DEFECTS

The listed defect criteria are applicable for conventional and flip-chip mounting.

4.9.1 General

(a) Die location, orientation, geometry and/or type not in accordance with the applicable assembly drawing.
(b) Die mounting material that extends on to, or vertically above, the top surface of the die.
(c) Die mounting material on the top surface of the die, scribe line excluded.
(d) Any flaking, peeling, or lifting of the die mounting material.

FIGURE 40 - DIE MOUNTING DEFECTS



NOTES TO FIGURE 40

1. ACCEPT: Not exceeding die height. Para. 4.9.1(b) refers.
2. REJECT: Exceeding die height. Para. 4.9.1(b) refers.
3. REJECT: Die attach material on the surface of the die. Para4.9.1(c) refers.
4. REJECT: Flaking of the die mounting material. Para. 4.9.1(d) refers.

(e) Transparent die with <50% of the area bonded.

4.9.2 Die Mounting, Eutectic

(a) Preform not properly melted.

(b) Die mounting material (eutectic wetting) not visible around at least two complete opposite sides, or <75%, of the die perimeter, except for transparent die. See Figure 41 for minimum acceptance. The absence of die mounting material shall be confirmed by a tilted inspection.

FIGURE 41 - VISIBILITY OF DIE MOUNTING MATERIAL

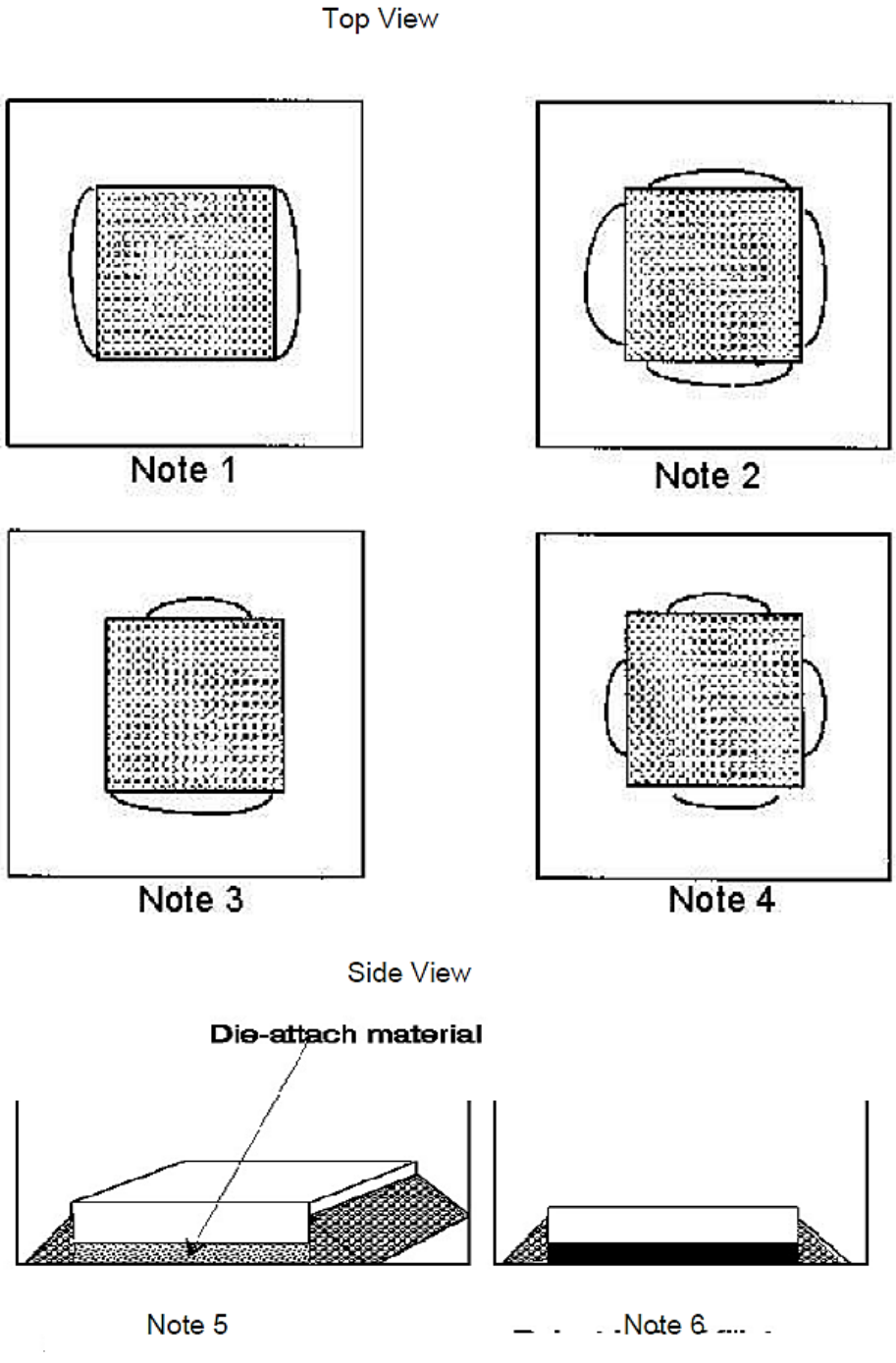
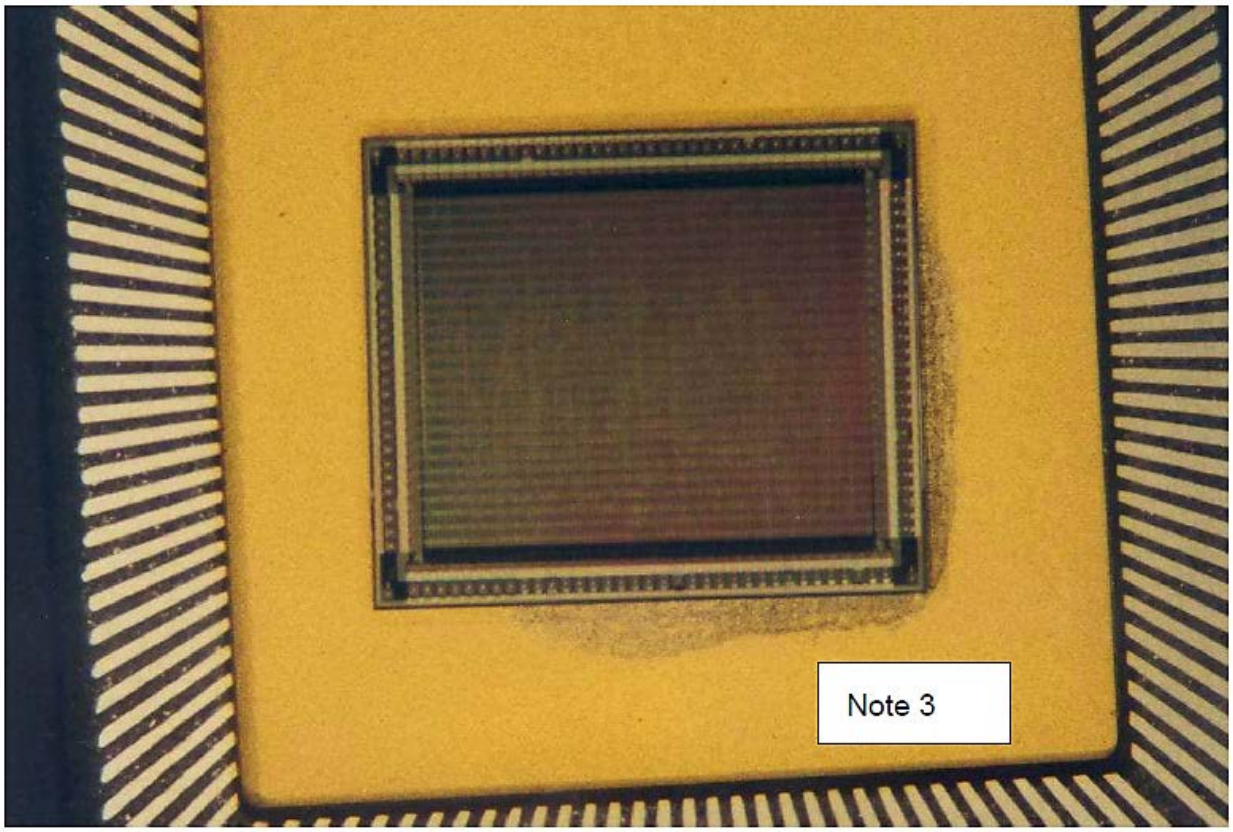


FIGURE 41 – VISIBILITY OF DIE MOUNTING MATERIAL (CONTINUED)

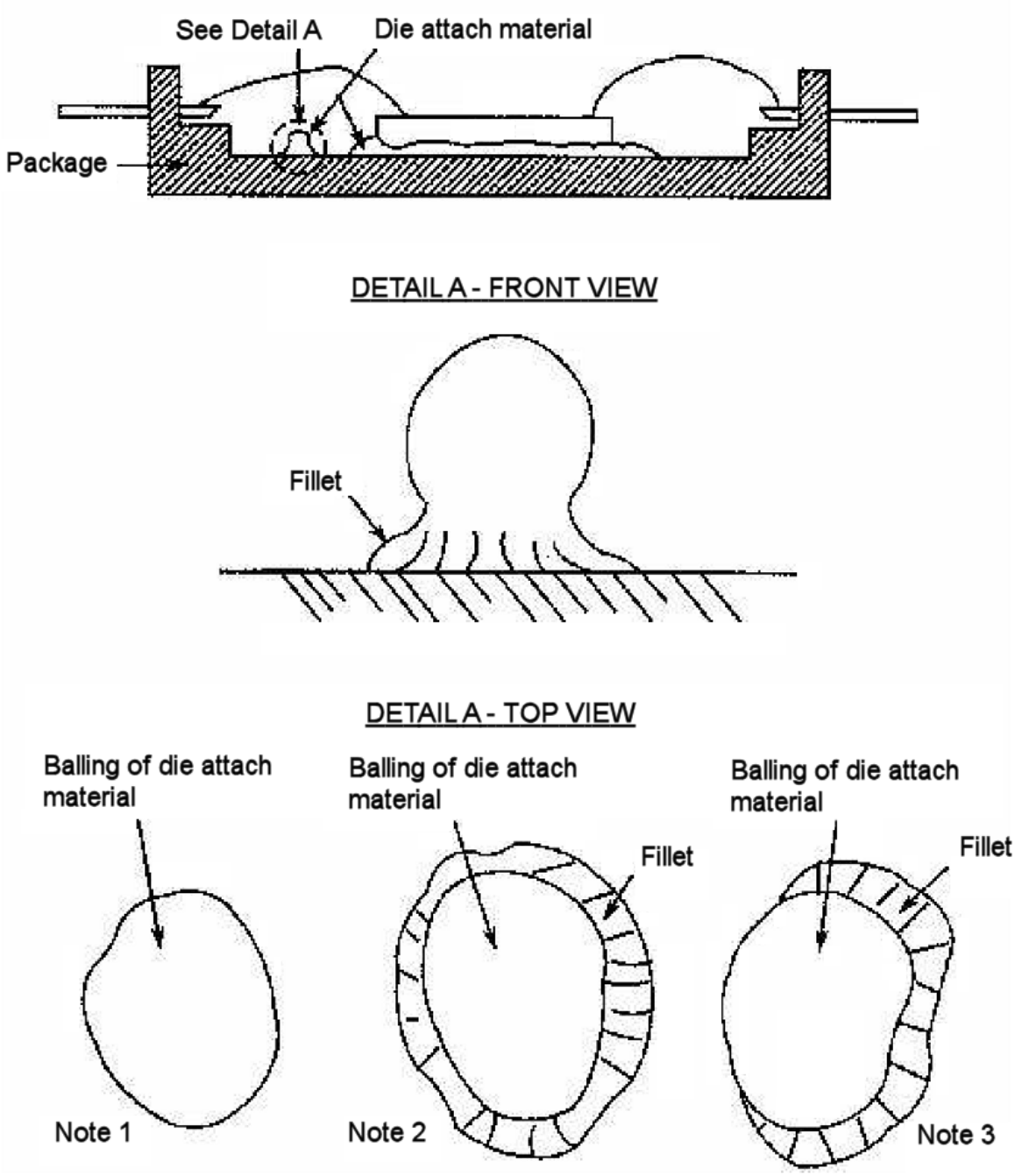


NOTES TO FIGURE 41

1. ACCEPT: Visible at two complete sides. Para. 4.9.2(b) refers.
2. ACCEPT: Visible at >75% of perimeter. Para. 4.9.2(b) refers.
3. REJECT: Not visible at two complete opposite sides as a result of top and tilted inspection. Para. 4.9.2(b) refers.
4. REJECT: Visible at <75% of perimeter as a result of top and tilted inspection. Para. 4.9.2(b) refers.
5. ACCEPT: Visible die mounting material. Para. 4.9.2(b) refers.
6. REJECT: No die mounting material. Para. 4.9.2(b) refers.

(c) Balling or build-up of the die mounting material that does not exhibit a minimum of a 50% peripheral fillet, when viewed from above, or the accumulation of bonding material is such that the height of the accumulation is greater than the longest base dimension or the accumulation necks down at any point.

FIGURE 42 - BALLING OF DIE ATTACH MATERIAL



NOTES TO FIGURE 42

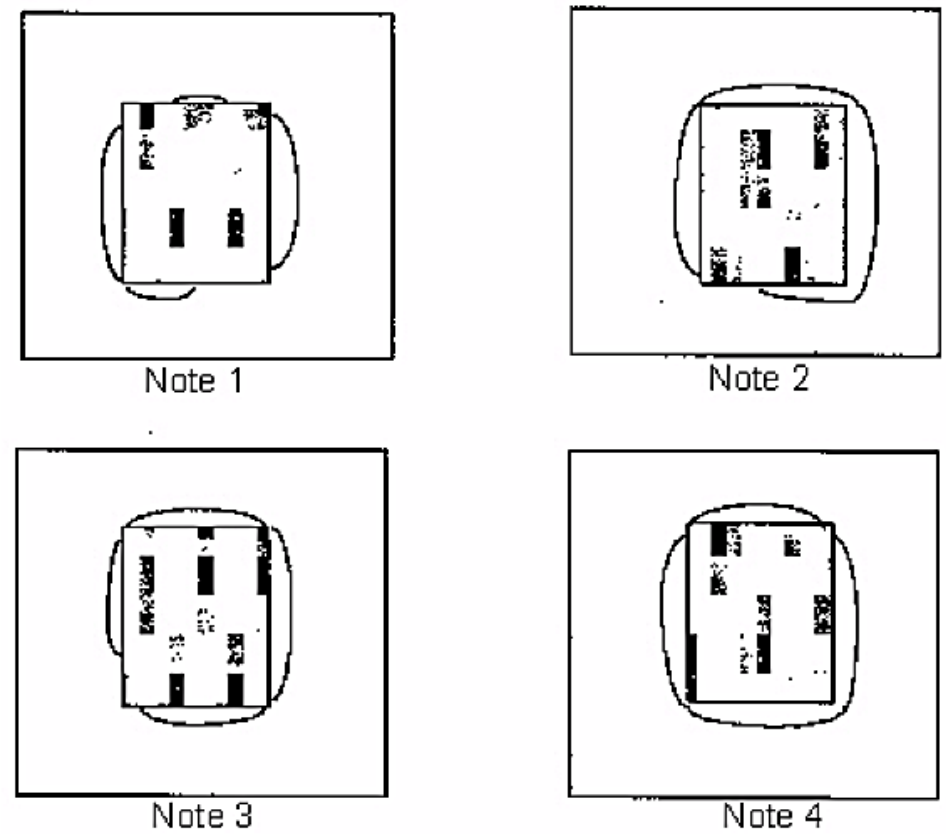
1. REJECT: No fillet visible. Para. 4.9.2(c) refers.
2. ACCEPT: Fillet visible. Para. 4.9.2(c) refers.
3. ACCEPT: Fillet visible for >50% of perimeter. Para. 4.9.2(c) refers.

4.9.3 Die Mounting, Non-Eutectic

(a) Adhesive fillet not visible along 75% of each side of the die.
Note: In the case of silver glass, if the adhesive fillet is not visible on one side only, a tilted inspection must show that the adhesive is perpendicular to the side of the die. The absence of die mounting material shall be confirmed by a tilted inspection.

FIGURE 43 - VISIBILITY OF ADHESIVE

Top View



Side View

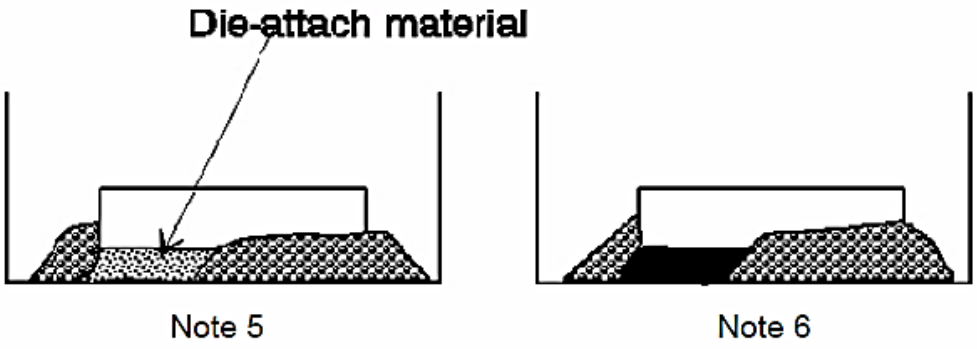
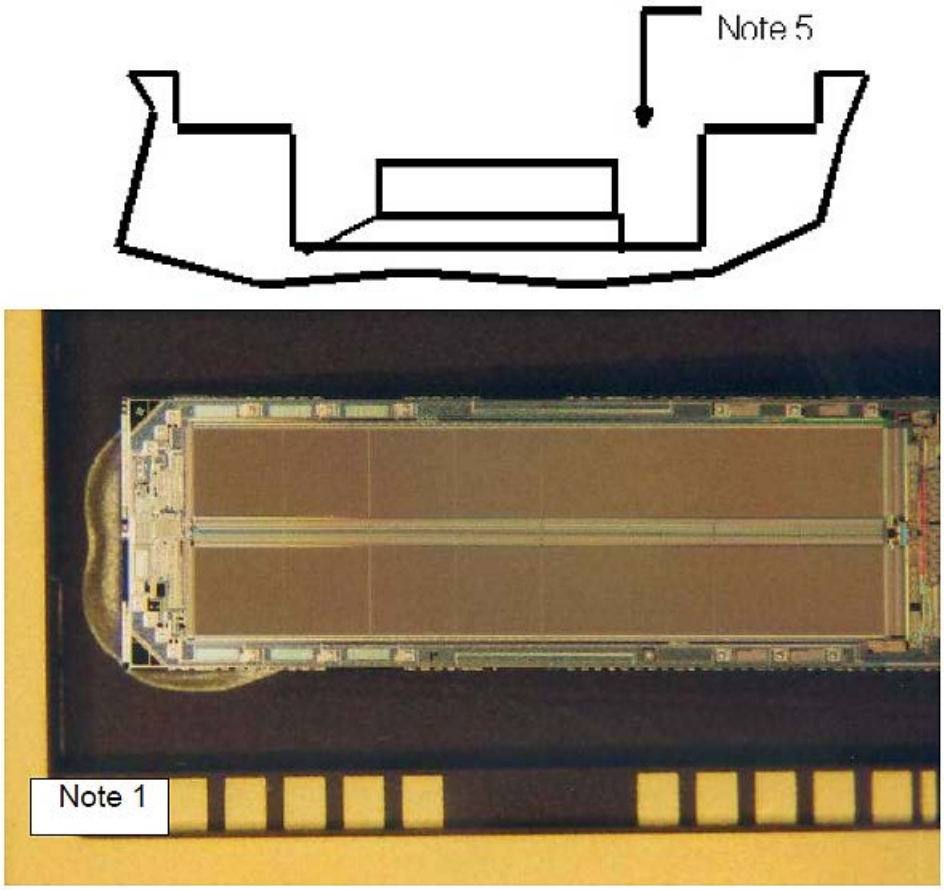


FIGURE 43 – VISIBILITY OF ADHESIVE (CONTINUED)



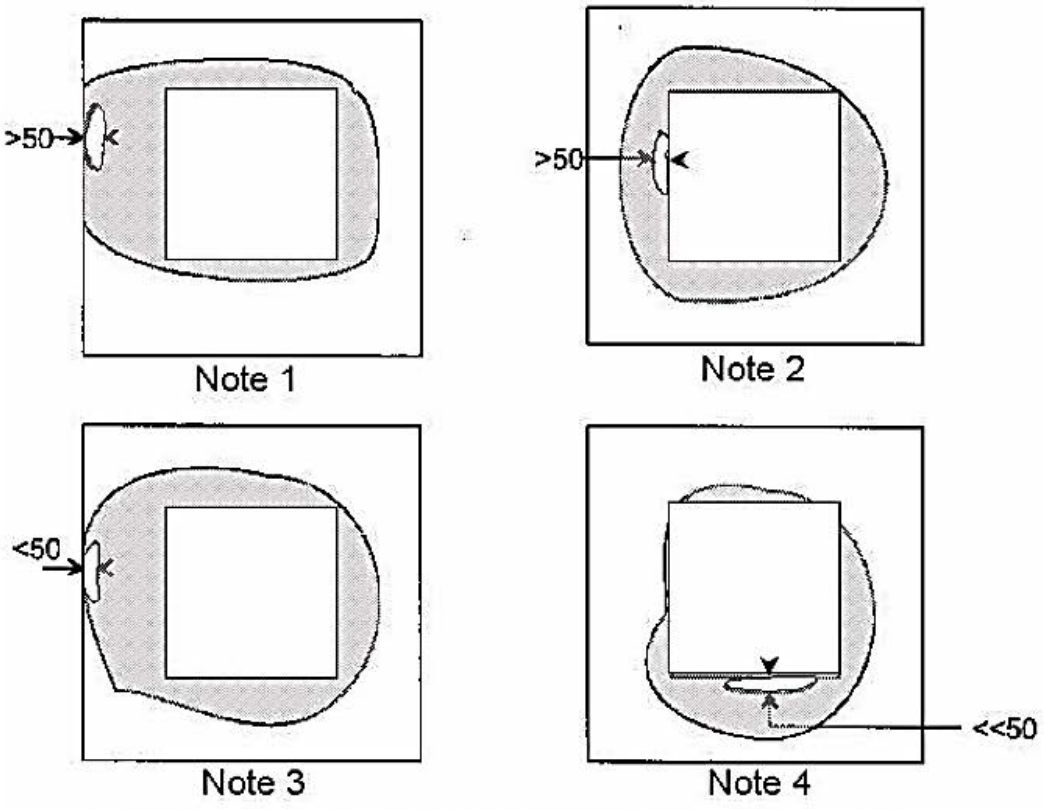
NOTES TO FIGURE 43

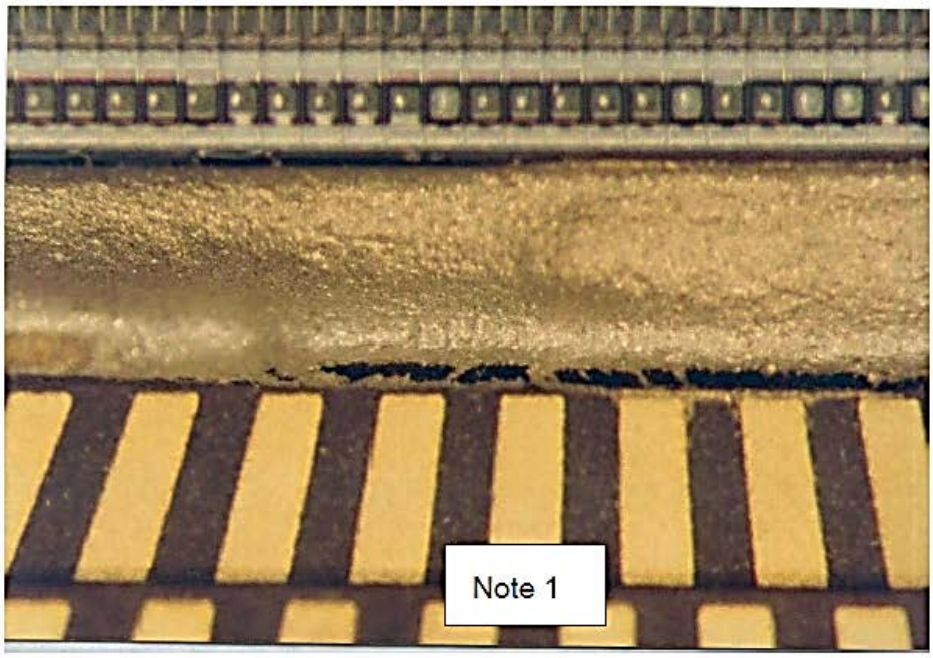
1. REJECT: At least one side with <75% visibility of fillet. Para. 4.9.3(a) refers.
2. REJECT: One side with <75% visibility of fillet. Para. 4.9.3(a) refers.
3. REJECT: One side with <75% visibility of fillet. Para. 4.9.3(a) refers.
4. ACCEPT: Each side with >75% visibility of fillet. Para. 4.9.3(a) refers.
5. ACCEPT: Visible die mounting material. Para. 4.9.3(a) refers.
6. REJECT: No die mounting material. Para. 4.9.3(a) refers.

(b) Crazing in the adhesive material.

(c) Separation, cracks or fissures whose width is >50µm in the adhesive at the cavity wall or cavity floor, where cracks are considered to be fractures in the adhesive that have sharp broken edges.

FIGURE 44 - FRACTURES IN THE ADHESIVE



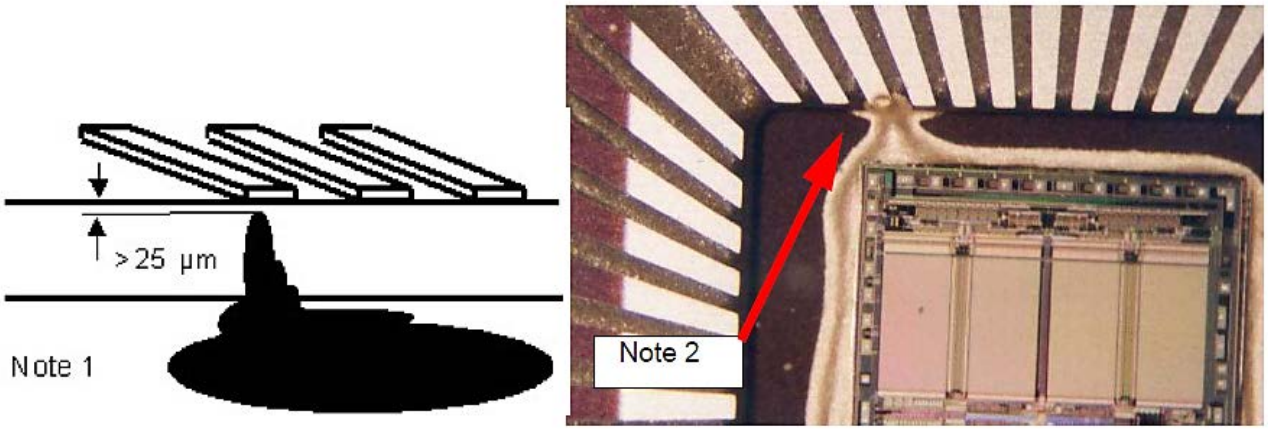


NOTES TO FIGURE 44

1. REJECT: fissure width >50µm in the adhesive. Para. 4.9.3(c) refers.
2. REJECT: fissure width >50µm in the adhesive. Para. 4.9.3(c) refers.
3. ACCEPT: fissure width <50µm in the adhesive. Para. 4.9.3(c) refers.
4. ACCEPT: fissure width <50µm in the adhesive. Para. 4.9.3(c) refers.

(d) Any adhesive material which extends up the cavity wall to within 25µm of the package post.

FIGURE 45 - ADHESIVE ON THE CAVITY WALL



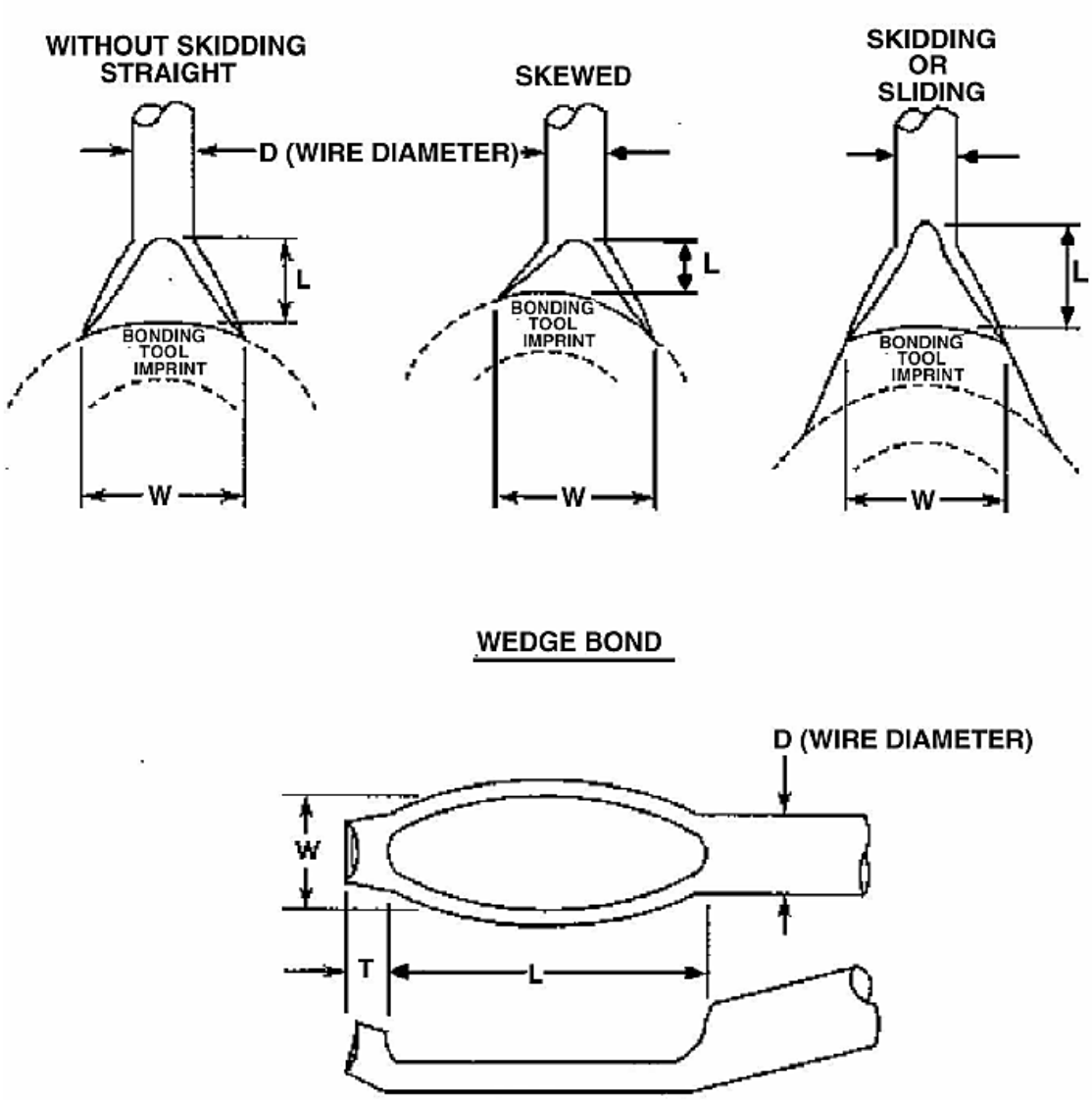
NOTES TO FIGURE 45

1. ACCEPT: adhesive on cavity wall >25µm separated from posts. Para. 4.9.3(d) refers.
2. REJECT: adhesive on cavity wall <25µm separated from posts. Para. 4.9.3(d) refers.

4.10 BOND INSPECTION

The criteria applicable for bonds (called "wedge bonds" or "bonds") in Paras. 4.10.1, 4.10.2 and 4.10.3 refers to the fully or partially deformed area including the tool impression shown as "L" in Figure 46. The criteria applicable for "bond tails" or "tails" refers to the resulting length of bonding wire extending beyond the bond shown as "T" in Figure 46. The tail is not part of the bond.

FIGURE 46 - BOND DIMENSIONS



NOTES TO FIGURE 46

The specification limits for bond width (W) and length (L) are given as factors of the wire diameter (D) in the table below:

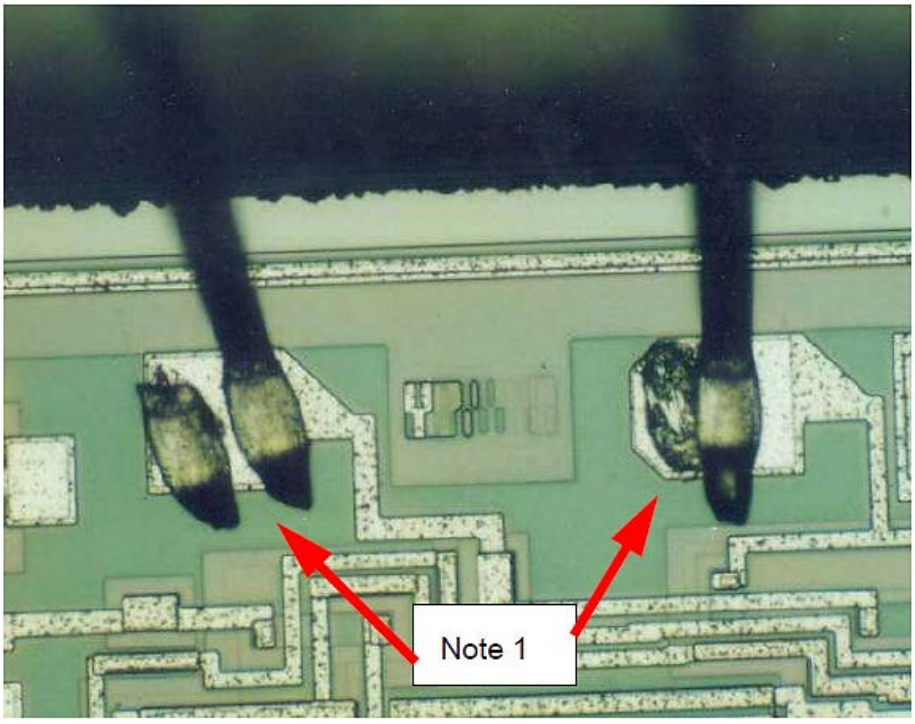
Type	Wmin	Wmax	Lmin	Lmax	Para. Ref.
Ultrasonic Wedge Bond	1.2	3	1.5	6	4.10.2(a)
Thermocompression W.B.	1.5	3	1.5	6	4.10.2(b)
Crescent Bond	1.2	5	0.5	3	4.10.3(a)

4.10.1 General (Gold Ball, Aluminium, Wedge, and Tailless)

Note: Bond wire fragments or bond pad metal detached from the bond or pad shall be treated as foreign material (see Para. 4.12).

(a) Re-bonding is not allowed.

FIGURE 47 - REBONDING

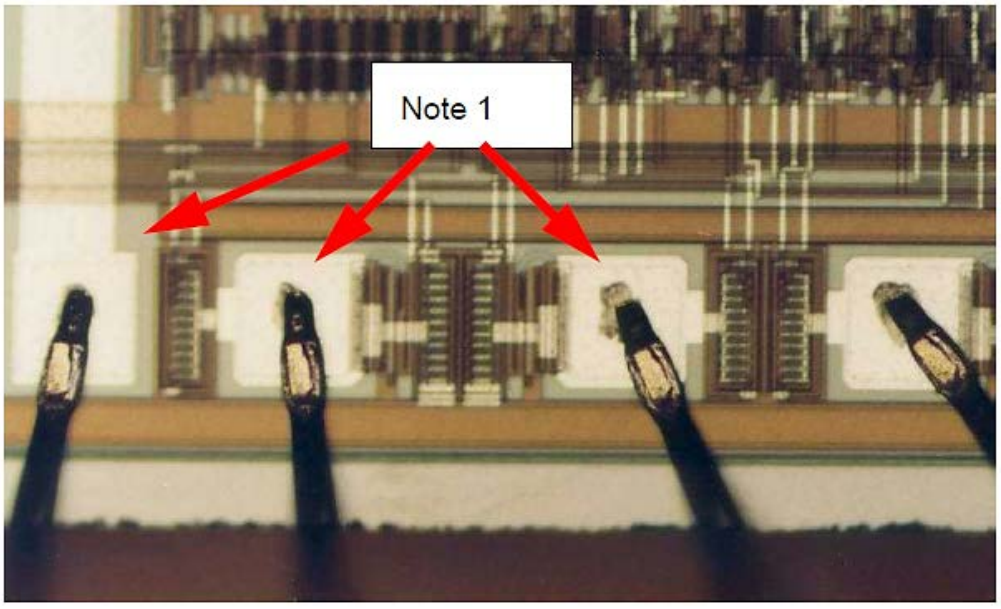


NOTE TO FIGURE 47

1. REJECT: Re-bonding is not allowed. Para. 4.10.1(a) refers.

(b) Bonds on the die where <75% of the bond is within the unglassivated bonding pad area. Not applicable for wedge bonding (see Para. 4.10.2).

FIGURE 48 - BOND POSITION

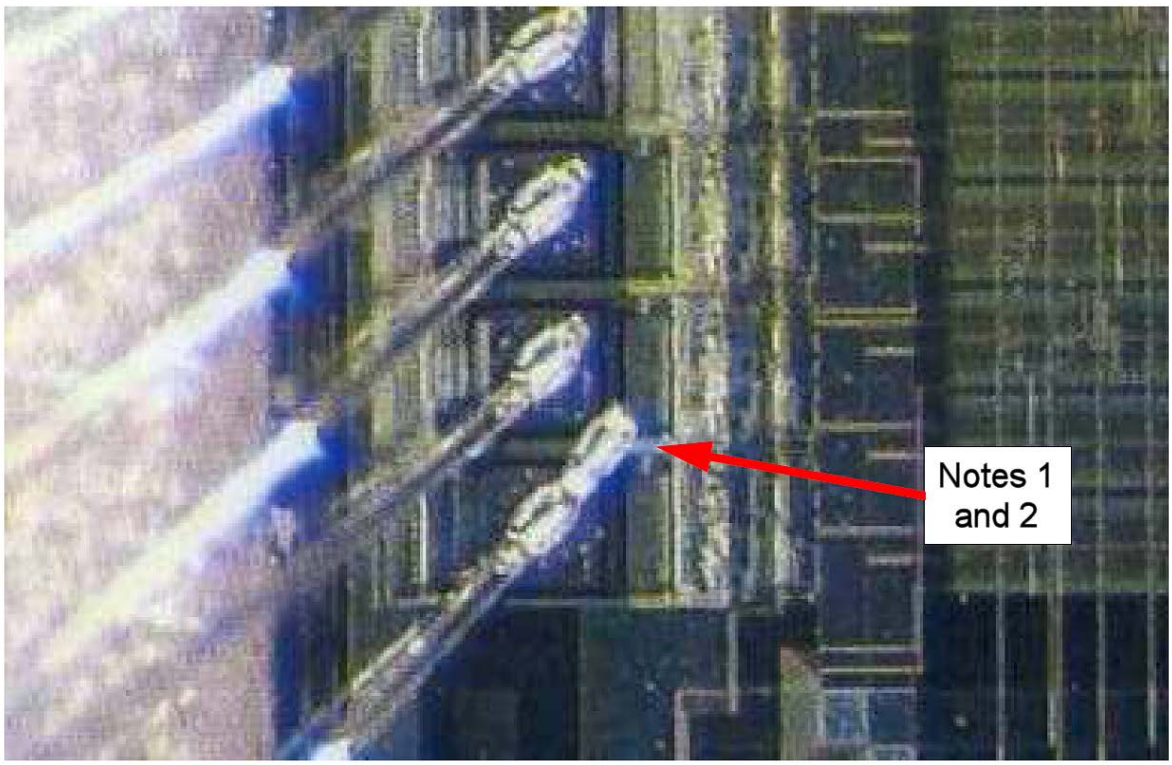


NOTE TO FIGURE 48

1. REJECT: <75% of the bond is within the bond pad area. Para. 4.10.1(b) refers.

(c) Bond tails, where no visible line of separation is evident between the tail and the unglassivated metallisation, another wire, bond, or bond tail, excluding common conductors and pads.

FIGURE 49 - BOND TAILS, VISIBLE SEPARATION LINE

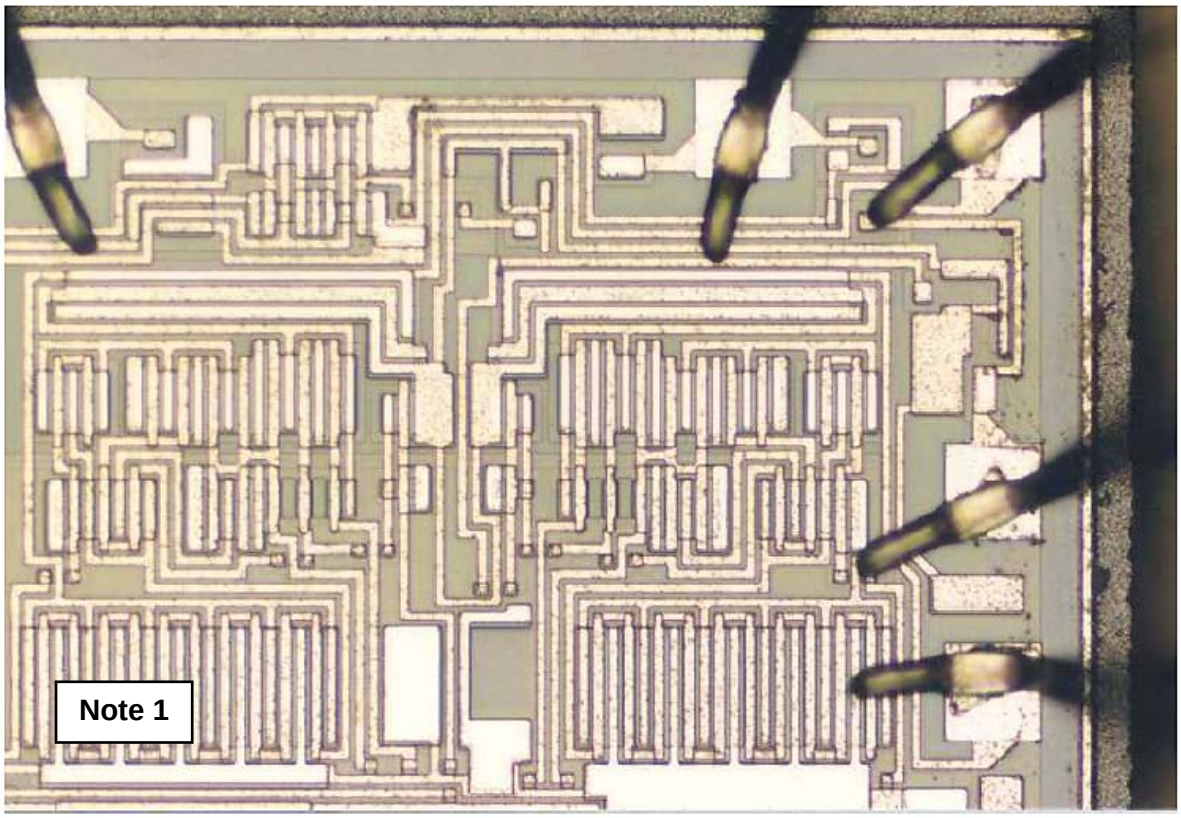


NOTES TO FIGURE 49

1. REJECT: No separation evident between tail and unglassivated metallisation. Para. 4.10.1(c) refers.
2. REJECT: Wire tail longer than 2 times wire diameter. Para. 4.10.1(d) refers.

(d) Bond tails, at the die or package post/lead, that exceed two wire diameters in length.

FIGURE 50 - BOND TAILS



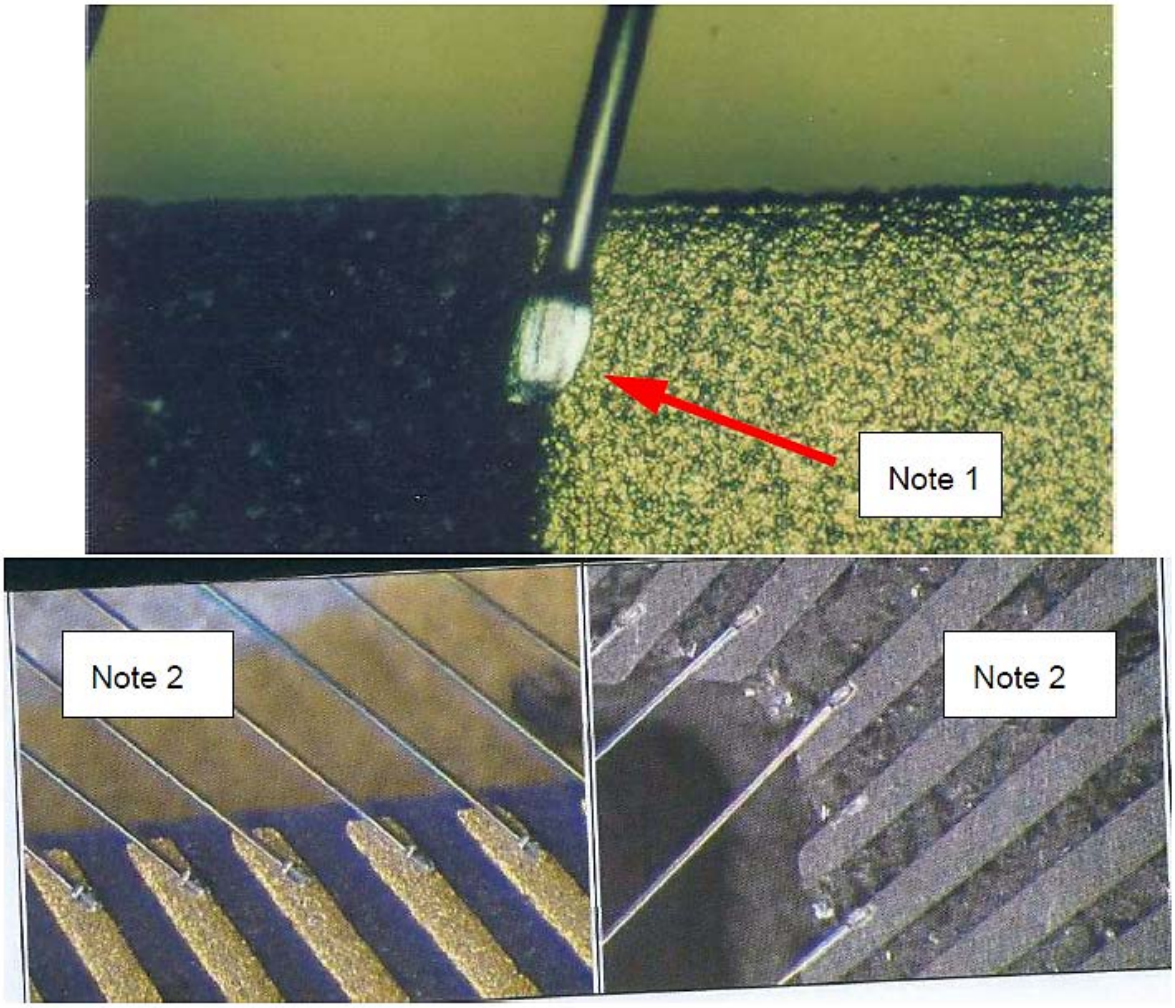
NOTE TO FIGURE 50

1. REJECT: Bond tails exceeding 2 wire diameters in length. Para. 4.10.1(d) refers.

(e) Bond tails extending over glassivated metallisation where the glass exhibits evidence of crazing or cracking that extends under the tail, excluding common conductors.

(f) Bonds that are not completely within the boundaries of the package post. For glass sealed packages, bonds not within 0.5mm of the end of the post.

FIGURE 51 - POST BOND

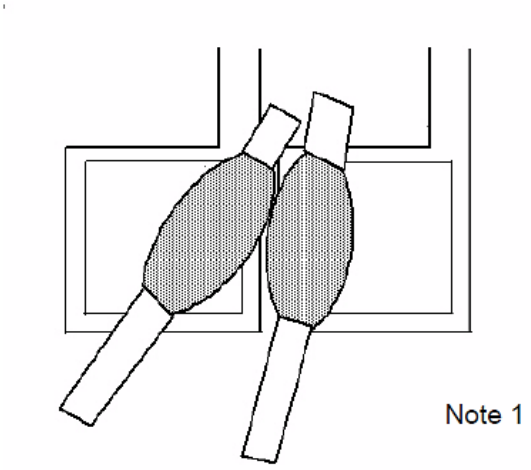


NOTES TO FIGURE 51

1. REJECT: Bond not completely within the boundaries of the post. Para. 4.10.1(f) refers.
2. ACCEPT: Bond completely within the boundaries of the post. Para. 4.10.1(f) refers.

(g) Bonds, excluding tails, placed so that no line of separation between bond and non-common metallisation, scribe lines, another bonding wire or bond is visible.
Note: When, by design, there are multiple bonds on a common bonding pad or post, they may not reduce the width of an adjacent bond by >25%.

FIGURE 52 - BOND SEPARATION



NOTE TO FIGURE 52

1. REJECT: No line of separation visible between bonds. Para. 4.10.1(g) refers.

(h) Bonds, excluding tails, placed such that there is no undisturbed metallisation line visible between the metallisation pad and any metallised stripe connected to this pad.
Note: When bond tails prevent visibility of the connecting path, and the metallisation immediately adjacent to the bond tail is disturbed, the device shall be unacceptable.

FIGURE 53 - BONDS AT THE METALLISATION EXIT

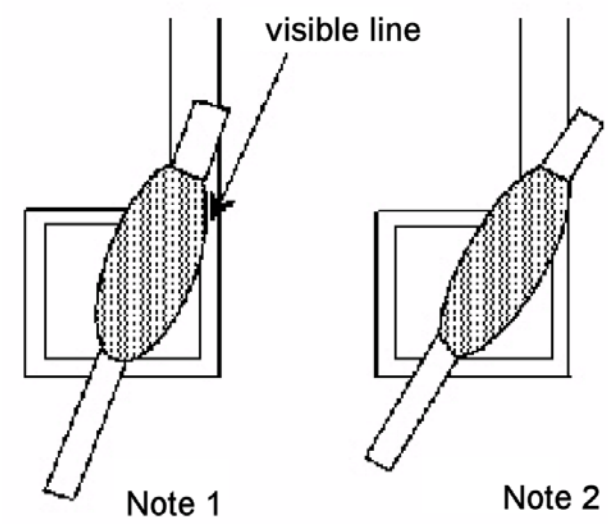
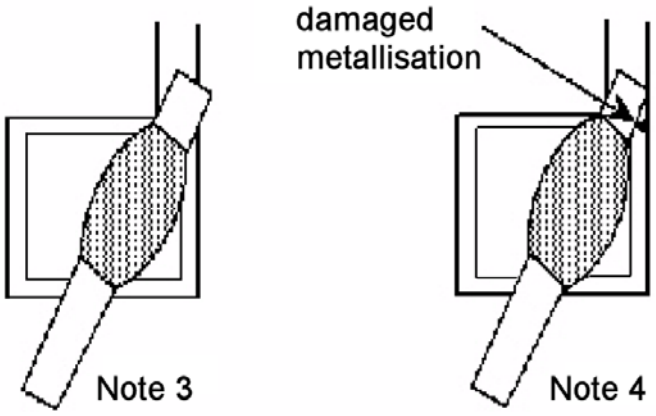


FIGURE 53 – BONDS AT THE METALLISATION EXIT (CONTINUED)

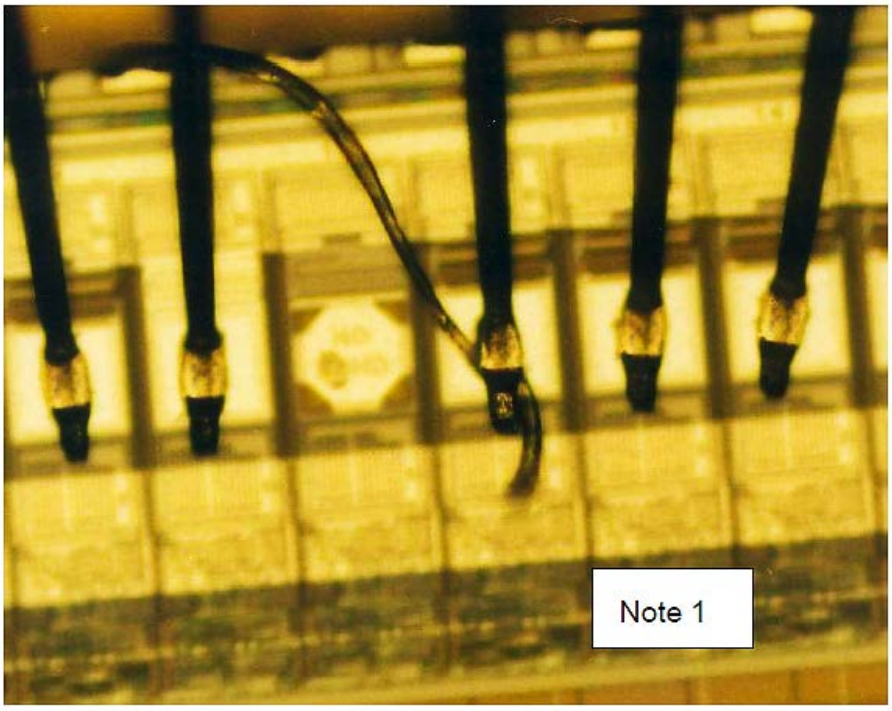


NOTES TO FIGURE 53

1. ACCEPT: Undisturbed metallisation line visible in the connecting path. Para. 4.10.1(h) refers.
2. REJECT: No undisturbed metallisation line visible in the connecting path. Para. 4.10.1(h) refers.
3. ACCEPT: Bond tail preventing visibility of connecting path but the metallisation immediately adjacent is undisturbed. Para. 4.10.1(h) refers.
4. REJECT: Bond tail preventing visibility of connecting path and the metallisation immediately adjacent is disturbed. Para. 4.10.1(h) refers.

(i) For bonds placed in the die attach cavity, a bond where >25% of the bond is located on die mounting material.
(j) Bonds placed so that the wire exiting from the bond crosses over another bond.
(k) Any evidence of repair of conductors by bridging with additional material.
(l) A bond overlapping another bond, bond wire or residual segment of lead wire.
(m) Intermetallic formation extending in >2.5µm completely around the periphery of that portion of the bond located on metal.
(n) Bonds on foreign material.

FIGURE 54 - BONDS ON FOREIGN MATERIAL

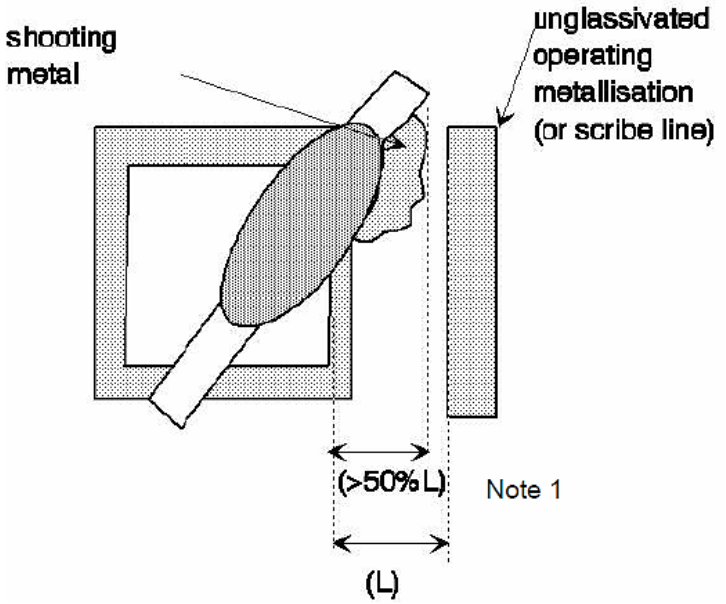


NOTE TO FIGURE 54

1. REJECT: Bond on foreign material. Para. 4.10.1(n) refers.

(o) Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) but is still connected to the bonding pad, if it reduces the original separation between unglassivated operating metallisation, or scribe line and the bonding pad, to <50% of the design separation.

FIGURE 55 - DISPLACED METAL

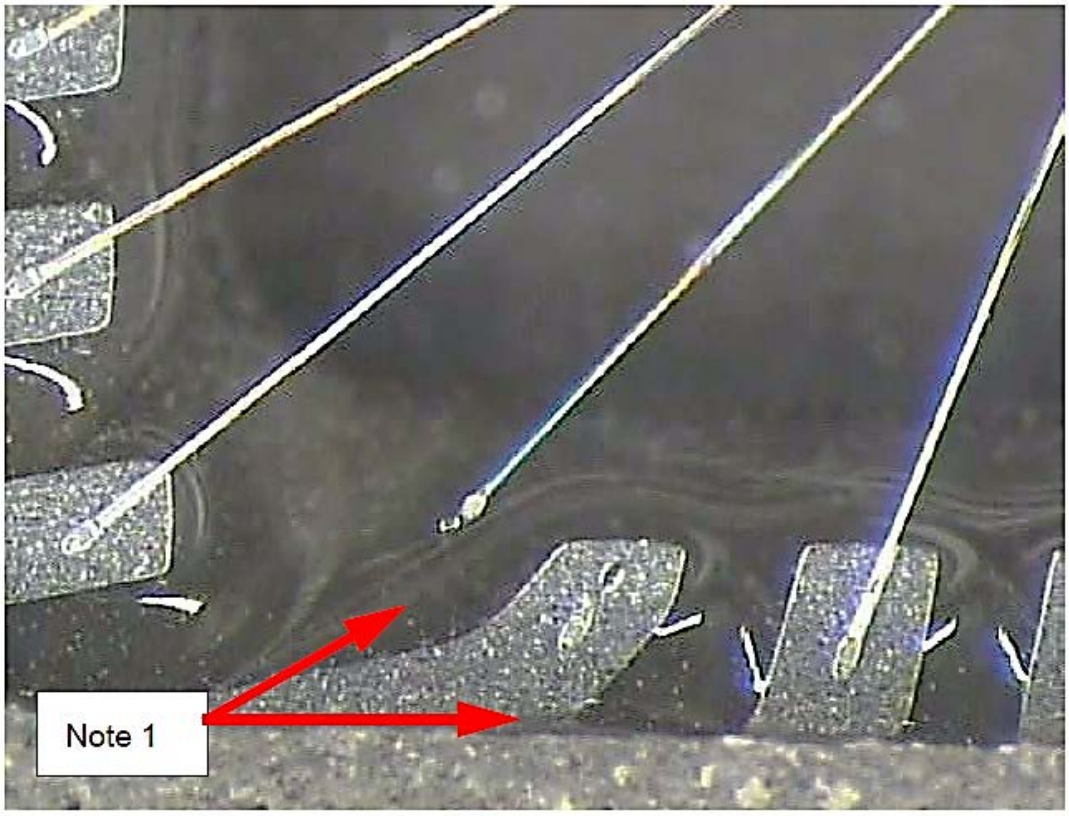


NOTE TO FIGURE 55

1. REJECT: Shooting metal reducing the separation from operating metallisation to <50% of the original separation. Para. 4.10.1(o) refers.

(p) Bond lifting or tearing at the interface of the pad and wire. This criterion is applicable to single bonds and any part of a double bond.

FIGURE 56 - BOND LIFTING AND TEARING

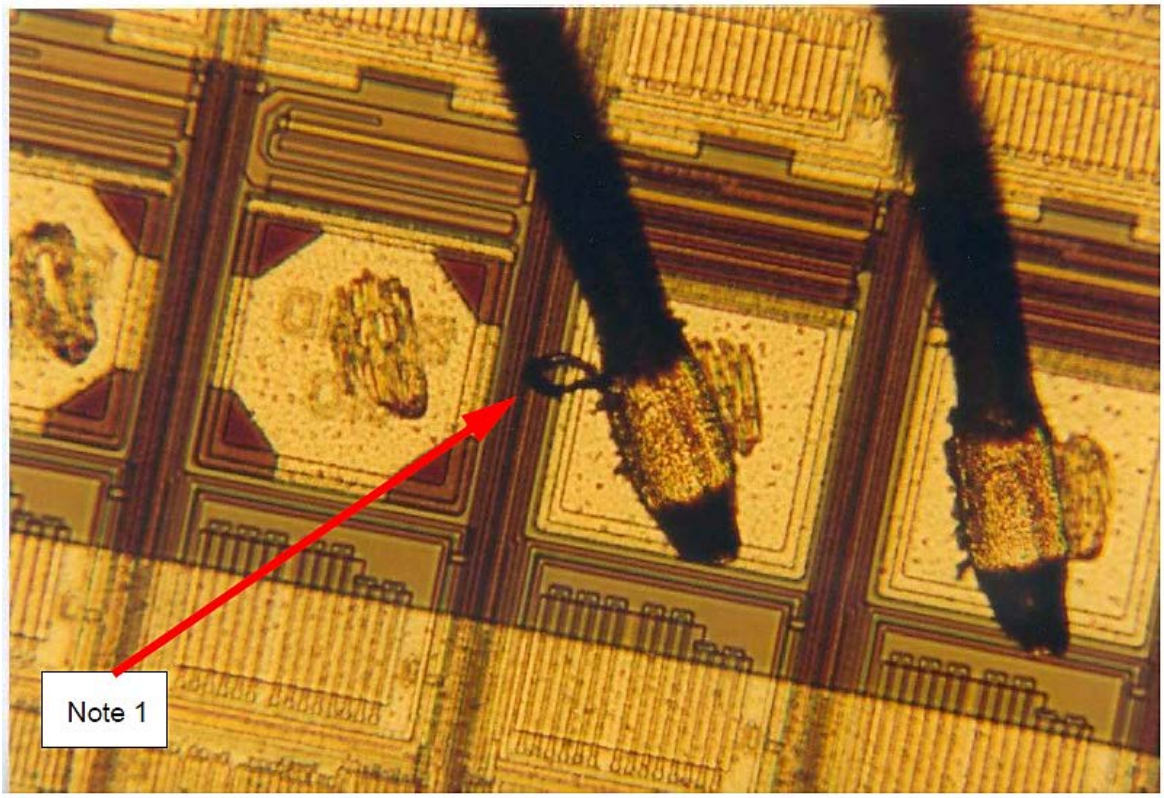


NOTE TO FIGURE 56

1. REJECT: Bond is lifted. Para. 4.10.1(p) refers.

(q) Presence of aluminium whisker(s) greater than the minimum distance between two conducting areas.

FIGURE 57 - ALUMINIUM WHISKER(S)



NOTE TO FIGURE 57

1. REJECT: Presence of aluminium whisker(s) greater than the distance between two conducting areas. Para. 4.10.1(q) refers.

(r) Multicoloured stains in the bonding pad area. Multicoloured stains appearing along the periphery of the etch line are acceptable, provided that the unstained metallisation is not reduced to <75% of the bonding pad area.

Acceptable Observation

(1) Bond tails extended on top of glassivated metallisation remain acceptable as long as other associated criteria are satisfied.

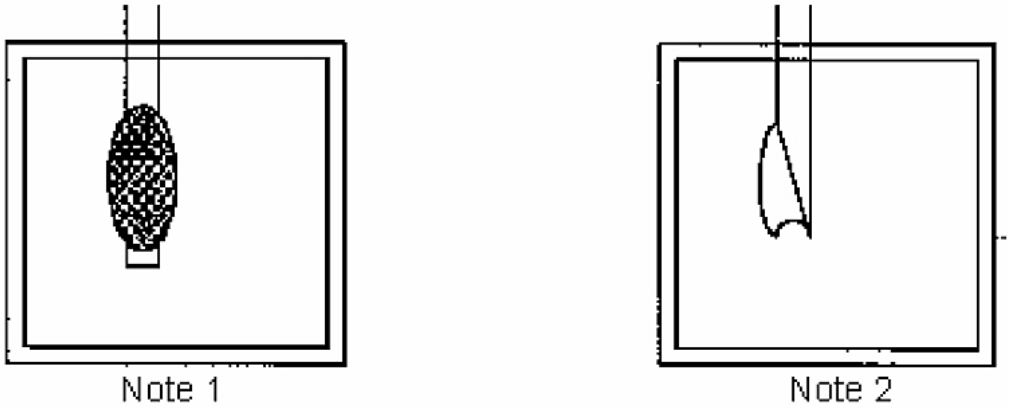
4.10.2 Wedge Bonds

(a) Ultrasonic bonds on the die or package post that are <1.2 times or >3 times the wire diameter in width, or are <1.5 times or >6 times the wire diameter in length (see Figure 46).

(b) Thermocompression wedge bonds on the die or package post that are <1.5 times or >3 times the wire diameter in width, or are <1.5 times or >6 times the wire diameter in length (see Figure 46).

(c) Wedge bonds where the tool impression does not cover the entire width of the wire.

FIGURE 58 - PARTIAL TOOL IMPRESSION

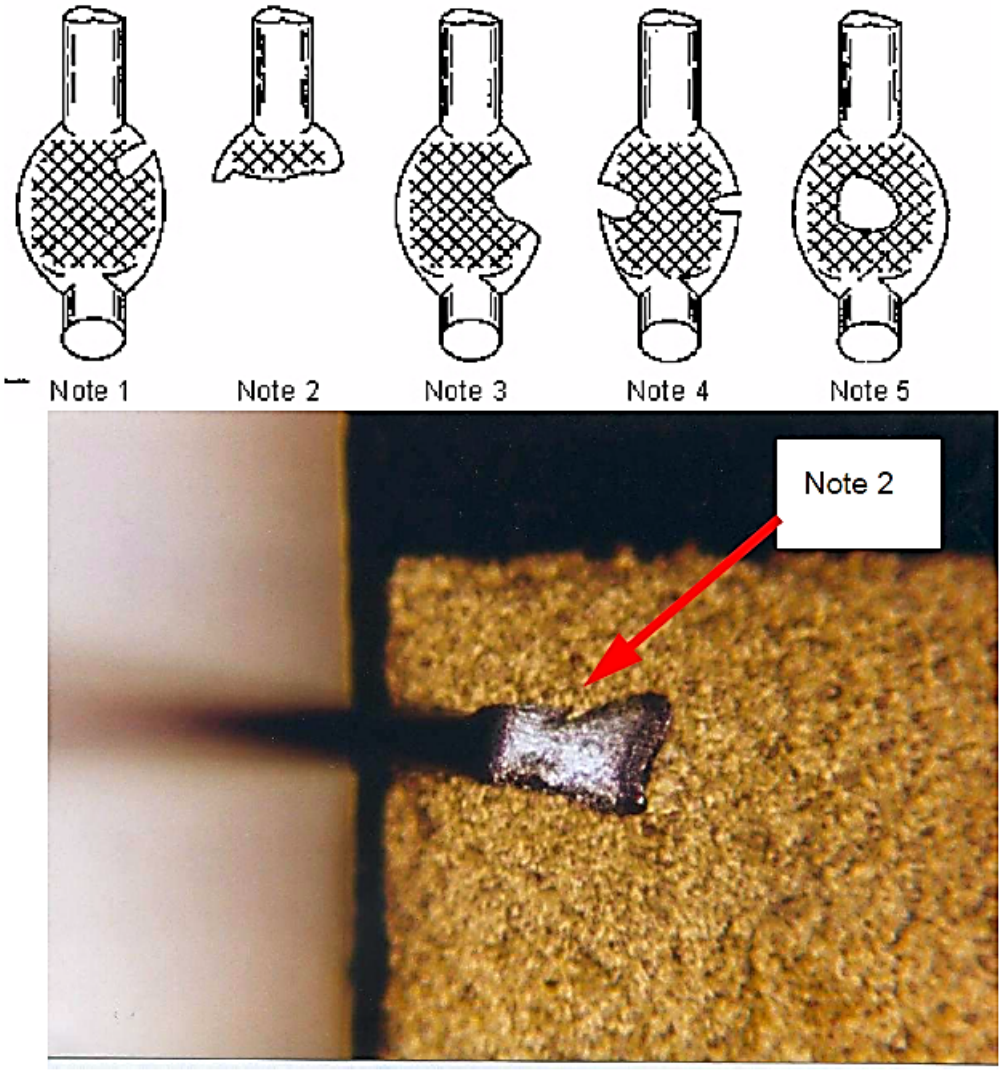


NOTES TO FIGURE 58

1. ACCEPT: tool impression covers the entire width of the wire. Para. 4.10.2(c) refers.
2. REJECT: tool impression does not cover the entire width of the wire. Para. 4.10.2(c) refers.

(d) For Aluminium wires, 50µm or greater in diameter, bond width <1 times the wire diameter.
(e) Pad bond torn in the bond area or behind the bond. (See Figure 59).
(f) Nicks in the side of the bond or holes in the centre of the bond.

FIGURE 59 - TORN AND INCOMPLETE BONDS

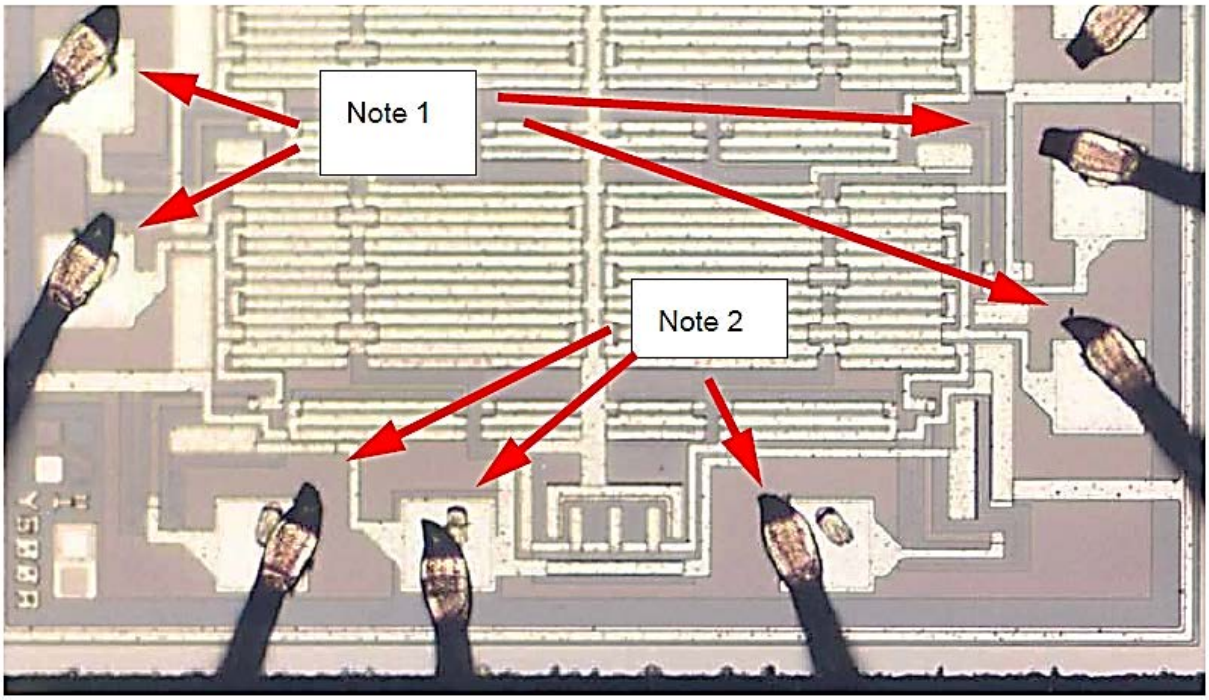


NOTES TO FIGURE 59

1. REJECT: Nick in the side of a bond. Para. 4.10.2(f) refers.
2. REJECT: Bond torn in the bond area. Para. 4.10.2(e) refers.
3. REJECT: Nick in the side of a bond. Para. 4.10.2(f) refers.
4. REJECT: Nick in the side of a bond. Para. 4.10.2(f) refers.
5. REJECT: Hole in the centre of the bond. Para. 4.10.2(f) refers.

(g) If the bond is smaller than the pad area, ≥75% of the tool impression of the pad bond must be bonded to the metallisation.

FIGURE 60 - TOOL IMPRESSION OUTSIDE BONDING PAD



NOTES TO FIGURE 60

1. ACCEPT: ≥75% of tool impression bonded to metallisation. Para. 4.10.2(g) refers.
2. REJECT: <75% of tool impression bonded to metallisation. Para. 4.10.2(g) refers.

(h) If the bond is larger than the pad area, <50% of the tool impression of the pad bond appearing on the area of the pad.

4.10.3 Tailless Bonds (Crescent, Terminating Capillary Bond)

(a) Bonds on the die or package post that are <1.2 times or >5 times the wire diameter in width, or are <0.5 times or >3 times the wire diameter in length (see Figure 46).

(b) Bonds where bond impression does not cover the entire width of the wire.

4.10.4 Gold Ball Bonds

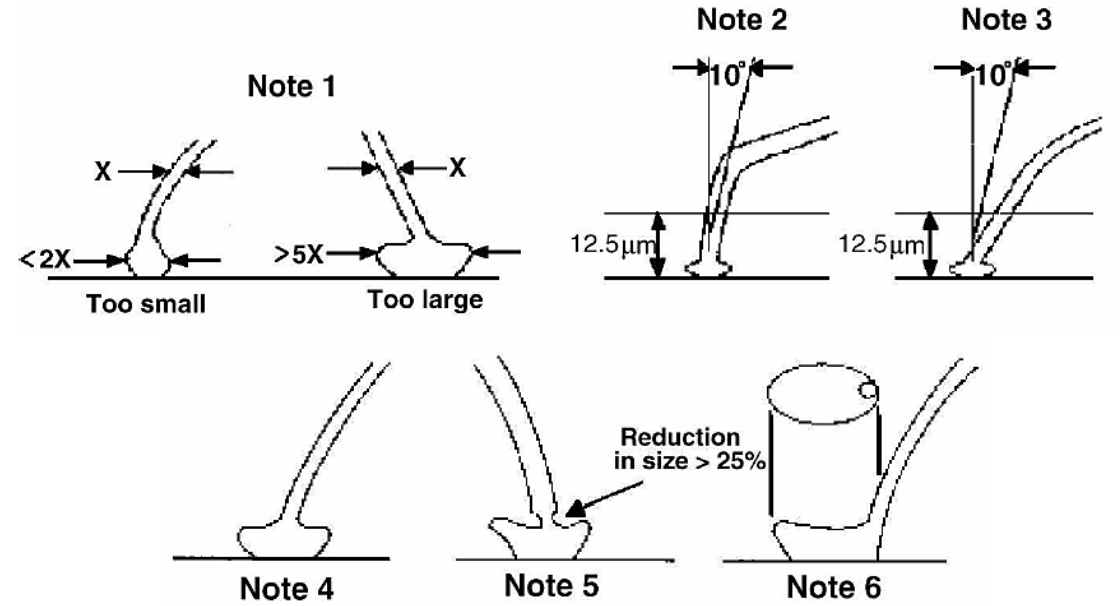
(a) Ball Bonds on the die or package post where the ball bond diameter is <2 times or >5 times the wire diameter (see Figure 61).

(b) Wire not within 10° of the perpendicular to the surface of the chip for a distance of >12.5µm before bending towards the package post or other terminating point (see Figure 61).

(c) A reduction in the diameter of the wire of >25% where the wire contacts the ball (see Figure 61).

(d) Bonds where the wire exit is not completely within the periphery of the ball.

FIGURE 61 - BALL BONDS



NOTES TO FIGURE 61

1. REJECT: Ball bond diameter either too small or too large. Para. 4.10.4(a) refers.
2. ACCEPT: Wire within 10° of perpendicular to the chip surface for at distance >12.5µm. Para. 4.10.4(b) refers.
3. REJECT: Wire not within 10° of perpendicular to the chip surface. Para. 4.10.4(b) refers.
4. ACCEPT: No reduction in wire diameter where the wire contacts the ball. Para. 4.10.4(c) refers.
5. REJECT: A reduction in wire diameter of >25% where the wire contacts the ball. Para. 4.10.4(c) refers.
6. REJECT: Wire exits from edge of ball.

(e) Bonds where the wire centre exit is not within the boundaries of the unglassivated bonding pad area.

(f) Intermetallic formation extending more than 2.5 m completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.

(g) A wire from the ball bond which does not leave the die vertically without kinking or otherwise departing from a smooth line and does not begin to curve towards the post before reaching two thirds of the post height.

(h) The wire from the ball bond on the die rising to >4/3 of the post height. The requirement of the excessive loop sag must still be met (Para. 4.11.3(c)).

(i) <2/3 of the ball in contact with the pad.

4.11 INTERNAL LEADS

4.11.1 Wires

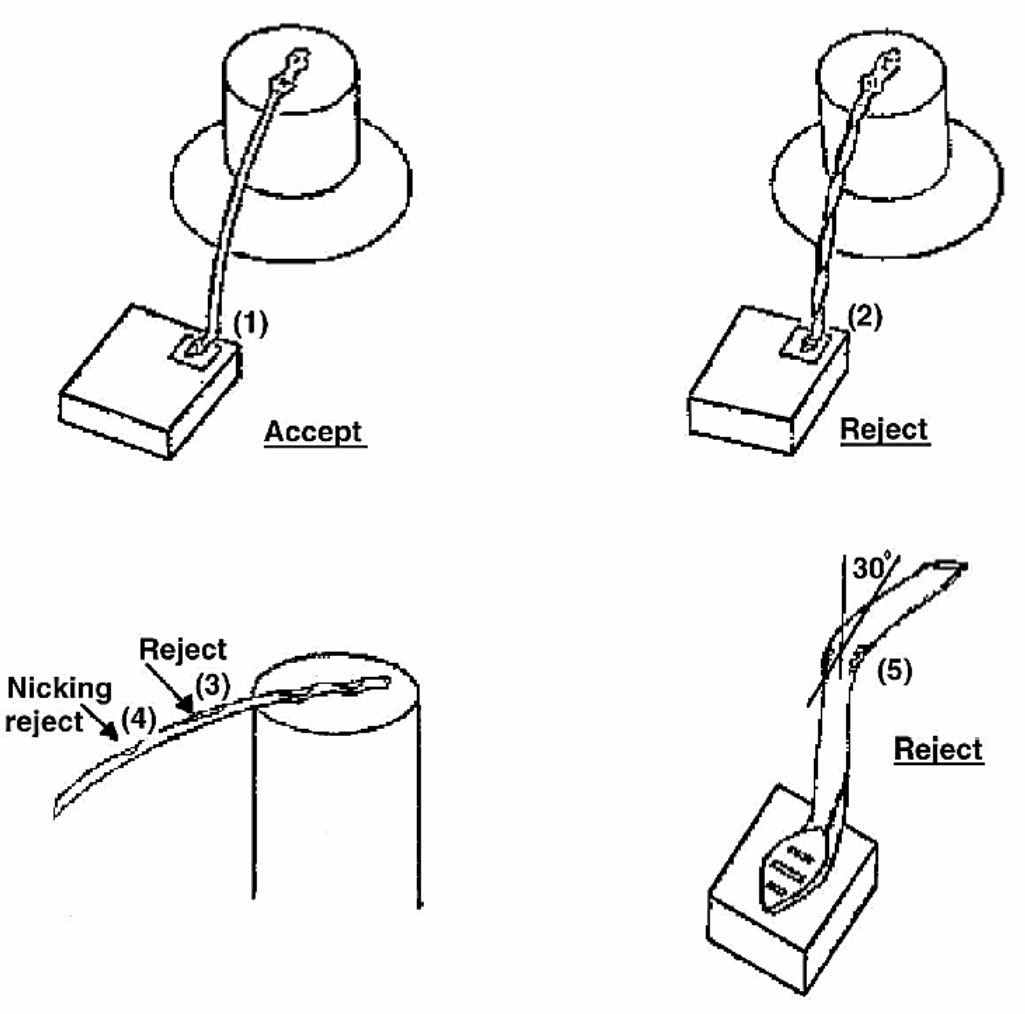
(a) Any wire with a separation of <1 wire diameter to unglassivated operating metallisation, other bonds, another wire (common wires excluded), package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any portion of the package, including the plane of the lid to be attached. Within a 120µm radial distance from the perimeter of the bond on the die, the separation shall be 2.5µm minimum. Smaller distances are acceptable if justified by design.

(b) Wire twisted >360° from the pad post to the pillar bond.

(c) Nicks, bends, cuts, crimps, scoring or neck-down in any wire that reduces the wire diameter by >25%.

(d) Any wire exhibiting a kink of exterior angle >30°.

FIGURE 62 - GENERAL BOND DEFECTS



NOTES TO FIGURE 62

1. ACCEPT: No twist. Para. 4.11.1(b) refers.
2. REJECT: 360° twist. Para. 4.11.1(b) refers.
3. REJECT: Crimp reduces wire diameter by >25%. Para. 4.11.1(c) refers.
4. REJECT: Nick reduces wire diameter by >25%. Para. 4.11.1(c) refers.
5. REJECT: Kink with exterior angle >30°. Para. 4.11.1(d) refers.

(e) Wire(s) not in accordance with bonding diagram with clear evidence of missing or extra lead wires.
(f) Tearing at the junction of the wire and bond or lifted bonds.
(g) Excessive loops, bows or sags in any wires such that they could short to another wire, pad package post, die or touch any portion of the package.
(h) Wire(s) crossing wire(s), except common conductors, when viewed from above, except in multitiered packages, where the crossing occurs within the boundary of the lower wire bond tier(s) being crossed or packages with down bond(s). In these situations, the wires that cross are acceptable if they maintain a minimum clearance of 1 wire diameter.

FIGURE 63 - CRITERIA FOR WIRE(S) CROSSING WIRE(S)

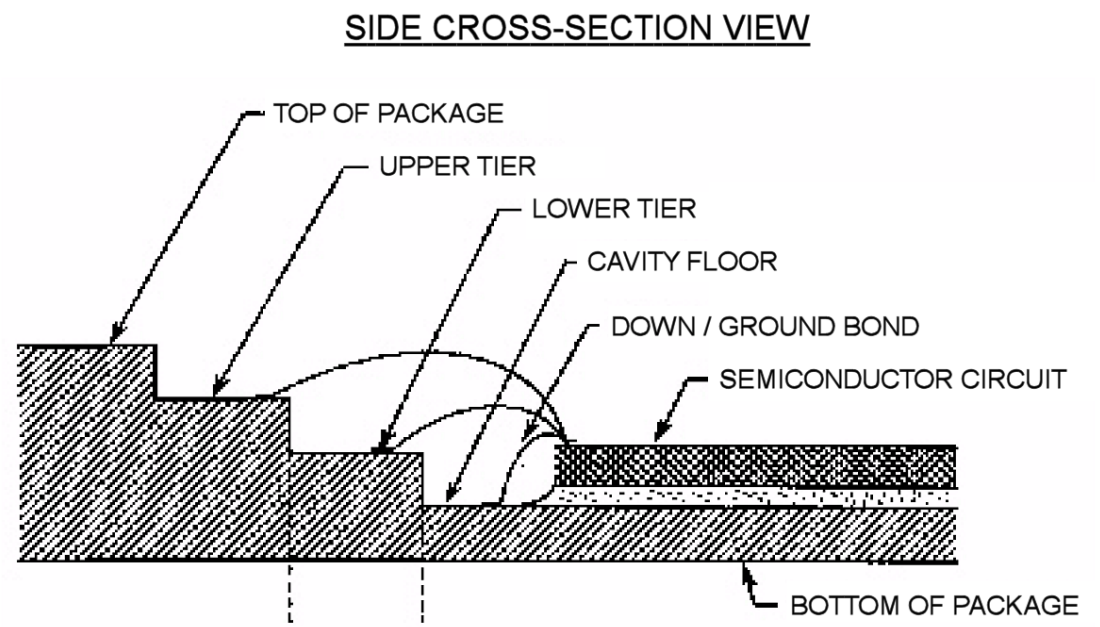
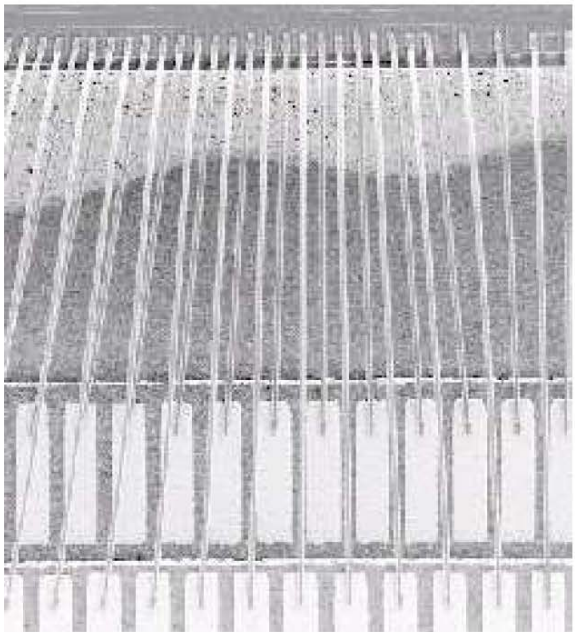
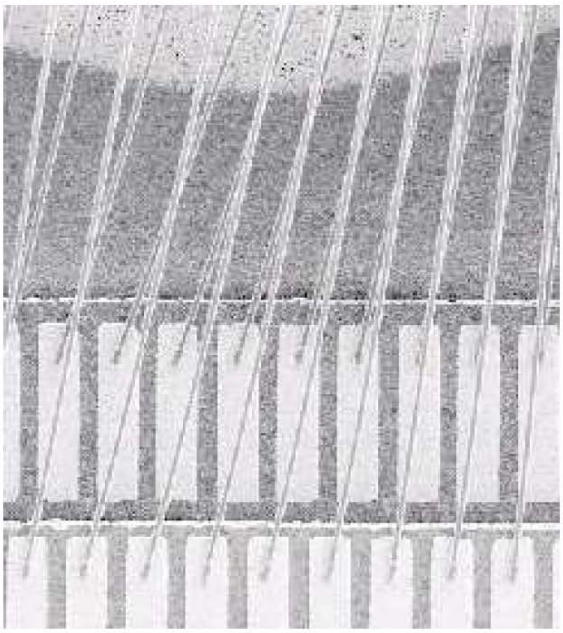


FIGURE 63 – CRITERIA FOR WIRE(S) CROSSING WIRE(S) (CONTINUED)

TOP VIEW



Note 1



Note 2

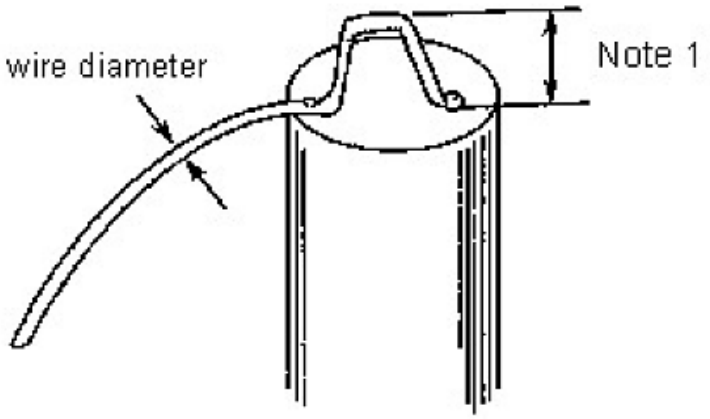
NOTES TO FIGURE 63

1. ACCEPT: No crossing of bond wires. Para. 4.11.1(h) refers.
2. ACCEPT: If minimum clearance between wires crossing is >1 wire diameter.
   REJECT: If minimum clearance between wires crossing is <1 wire diameter. Para. 4.11.1(h) refers.

(i) For ball bonded devices, wire not within 10° of the perpendicular to the surface of the chip for the distance >12.5µm.

(j) A bow or loop between double bonds at post >4 x wire diameter.

FIGURE 64 - LOOP BETWEEN DOUBLE BOND



NOTE TO FIGURE 64

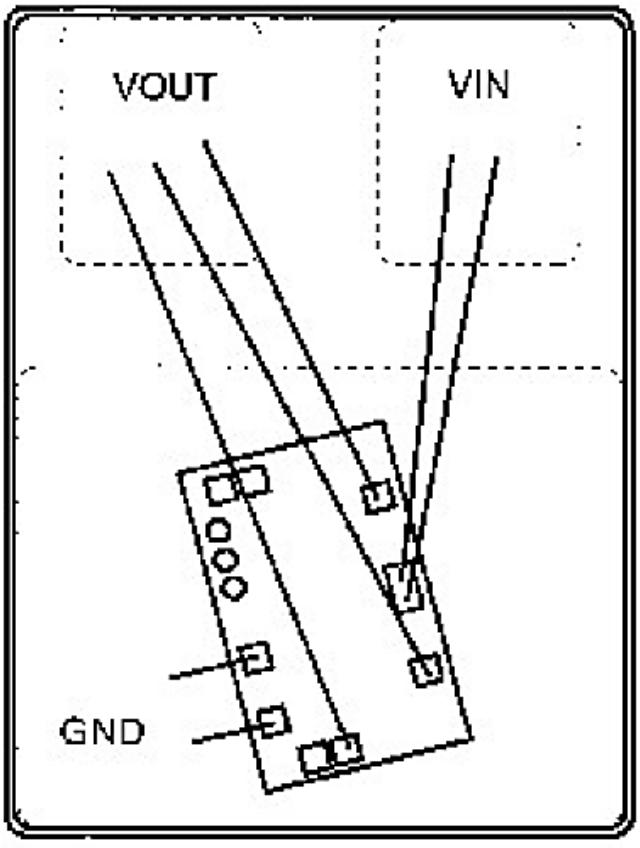
1. REJECT: Loop >4 x wire diameter. Para. 4.11.1(i) refers.

(k) Bond wires which do not clear the die edge by at least one (1) wire diameter unless justified by design.

Acceptable Observation

(1) A wire crossing over the die is considered acceptable if it is still in accordance with the approved bonding diagram and does not prevent the inspection of the die.

FIGURE 65 - WIRE CROSSING OVER THE DIE



Note 1

NOTE TO FIGURE 65

1. ACCEPT: Wires crossing over the die in accordance with bonding diagram and do not prevent inspection. Para. 4.11.1(1) refers.

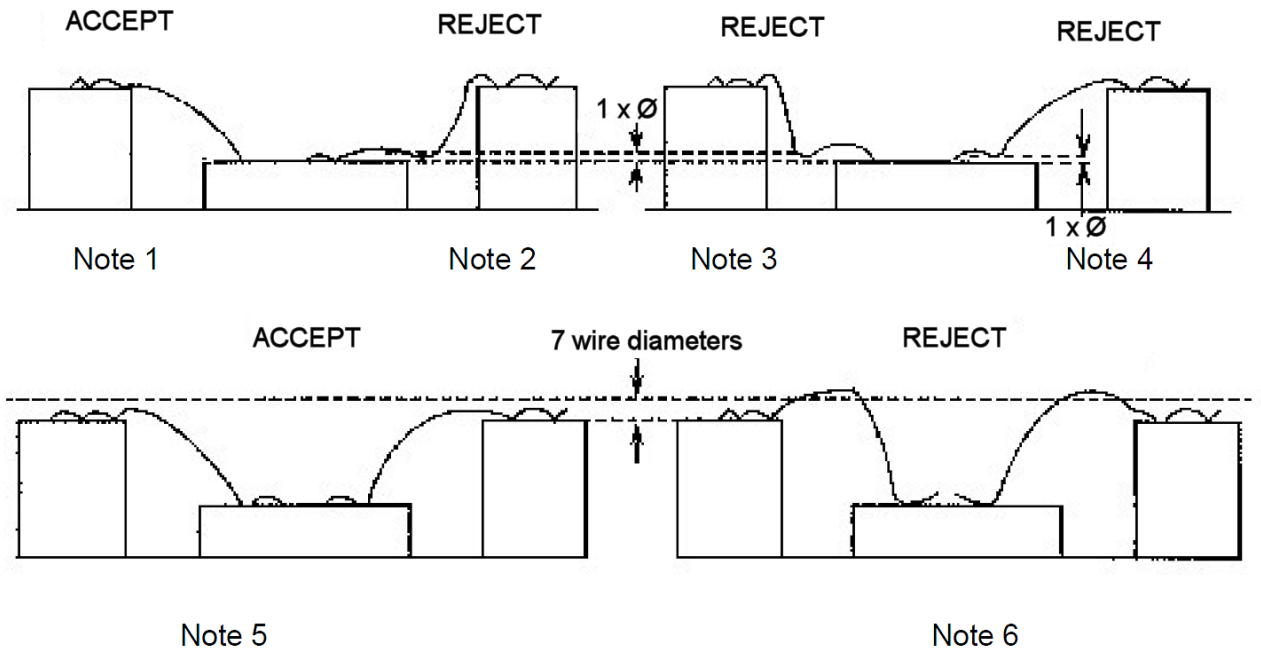
4.11.2 Up-Bonding

(a) Wire not travelling in a smooth upward arc from the pad bond to the edge of the die and clearing the edge by less than one (1) wire diameter (See Figure 66).

(b) Wire sagging below a line parallel to the top of the header and one (1) wire diameter above the top of the die (See Figure 66).

(c) Wire rising >seven (7) wire diameters above the top of the pillar.

FIGURE 66 - UP-BONDING



NOTES TO FIGURE 66

1. ACCEPT: Proper arc and clearance. Para. 4.11.2(a) refers.
2. REJECT: Clearance <1 x wire diameter Para. 4.11.2(a) refers.
3. REJECT: No rising in a smooth upward arc. Para. 4.11.2(a) refers.
4. REJECT: Sags below 1 x wire diameter above die top Para. 4.11.2(b) refers.
5. ACCEPT: Rises <7 x wire diameter. Para. 4.11.2(c)refers.
6. REJECT: Rises >7 x wire diameter. Para. 4.11.2(c) refers.

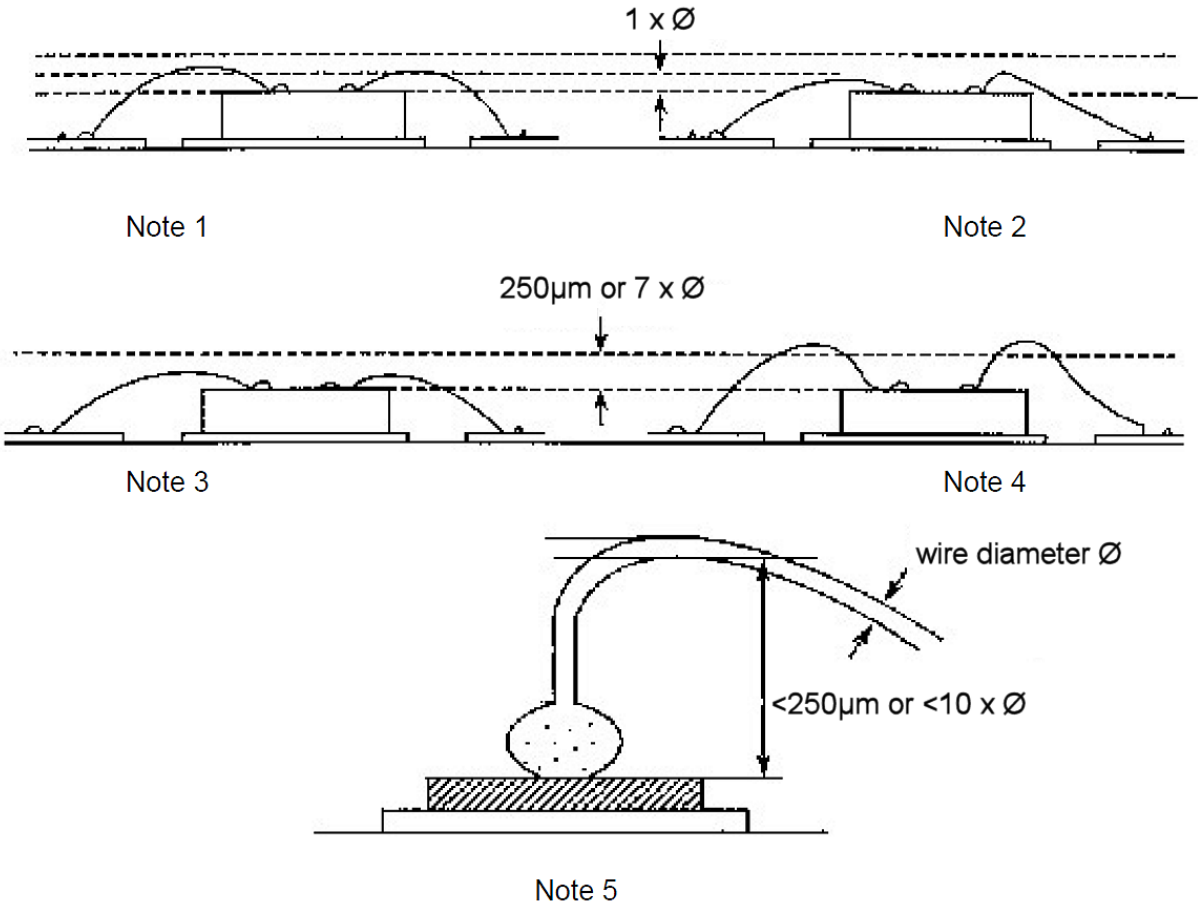
4.11.3 Down-Bonding

(a) Wire not travelling in smooth arc from the bond to the edge of the die and clearing the edge by one (1) wire diameter (see Figure 67).

(b) For ultrasonic bonding: Wire rising >250µm or seven (7) wire diameters, whichever is the less, above the top of the die (see Figure 67).

(c) For gold ball bonding: Gold wire rising >250µm or 10 wire diameters whichever is less above the top of the die.

FIGURE 67 - DOWN-BONDING



NOTES TO FIGURE 67

1. ACCEPT: Proper arc and clearance. Para. 4.11.3(a) refers.
2. REJECT: Clearance <1 x wire diameter. Para. 4.11.3(a) refers.
3. ACCEPT: Proper arc and clearance. Para. 4.11.3(b) refers.
4. REJECT: Wire rising >250µm or 7 x wire diameters. Para. 4.11.3(b) refers
5. ACCEPT: <250µm or <10 x wire diameter above top of the die. Para. 4.11.3(c) refers.

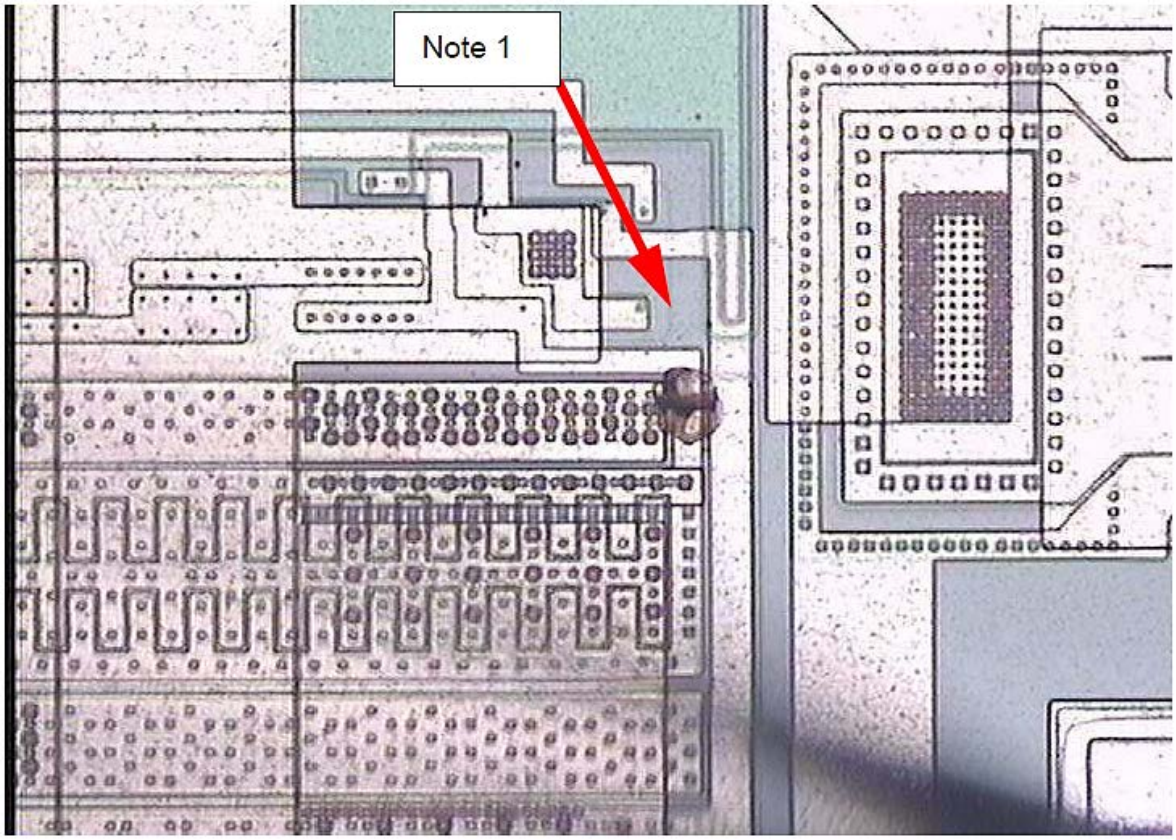
4.12 FOREIGN MATERIAL

Die inspection shall be at high magnifications while package cavity inspection may be at low magnifications.

(a) Non-attached and non-embedded foreign particle(s) that is/are large enough to bridge the narrowest spacing between unglassivated operating material (metallisation, bare semiconductor material, mounting material, bonding wire, etc.).
Note: Chips of semiconductor material shall be considered as foreign particles.

(b) Visible foreign material attached to, or embedded in, the die surface that appears to bridge the active circuit elements including metallisation. Suspected particles shall cause rejection unless verified as only attached to the surface of the die, but not embedded, by high power dark field illumination.

FIGURE 68 - VISIBLE FOREIGN MATERIAL

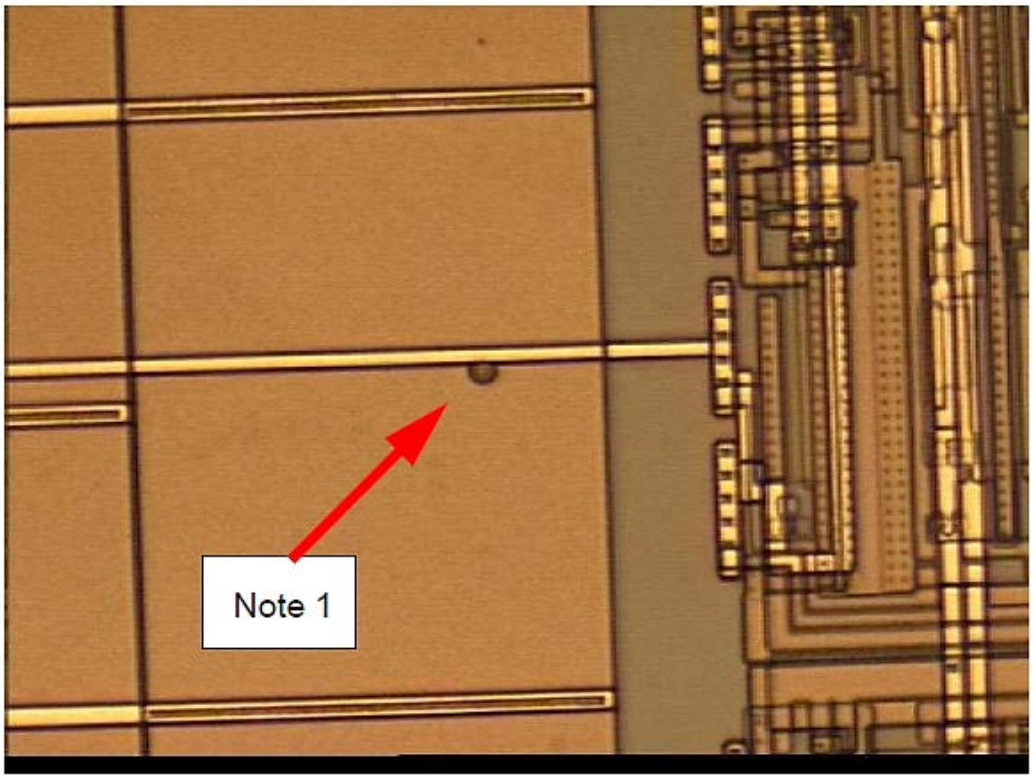


NOTE TO FIGURE 68

1. REJECT: Evidence of foreign material attached to the die surface. Para. 4.12(b) refers.

(c) Any device that exhibits a protuberance (metal aspect) on a level n metallisation path on a step created by a level n-1 metallisation path. Example: metal 3 on metal 2; metal 2 on metal 1; metal 1 on polysilicon; polysilicon on silicon.

FIGURE 69 - METAL ASPECT

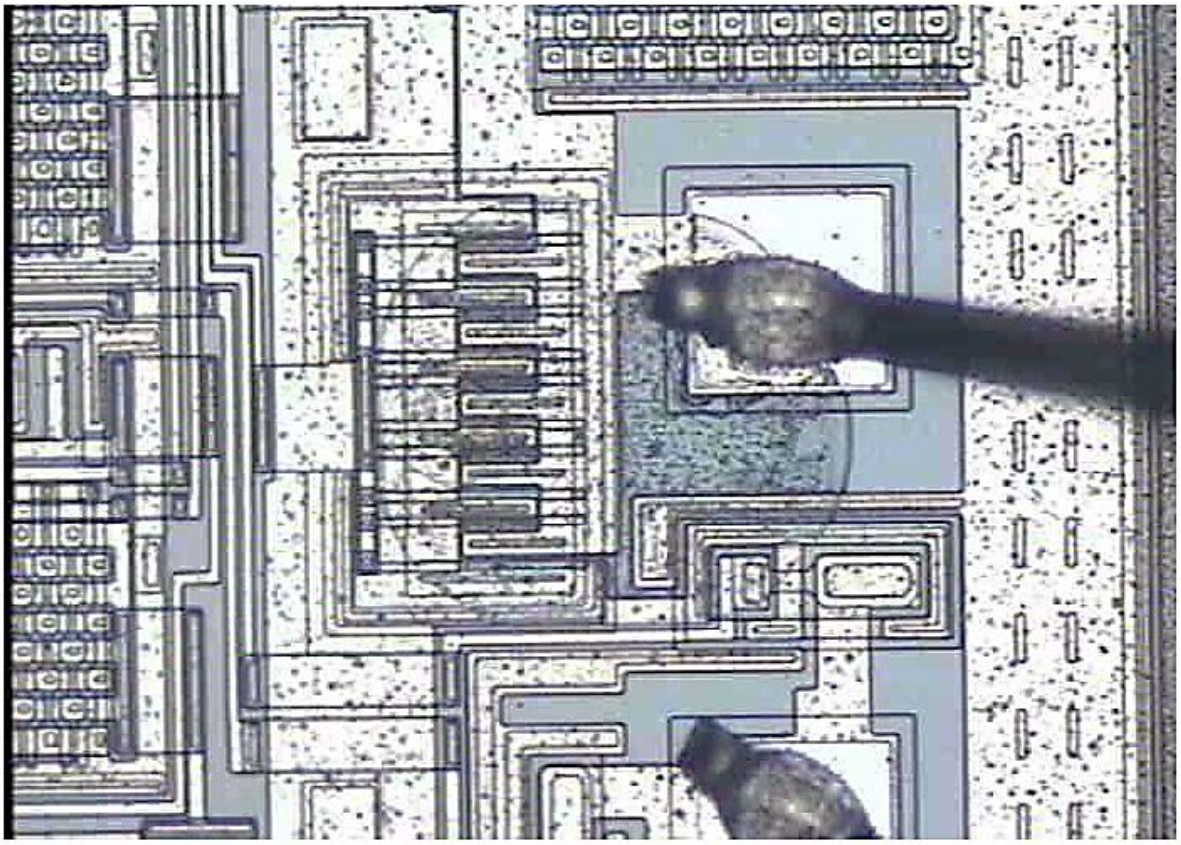


NOTE TO FIGURE 69

1. REJECT: Evidence of metal aspect. Para. 4.12(c) refers.

(d) Liquid droplets, chemical stains, ink or photoresist on the die surface that appears to bridge any combination of unglassivated metallisation or bare areas of semiconductor material.

FIGURE 70 - LIQUID DROPLETS



NOTE TO FIGURE 70

1. REJECT: Evidence of liquid droplet. Para. 4.12(d) refers.

(e) Foreign material, that is attached to the backside and might affect the die picking or the die attach procedure.

(f) A particle of gold eutectic material, package ceramic material or semiconductor material, not attached to the die, large enough to bridge the narrowest spacing between unglassivated operating materials, that does not exhibit ≥50% cumulative peripheral fillet or whose height is greater than the longest base dimension.
Note: Gold imperfections in the die attach area that do not interfere with proper die attachment, sealing glass splatter (provided it does not suggest inadequately controlled process and does not interfere with the die attach area) or internal glass runout from frit seal (provided it is confined to package walls and does not interfere with the die attach area) are acceptable.

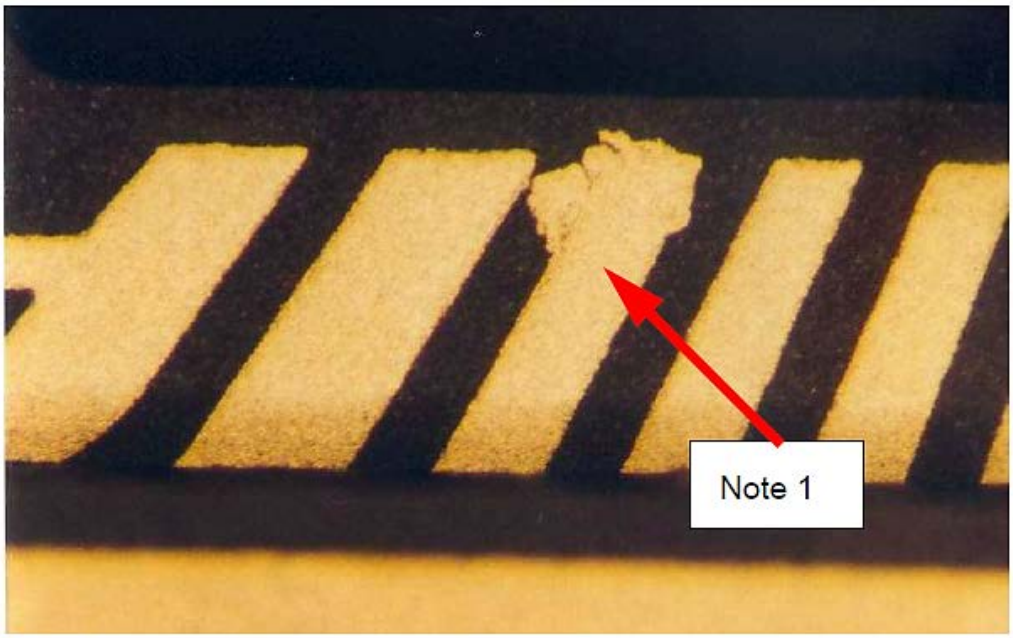
Acceptable Observation

(1) If the protuberance is shown on a step created by a level n-2 or n-3 metallisation path, the defect is acceptable if the width of the protuberance is <25% of the original metallisation path width (see also Para. 4.12(c)).

4.13 PACKAGE AND HEADER DEFECTS

(a) Blistering or flaking of the plating or package or leads.
(b) Contamination, such as grease, varnish, ink, resin, on the insulation (ceramic, glass etc.).
(c) Excess metallisation which reduces the insulation separation by >50%.

FIGURE 71 - EXCESS METALLISATION

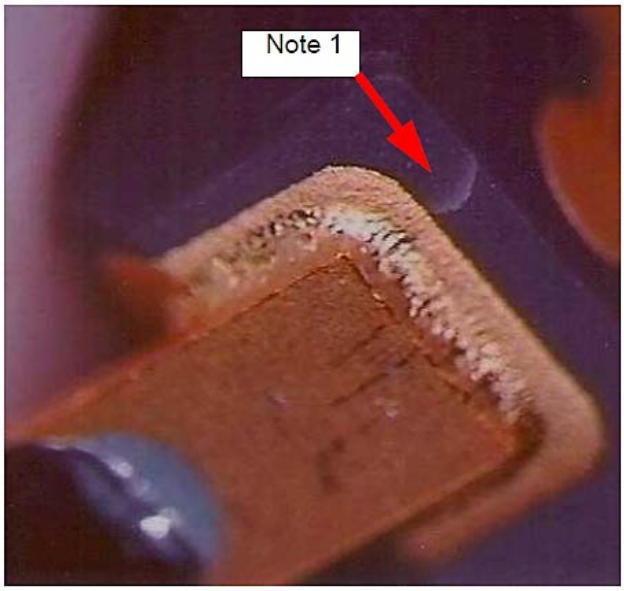


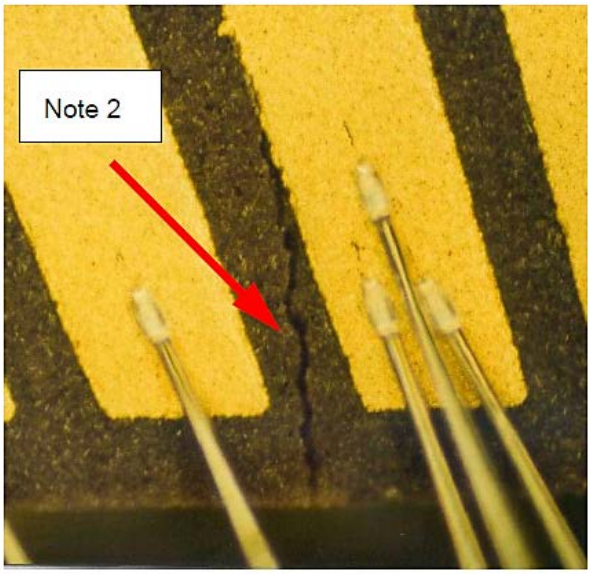
NOTE TO FIGURE 71

1. REJECT: Excess metallisation reducing the insulation separation by >50%. Para. 4.13(c) refers.

(d) Metal residue on the flange, rim or other cap sealing area with any dimension greater than the width of the sealing/welding area.
(e) Corrosion of the package, header or can
(f) Cracks in the ceramic body.

FIGURE 72 - CRACKS IN CERAMIC BODY



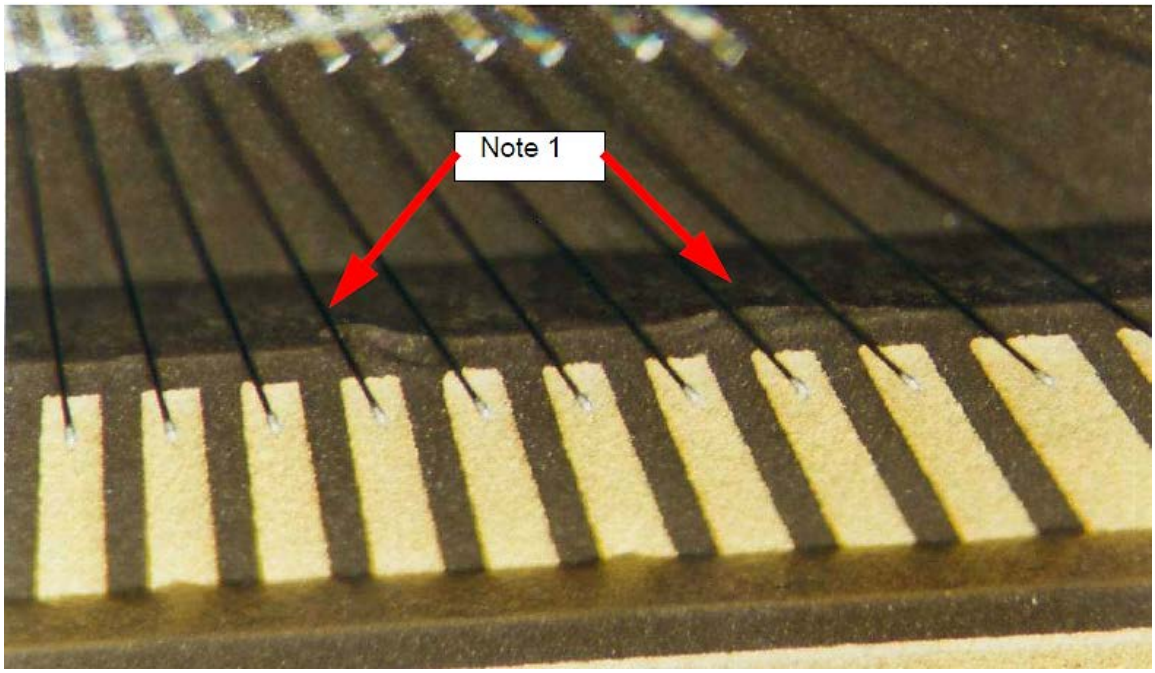


NOTES TO FIGURE 72

1. REJECT: Crack in ceramic body. Para. 4.13(f) refers.
2. REJECT: Crack in ceramic body between the bonding posts. Para. 4.13(f) refers.

(g) Mechanical damage.

FIGURE 73 - MECHANICAL DAMAGE



NOTE TO FIGURE 73

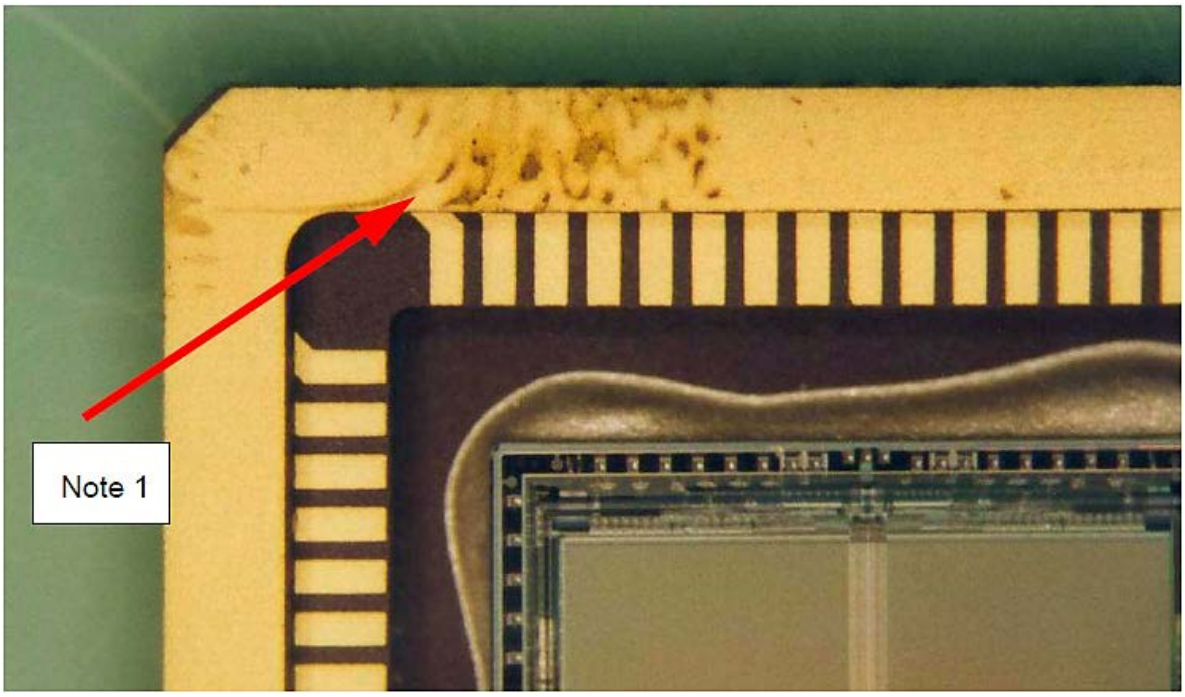
1. REJECT: Evidence of mechanical damage. Para. 4.13(g) refers.

(h) Radial cracks that extend in excess of a third of the distance from the pin to the outer member of the seal.

(i) Cracks in the circumference, except the meniscus, that extend >90° about the seal centre.

(j) Contamination on the flange, rim or other cap sealing area with any dimension greater than half the width of the sealing/welding area.

FIGURE 74 - CONTAMINATION ON THE FLANGE, RIM OR CAP SEALING AREA



NOTE TO FIGURE 74

1. REJECT: Contamination greater than half of the width of the sealing area. Para. 4.13(j) refers.

(k) Bubbles in the glass to metal seal with dimensions >0.8mm or any cluster of bubbles with a combined dimension greater than the adjacent pin.

(l) Bubbles, or an area of adjacent or interconnecting bubbles, in the seal area >1/8 (12.5%) of the seal area or which are more than half of the distance between the pin and body or pin and pin.

(m) Foreign material enclosed in the glass seal.

(n) Plating or die attach material overlapping the seals.

(o) Cracked or chipped glass seals. Meniscus chip-outs must not exceed 0.2mm in any dimension.