# SCANNING ELECTRON MICROSCOPE INSPECTION OF SEMICONDUCTOR DICE FOR DISCRETE SEMICONDUCTOR DEVICES

## ESCC Basic Specification No. 2145000


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| 838 | Specification upissued to incorporate editorial changes per DCR. |

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## 1 SCOPE

This specification, to be read in conjunction with ESCC Basic Specification No. 21400, Scanning Electron Microscope (SEM) Inspection of Semiconductor Dice, contains additional specific requirements for discrete semiconductor devices, which shall be applied to each wafer/dice inspected. (For SEM inspection of discrete microwave semiconductor devices refer to ESCC Basic Specification No. 2145010.)

## 2 GENERAL REQUIREMENTS

### 2.1 APPLICABILITY

The following criteria may not be varied or modified. Any ambiguity or proposed minor deviation shall be referred to the ESCC Executive for resolution and approval.

### 2.2 EQUIPMENT

The equipment specified in ESCC Basic Specification No. 21400 shall apply.

### 2.3 PROCEDURES

The procedures specified in ESCC Basic Specification No. 21400 shall apply.

### 2.4 DEFINITIONS

With reference to Figure 1 the following definitions apply.

#### 2.4.1 Void

(a) A void is any region in the metallisation, not caused by a scratch, where bare semiconductor material or oxide is visible within the design areas of the metallisation.
(b) In the case of glassivation, a void is the absence of glassivation over any active circuit area of the die.

#### 2.4.2 Notch

A notch is a hole in the edge of the metallisation.

#### 2.4.3 Crack

A crack is a fracture in the metallisation and may lie in any direction in the metallisation.

#### 2.4.4 Separation

Separation is where metallisation has lifted from the oxide or where two or more metallisation paths fail to meet as intended.

#### 2.4.5 Cavity

A localised area of reduced thickness in the deposited material.

#### 2.4.6 Tunnel

A tunnel is a cavity below the surface of the metallisation where contact between the oxide/oxide step is not established.

#### 2.4.7 Contact Window

A contact window is an opening in the dielectric usually covered by metallisation, where electrical contact is made with an underlying layer.

2.4.8 General Metallisation
Metallisation at all locations except oxide steps and including metallisation (stripes) in the contact window regions.

2.4.9 Multi-Layered-Metal Interconnection Systems
Two or more layers of metal or any other material used for interconnections.

2.4.10 Glassivation
The top layer(s) of transparent insulation material which cover(s) the active circuit area, including metallisation but excluding bond pads.

## 3 DETAILED REQUIREMENTS

3.1 ACCEPT/REJECT CRITERIA
A wafer/dice shall be rejected if it exhibits any of the defects listed in the relevant paragraphs of this section.

Where applicable, drawings have been included to provide additional explanatory material, but these shall be considered as examples only.

3.2 SINGLE-LAYER-METAL INTERCONNECTING SYSTEMS

3.2.1 Oxide Steps
The metallisation on all directional edges of every type of oxide step (i.e. contact window or other) shall be examined following the viewing requirements specified in ESCC Basic Specification No. 21400.

The metallisation shall be unacceptable if thinning and one or more defects such as voids, notches, cracks, separations, cavities or tunnels reduce the cross-sectional area of the metal at the directional edge to less than 50% of the metal cross-sectional area as deposited on the flat surface on either side of the directional edge.

For the metallisation to be acceptable, all directional edges shall be covered with metallisation which must be fully acceptable with the exception of the cases shown in the following two paragraphs.

3.2.2 Oxide Steps without Metallisation

In the event that a directional edge profile of a particular type of oxide step cannot be found which is covered with metallisation and, therefore, a judgement of the quality of the metallisation at that directional edge profile cannot be made, this shall not be cause for rejection if:

(a) It is established that the edge profile from which metal is absent does not occur in a current-carrying direction, such determination being made either by scanning all oxide steps of this type on the rest of the die, or by examination of a topographical map as supplied by the Manufacturer which shows the metal interconnection pattern; and
(b) Duplicate sample wafers/dice are examined whose locations are adjacent to the original sample wafers/dice in the holder whilst being rotated so as to orientate approximately 180˚ with respect to the original sample wafers/dice during metallisation.

If the conditions of both (a) and (b) are met, a Lot Acceptance basis may be used.

If only condition (a) is met, a single wafer/dice Acceptance basis must be used.

3.2.3 Oxide Steps with less than 50% Metallisation

If less than 50% of the metallisation is present at a particular directional edge profile (see Figure 1), but that defective edge profile is not an important current-carrying direction, rejection shall not take place if:

(a) It is established that the edge profile from which metal is absent does not occur in a current-carrying direction, such determination being made either by scanning all oxide steps of this type on the rest of the die, or by examination of a topographical map as supplied by the Manufacturer which shows the metal interconnection pattern and
(b) Acceptance is on a wafer/dice basis only.

3.2.4 General Metallisation

As per ESCC Basic Specification No. 21400.

In addition, any void which reduces the cross-sectional area of the metallisation stripe by more than 50% shall be cause of rejection.

3.3 MULTI-LAYERED-METAL INTERCONNECTION SYSTEMS

3.3.1 General

This type of system may be more susceptible to undercutting than single-layered-metal systems and shall be examined especially carefully for this type of defect in addition to the examination for other types of defect. Each layer of metal shall be examined.

The principal current-carrying layer shall be examined with the SEM while other layers (e.g. barrier layer or adhesion) may be examined using either the SEM or an Optical Microscope.

The glassivation, if any, and each successive layer of metal shall be stripped layer-by-layer using selective etching by suitable reagents so as to permit the individual examination of each layer.

If it is impracticable to remove the metals on a single die on a layer-by-layer basis, one or more dice immediately adjacent to the original die shall be etched so that all layers are exposed and may be examined.

3.3.2 Oxide Steps

The oxide step requirements for single-layer-metal systems herein shall apply to both the principal conducting metal and the barrier layer unless, by design, a barrier layer is not intended to cover the oxide steps. In this case the oxide step requirements shall not apply to the barrier layer.

3.3.3 General Metallisation

The general metallisation requirements for single-layer-metal systems herein shall apply to the principal conducting metal layer only.

Other metal layers (non-principal conducting layers such as barrier or adhesion layers) may be examined using either the SEM or an Optical Microscope.

*3.3.3.1 Interconnecting Stripes (excluding Contact Window Area)*

A defect consuming 100% of the cross-sectional area of a stripe shall be acceptable provided that the length of the defect is not greater than the width of the metallisation stripe.

*3.3.3.2 Contact Window Area*

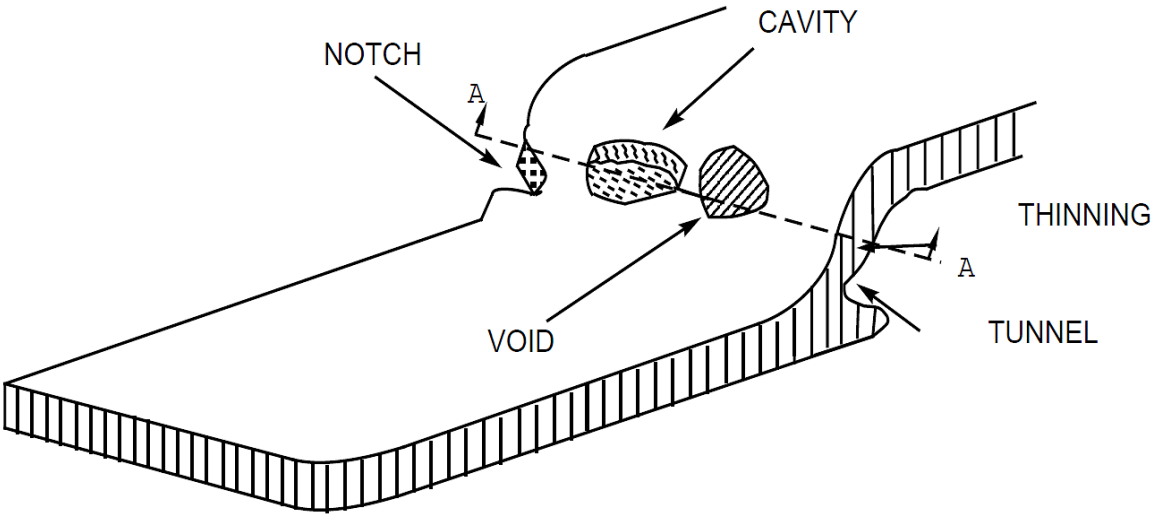
At least 70% of the contact window area and any underlying metal layer(s) must be covered by the principal metal layer. For the metal layer(s) above the principal conducting layer in the contact window area, a defect consuming 100% of the cross-sectional area of the metallisation stripe shall be acceptable provided that the length of the defect is not greater than the width of the metallisation stripe.

**NOTES:**

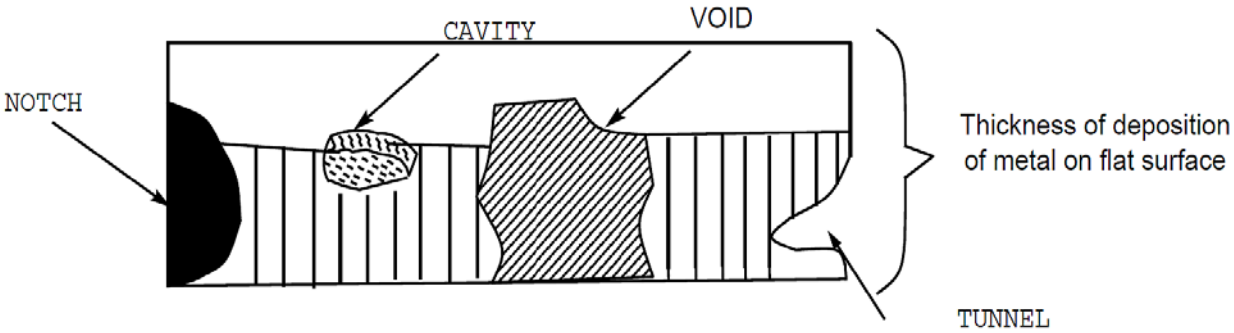
In the specific case of examination of contact window area metallisation for multi-metal systems, at least one of each type of contact window present shall be examined.

3.4 FIGURE 1 – METALLISATION AT OXIDE STEP

Metallisation at oxide step showing typical defects




Cross-section area (enlarged) of metallisation at oxide step

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