INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS, 128K X 8-BIT, ASYNCHRONOUS STATIC

RANDOM ACCESS MEMORY WITH THREE STATE OUTPUTS

BASED ON TYPE 65609E

ESCC Detail Specification No. 9301/053

Issue 2	April 2014

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
849	Specification upissued to incorporate editorial changes per DCR.

TABLE OF CONTENTS

1	GENERAL	5
1.1	SCOPE	5
1.2	APPLICABLE DOCUMENTS	5
1.3	TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS	5
1.4	THE ESCC COMPONENT AND COMPONENT TYPE VARIANTS	5
1.4.1	The ESCC Component Number	5
1.4.2	Component Type Variants	5
1.5	MAXIMUM RATINGS	6
1.6	HANDLING PRECAUTIONS	6
1.7	PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION	7
1.8	FUNCTIONAL DIAGRAM	8
1.9	PIN ASSIGNMENT	8
1.10	TRUTH TABLE AND TIMING DIAGRAMS	9
1.11	PROTECTION NETWORKS	13
2	REQUIREMENTS	13
2.1	GENERAL	13
2.1.1	Deviations from the Generic Specification	13
2.1.1.1	Deviations from Screening Tests - Chart F3	13
2.2	MARKING	14
2.3	ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES	14
2.3.1	Room Temperature Electrical Measurements	14
2.3.2	High and Low Temperatures Electrical Measurements	19
2.4	PARAMETER DRIFT VALUES	19
2.5	INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS	20
2.6	POWER BURN-IN CONDITIONS	20
2.7	OPERATING LIFE CONDITIONS	21
2.8	TOTAL DOSE RADIATION TESTING	21
2.8.1	Bias Conditions and Total Dose Level for Total Dose Radiation Testing	21
2.8.2	Electrical Measurements for Total Dose Radiation Testing	21

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930105301R

- Detail Specification Reference: 9301053
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	65609E	MFP-F32	G2	3	R [100kRAD(Si)]

The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 5	V	Note 1
Input Voltage Range	V_{IN}	-0.3 to V_{DD} +0.3	V	Notes 1, 2
Output Voltage Range	V_{OUT}	-0.3 to V_{DD} +0.3	V	Notes 1, 2
Input Current	I_{IN}	±10	mAdc	
Output Current into Input/Outputs (Low)	$I_{I/O}$	20	mAdc	Note 3
Device Power Dissipation (Continuous)	P_D	200	mW	
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Soldering Temperature	T_{sol}	+300	^oC	Note 4
Junction Temperature	T_j	+175	^oC	
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	14	$^oC/W$	

NOTES:

1. All voltages are with respect to V_{SS}. Device is functional from $3 \leq V_{DD} \leq 3.6V$
2. V_{DD} +0.3V shall not exceed 5V.
3. The maximum output current of any single I/O.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

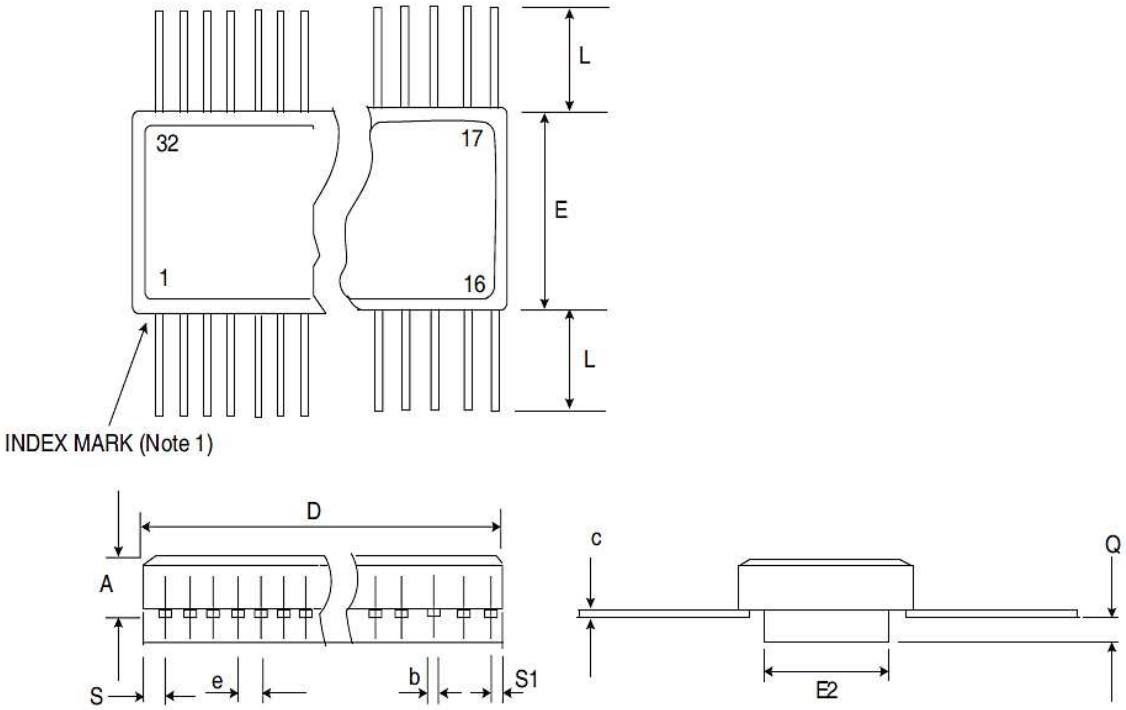
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 500 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Flat Leaded Multilayer Flat Package (MFP-F32) - 32 lead



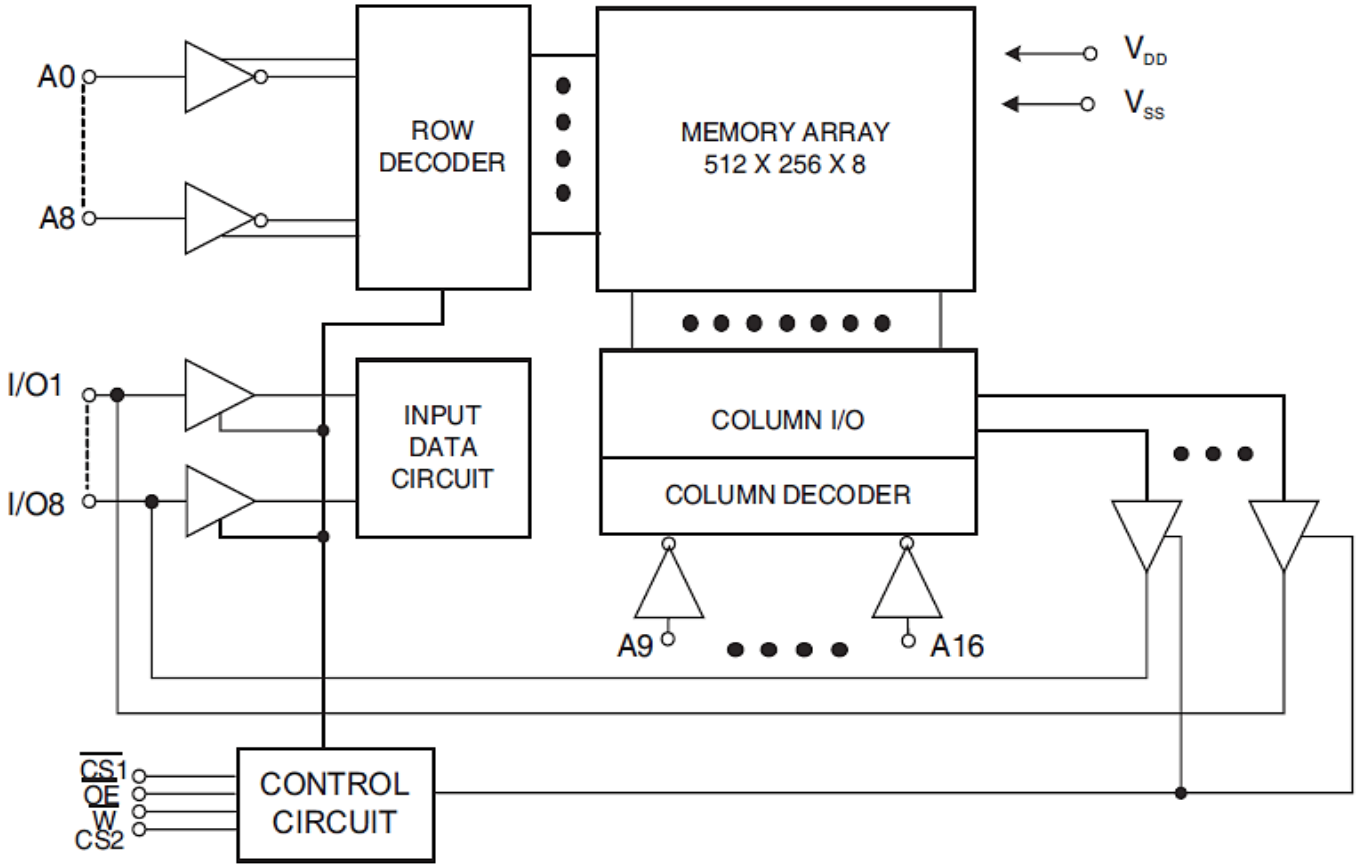
Symbols	Dimensions mm		Notes
	Min	Max	
A	1.78	2.72	
b	0.38	0.48	2
c	0.076	0.15	2
D	20.62	21.03	3
E	10.26	10.57	3
E2	6.96	7.26	
e	1.27 BSC		2, 4
L	7	8.5	4
Q	0.51	0.76	2, 5
S	-	1.14	6
S1	0	-	6

NOTES:

1. Index mark: a notch or terminal 1 identification mark shall be located adjacent to terminal 1.
2. All terminals.

3. This dimension allows for package edge anomalies caused by material protrusions such as rough ceramic, misaligned ceramic layers and lids, meniscus, and glass overrun.
   The corner shape (square, notch, radius etc.) may vary at the manufacturer option from that shown on the drawing.
4. 30 places. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. Dimension Q shall be measured at the point of exit of the lead from the body.
6. Two places.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Function
1	V_{DD}
2	A4 Input (Address)
3	I/O2 Input/Output (Data)
4	A7 Input (Address)
5	I/O1 Input/Output (Data)
6	A3 Input (Address)
7	A6 Input (Address)

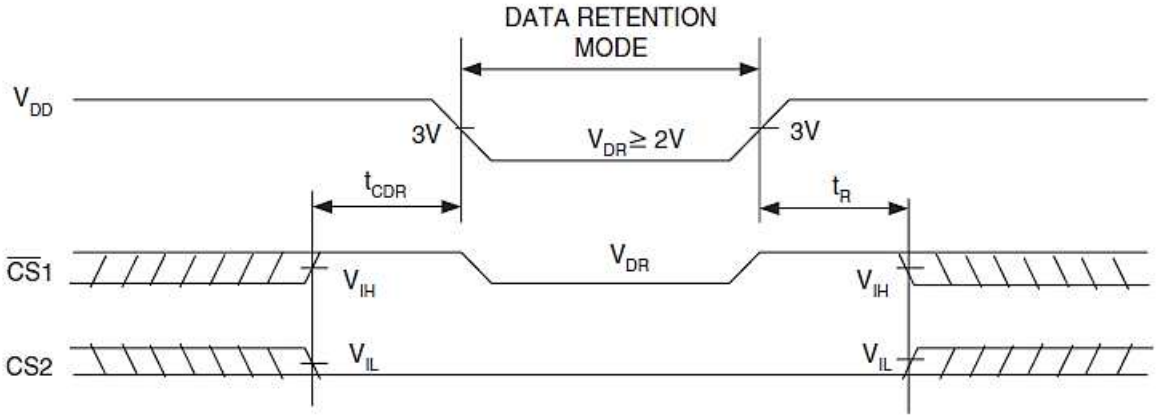
Pin	Function
8	A8 Input (Address)
9	A0 Input (Address)
10	A1 Input (Address)
11	CS2 Input (Chip Select)
12	I/O5 Input/Output (Data)
13	A2 Input (Address)
14	$\overline{W}$ Input (Write Enable)
15	I/O6 Input/Output (Data)
16	Not Connected
17	$\overline{CS1}$ Input (Chip Select)
18	V_{SS}
19	I/O7 Input/Output (Data)
20	$\overline{OE}$ Input (Output Enable)
21	A11 Input (Address)
22	I/O8 Input/Output (Data)
23	A10 Input (Address)
24	A9 Input (Address)
25	A14 Input (Address)
26	A13 Input (Address)
27	I/O4 Input/Output (Data)
28	A12 Input (Address)
29	A15 Input (Address)
30	I/O3 Input/Output (Data)
31	A16 Input (Address)
32	A5 Input (Address)

1.10 TRUTH TABLE AND TIMING DIAGRAMS

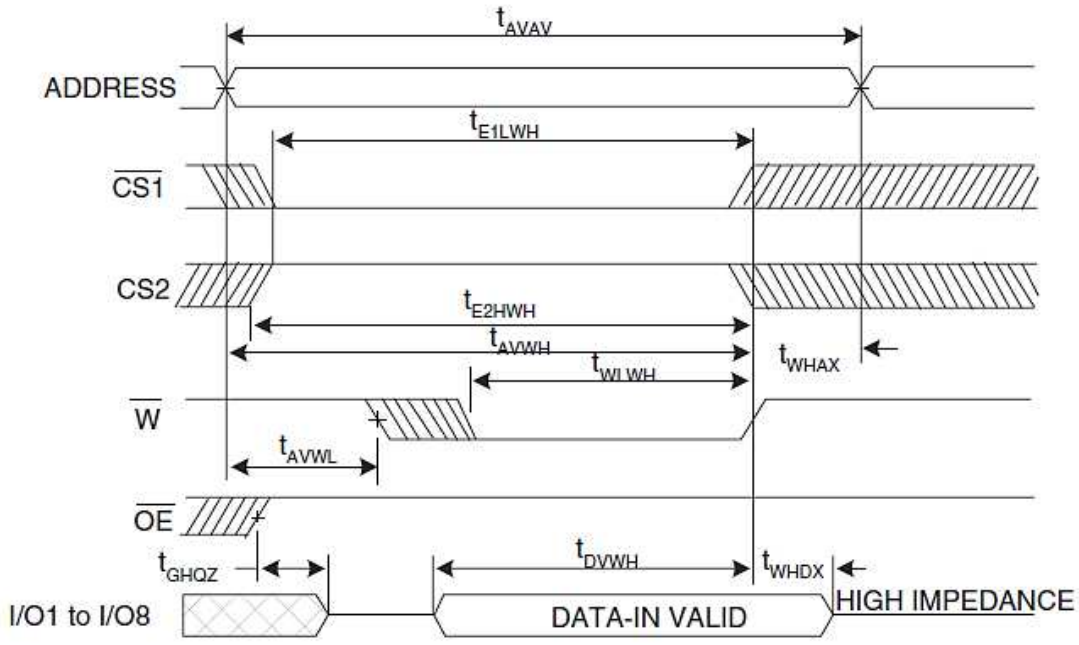
1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance

Inputs				Input/Outputs	Mode
$\overline{CS1}$	CS2	$\overline{W}$	$\overline{OE}$	I/On	
H	X	X	X	Z	Deselect/Power down
X	L	X	X	Z	Deselect/Power down
L	H	H	L	Data out	Read
L	H	L	X	Data in	Write
L	H	H	H	Z	Output disable

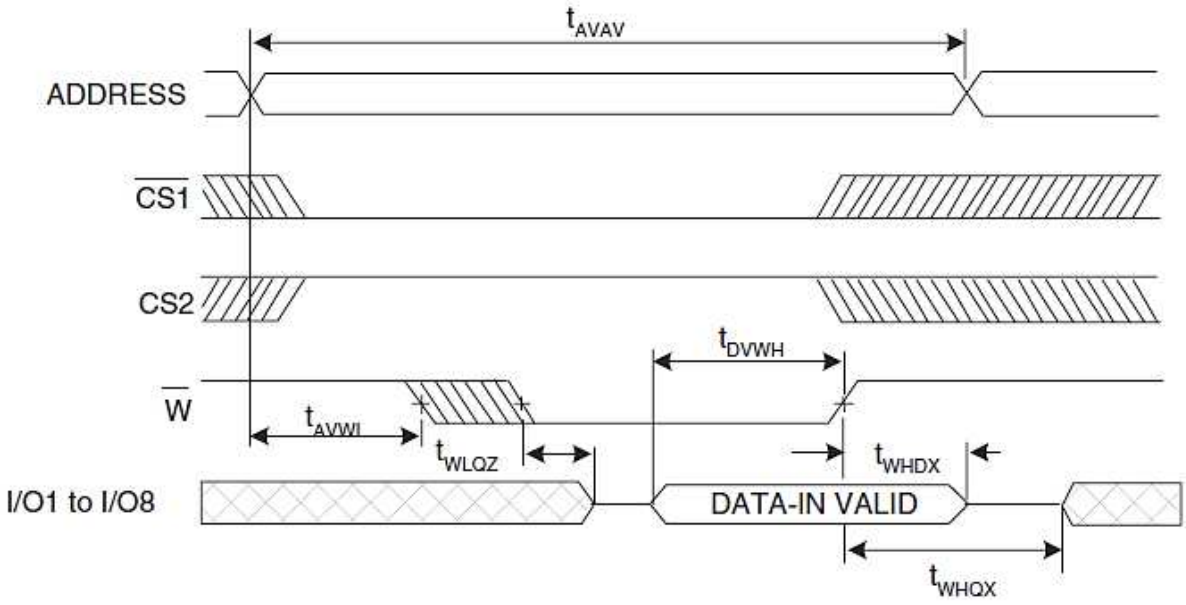
Data Retention



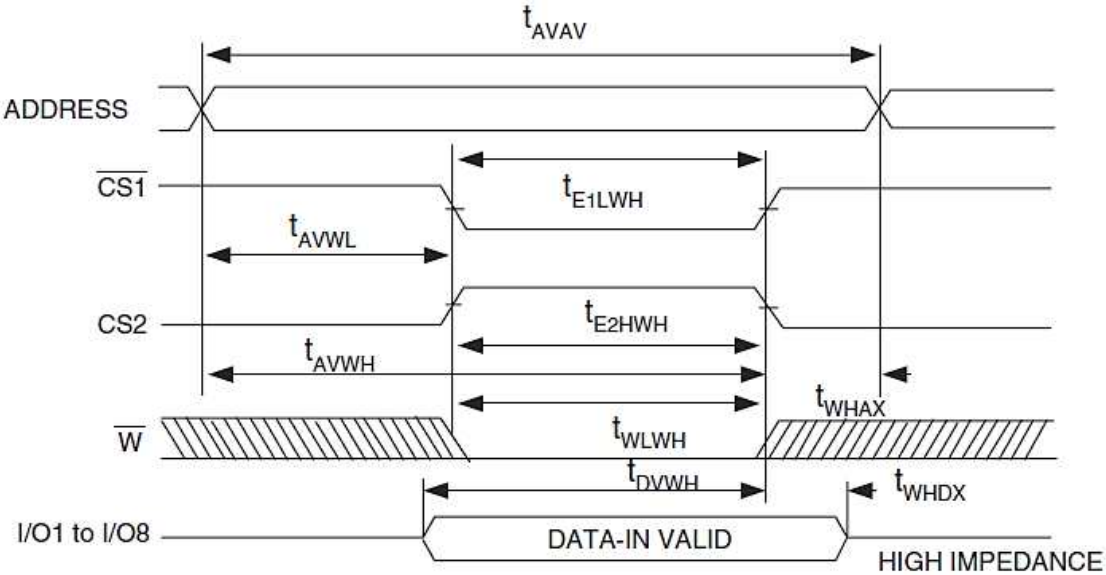
Write Cycle 1: $\overline{W}$ Controlled $\overline{OE}$ High during Write



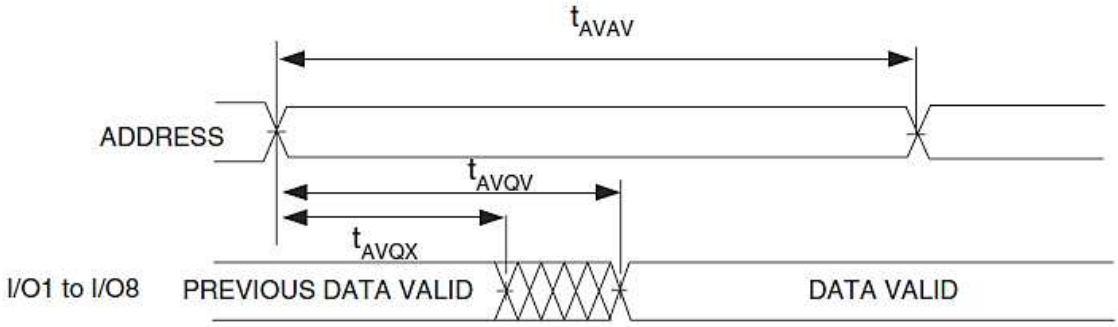
Write Cycle 2: $\overline{W}$ Controlled $\overline{OE}$ Low



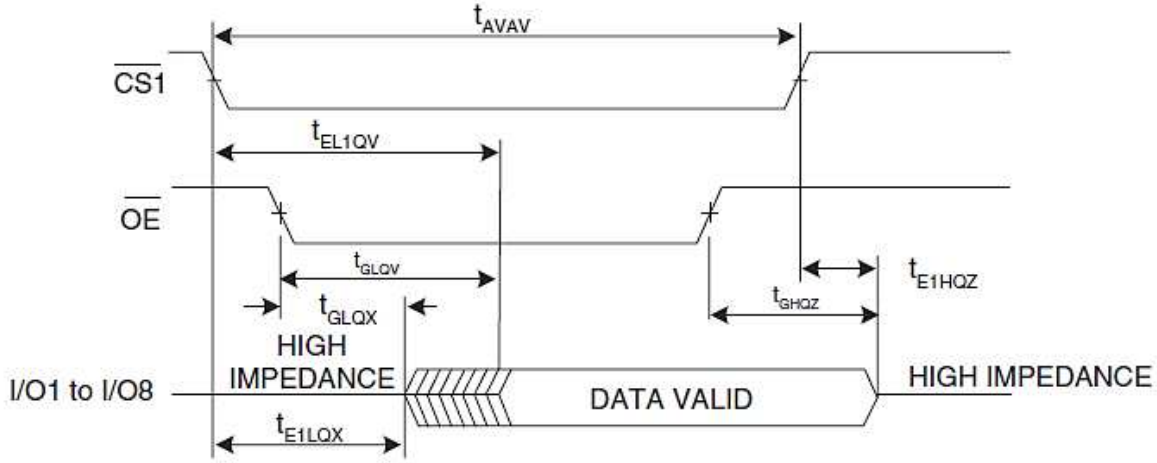
Write Cycle 3: $\overline{CS1}$ or CS2 Controlled



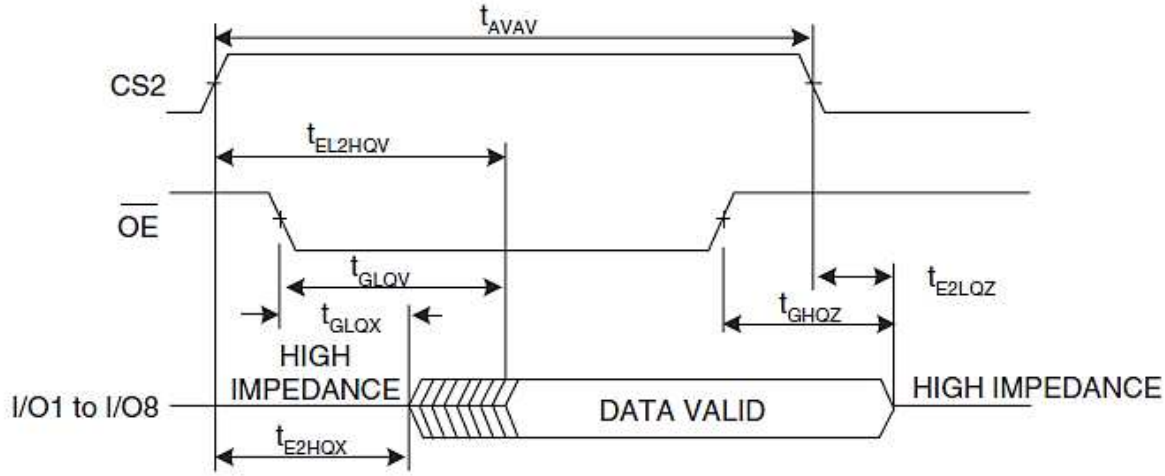
Read Cycle 1: Address Controlled $\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{W}$ = V_{IH}



Read Cycle 2: $\overline{CS1}$ Controlled $\overline{W}$ = CS2 = V_{IH}

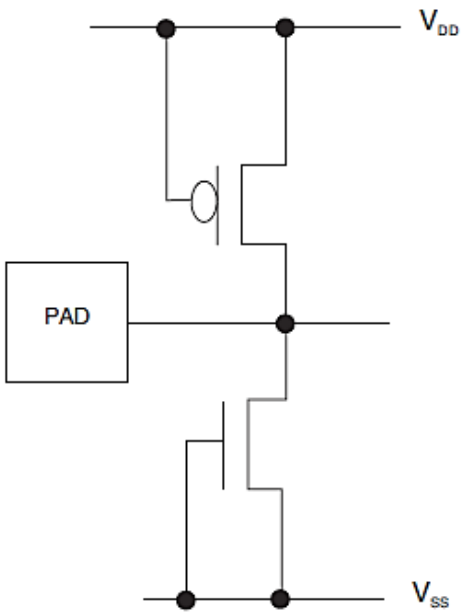


Read Cycle 3: CS2 Controlled $\overline{CS1}$ = V_{IL}, $\overline{W}$ = V_{IH}

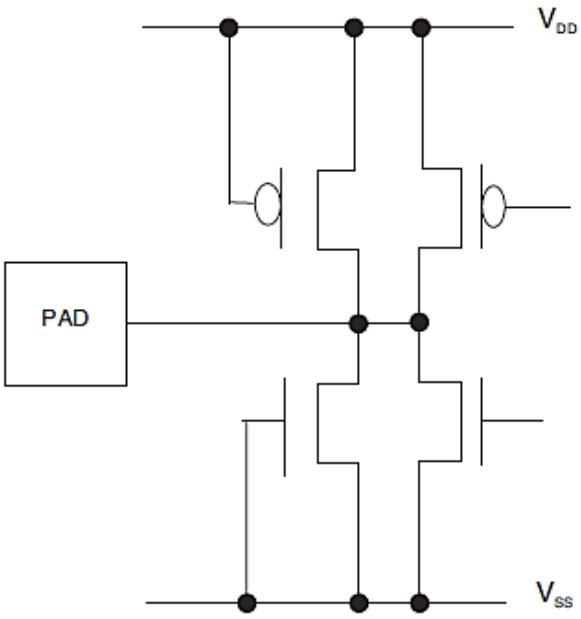


1.11 PROTECTION NETWORKS

Equivalent of each Input



Equivalent of each Output



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3 °C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 4	-	3014	Verify Truth Table Note 2	-	-	-
Input Clamp Voltage, to V_{SS}	V_{IC}	3008	I_{IN}(Under Test) = -100µA All Other Pins Open V_{DD} = Open, V_{SS} = 0V	-2	0.2	V
Low Level Input Current	I_{IL}	3009	V_{IN}(Under Test) = 0V V_{IN}(Remaining Inputs) = 3.6V V_{DD} = 3.6V, V_{SS} = 0V	-	-1	µA
High Level Input Current	I_{IH}	3010	V_{IN}(Under Test) = 3.6V, V_{IN}(Remaining Inputs) = 0V V_{DD} = 3.6V, V_{SS} = 0V	-	1	µA
Output Leakage Current, Third State, Low Level Applied 1	I_{OZL1}	3020	$V_{IN}(\overline{CS1})$ = 3.3V V_{IN}(CS2) = 0V V_{OUT} = 0V V_{DD} = 3.6V, V_{SS} = 0V	-	-1	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Leakage Current, Third State, Low Level Applied 2	I_{OZL2}	3020	$V_{IN}(\overline{CS1})$ = 0V V_{IN}(CS2) = 3.3V V_{OUT} = 0V V_{DD} = 3.6V, V_{SS} = 0V	-	-1	µA
Output Leakage Current, Third State, High Level Applied 1	I_{OZH1}	3020	$V_{IN}(\overline{CS1})$ = 3.3V V_{IN}(CS2) = 0V V_{OUT} = 0V V_{DD} = 3.6V, V_{SS} = 0V	-	1	µA
Output Leakage Current Third State, High Level Applied 2	I_{OZH2}	3020	$V_{IN}(\overline{CS1})$ = 0V V_{IN}(CS2) = 3.3V V_{OUT} = 0V V_{DD} = 3.6V, V_{SS} = 0V	-	1	µA
Low Level Output Voltage	V_{OL}	3007	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = 1mA V_{DD} = 3V, V_{SS} = 0V Note 3	-	0.4	V
High Level Output Voltage	V_{OH}	3006	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OH} = -0.5mA, V_{DD} = 3V, V_{SS} = 0V Note 4	2.4	-	V
Stand-by Supply Current 1	I_{DDSB1}	3005	$V_{IN}(\overline{CS1})$ = 2.2V V_{IN}(CS2) = 0.8V f = 0 Hz V_{DD} = 3.6V, V_{SS} = 0V Note 5	-	2.5	mA
Stand-by Supply Current 2	I_{DDSB2}	3005	$V_{IN}(\overline{CS1})$ = 3.3V V_{IN}(CS2) = 0.3 V f = 0 Hz V_{DD} = 3.6V, V_{SS} = 0V Note 5	-	1.5	mA
Operating Supply Current	I_{DDOP}	3005	V_{IN}(CS2, $\overline{W}$, $\overline{OE}$) = 3V V_{IN}(CS1) = 0V I_{OUT} = 0mA f = 25 MHz V_{DD} = 3.6V, V_{SS} = 0V	-	50	mA
Data Retention Current	I_{DDDR}	3005	$V_{IN}(\overline{CS1})$ = 1.8V V_{IN}(CS2) = 0.2V V_{DD} = 2V, V_{SS} = 0V Notes 5, 6	-	1	mA
Data Retention Test	-	-	Note 6	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Input Capacitance	C_{IN}	3012	$V_{IN} = V_{SS} = V_{DD} = 0V$ f = 1 MHz Note 10	-	8	pF
Output Capacitance	C_{OUT}	3012	$V_{IN} = V_{SS} = V_{DD} = 0V$ f = 1 MHz Note 10	-	8	pF
Read Cycle Time	t_{AVAV}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	40	-	ns
Address Access Time	t_{AVQV}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 8	-	40	ns
Address Valid to Low Z	t_{AVQX}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	3	-	ns
Write Cycle Time	t_{AVAW}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	35	-	ns
Address Set-up Time	t_{AVWL}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	0	-	ns
Address Valid to End of Write	t_{AVWH}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	28	-	ns
Data Set-up Time	t_{DVWH}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 8	28	-	ns
Chip Select 1 Low to Write End	t_{E1LWH}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	28	-	ns
Chip Select 2 High to Write End	t_{E2HWH}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	28	-	ns
Write Low to High Z	t_{WLQZ}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 9	-	15	ns
Write Pulse Width	t_{WLWH}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 8	28	-	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Address Hold from to End of Write	t_{WHAX}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	3	-	ns
Data Hold Time	t_{WHDX}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 8	0	-	ns
Write High to Low Z	t_{WHQX}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 9	0	-	ns
Chip Select 1 Access Time	t_{E1LQV}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 8	-	40	ns
Chip Select 1 Low to Low Z	t_{E1LQX}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 9	3	-	ns
Chip Select 1 High to High Z	t_{E1HQZ}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 9	-	15	ns
Chip Select 2 Access Time	t_{E2HQV}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 8	-	40	ns
Chip Select 2 High to Low Z	t_{E2HQX}	3003	V_{DD}=3 & 3.6V V_{SS}=0V Note 9	3	-	ns
Chip Select 2 Low to High Z	t_{E2LQZ}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 9	-	15	ns
Output Enable Access Time	t_{GLQV}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 7	-	12	ns
Output Enable Low to Low Z	t_{GLQX}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 9	0	-	ns
Output Enable High to High Z	t_{GHQZ}	3003	V_{DD} = 3 & 3.6V V_{SS} = 0V Note 9	-	10	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be V_{IN} = V_{SS} or V_{DD} and outputs not under test shall be open.
2. Functional go-no-go test with the following test sequences:

FUNCTIONAL TEST 1

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
March	100	3 & 3.6	0	0	3	0.5	-0.5	1.5
Checkerboard	100	3 & 3.6	0	0	3	0.5	-0.5	1.5
Imag	100	3 & 3.6	0	0	3	0.5	-0.5	1.5
Genbl	100	3	0	0	3	0.5	-0.5	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (mV)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
March	100	3.6	0	-300	3.9	0.5	-0.5	1.5
March	100	3	0	-300	3.3	0.5	-0.5	1.5
March	100	3.6	0	0	2.2	0.5	-0.5	1.5
March	100	3	0	800	0	0.5	-0.5	1.5

FUNCTIONAL TEST 3

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
March	100	3	0	0	3	1	-0.5	Note (b)

FUNCTIONAL TEST 4

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (c)
March	80	3 & 3.6	0	0	3	0.5	-0.5	1.5
Comarch	80	3 & 3.6	0	0	3	0.5	-0.5	1.5
Imag	80	3 & 3.6	0	0	3	0.5	-0.5	1.5
Checkerboard	80	3 & 3.6	0	0	3	0.5	-0.5	1.5

(a) A write cycle is followed by a read cycle. The time between start of write and start of read per the truth table is the specified timing parameter. $t_r = t_f \leq 5$ns.
(b) 0.4V for low output level, 2.4V for high output level.
(c) Output load 1 TTL gate equivalent $+C_L < 30$pF.

3. Address inputs shall be selected to produce a low level at the pin under test.

4. Address inputs shall be selected to produce a high level at the pin under test.
5. Measurements are performed with the memory loaded with a background of zeros, then with a background of ones, for all inputs High, then Low. Only the worst case is recorded.
6. Data retention procedure:
   (a) Write memory at V_{DD} = 3V with CHECKERBOARD pattern with V_{IL} = 0V and V_{IH} = 3V.
   (b) Power down to V_{DD} = 2V for 250ms, $V_{IN}(\overline{CS1})$ = 1.8V.
   (c) Restore V_{DD} to 3V, wait t_R(operation recovery time), read memory and compare with original pattern.
   (d) Repeat the procedure with $\overline{\text{CHECKERBOARD}}$ pattern.
   (e) t_R = 40ns.
   (f) During power up and power down transitions, $V_{IN}(\overline{CS1}) \geq V_{DD}$-0.2V, V_{IN}(Remaining Inputs) ≤ 0.2V or ≥ V_{DD}-0.2V.
7. Parameter tested go-no-go during Functional Test 4.
8. Parameter measured during Functional Test 4 using pattern March at 3V and 3.6V.
9. Guaranteed with output loading 5pF but not tested.
10. Guaranteed but not tested.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5) °C and T_{amb} = -55 (+5 -0) °C. The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 °C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}	±0.1	-	1	µA
Output Leakage Current, Third State, Low Level Applied 1	I_{OZL1}	±0.1	-	-1	µA
Output Leakage Current, Third State, Low Level Applied 2	I_{OZL2}	±0.1	-	-1	µA
Output Leakage Current, Third State, High Level Applied 1	I_{OZH1}	±0.1	-	1	µA
Output Leakage Current, Third State, High Level Applied 2	I_{OZH2}	±0.1	-	1	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V
Stand-by Supply Current 1	I_{DDSB1}	±0.25	-	2.5	mA
Stand-by Supply Current 2	I_{DDSB2}	±0.15	-	1.5	mA
Data Retention Current	I_{DDDR}	±0.1	-	1	mA

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 ^{o}C.

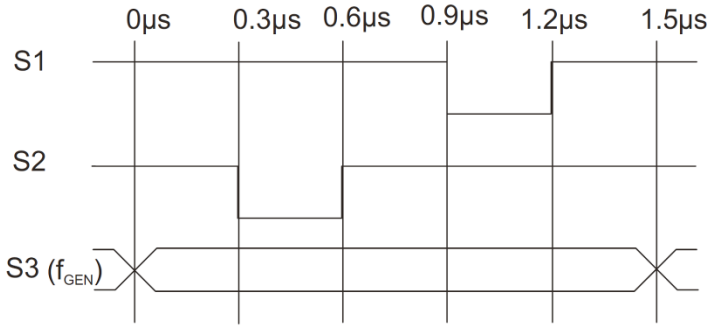
The characteristics, test methods, conditions and limits shall be as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Inputs A0 to A16	V_{IN}	S3 to S19 (Note 1)	V
Input $\overline{CS1}$	V_{IN}	V_{SS}	V
Input CS2	V_{IN}	V_{DD}	V
Inputs $\overline{W}$	V_{IN}	V_{GEN}(S1) (Note 2)	V
Input $\overline{OE}$	V_{IN}	V_{GEN}(S2) (Note 2)	V
Inputs/Outputs I/O2, I/O4, I/O6, I/O8	V_{IN}	V_{GEN}(S20) (Note 1)	V
Inputs/Outputs I/O1, I/O3, I/O5, I/O7	V_{IN}	V_{GEN}(S21) (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency	f_{GENS3}	330 ±20% (Note 1)	kHz
Positive Supply Voltage	V_{DD}	3.7 (±0.1)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1.
$$f_{GEN(Sn)} = \frac{1}{2} . f_{GEN(Sn-1)}, \text{for } n > 3$$

2. Input waveforms to indicate required timing and phase relationship:



3. Input Protection Resistor = Output Load = 1 kΩ.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during radiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Inputs An, CS2, $\overline{W}$, $\overline{OE}$	V_{IN}	V_{DD}	V
Input/Outputs I/On	V_{IN}	Open	V
Input $\overline{CS1}$	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	3.6 ±0.1	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input protection resistor = 1kΩ.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of radiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at T_{amb} = 22 ±3 °C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.