CHARGE COUPLED DEVICES, SILICON, PHOTOSENSITIVE, ADVANCED INVERTED MODE SENSOR, BACK ILLUMINATED, 740 X 514 IMAGE AREA, FRAME TRANSFER

BASED ON TYPE CCD55-20

ESCC Detail Specification No. 9610/004

Issue 2	April 2014

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
849	Specification upissued to incorporate editorial changes per DCR.

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical, electro-optical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9020.
(b) ESCC 25000, Electro-optical Test Methods for Charge Coupled Devices.
(c) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 961000401D

- Detail Specification Reference: 9610004
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: D (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Reference Temperature T_{ref} (°C)	Case	Weight Max (g)	Total Dose Radiation Level Letter	Number of Thermistors per Device
01	CCD55-20-*-B18	+5	PGA	35	D [10kRAD(Si)]	2
02	CCD55-20-*-C61	+5	PGA	35	D [10kRAD(Si)]	0

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Input Voltage	V_{IN}	-20 to +20	V	Notes 1, 3
		-0.3 to +25		Notes 2, 3
Input Voltage, Pin OD	V_{IN}	-0.3 to +35	V	Notes 3, 4
Output Voltage, Pin OS	V_{OUT}	-0.3 to +25	V	Notes 3, 4
Thermistor Maximum Voltage Difference	-	Note 5	-	Not applicable to Variant 02
Operating Temperature Range	T_{op}	-55 to +50	^{o}C	Note 6
Storage Temperature Range	T_{stg}	-55 to +125	^{o}C	
Rate of Change of Temperature	-	5	^{o}C/min	Note 7

NOTES:

1. For input pins ΦR, IΦn, RΦn, SΦn, IG, DG, OG.
2. For input pins RD, DD.
3. With respect to V_{SS}.
4. Maximum voltage applied between OD and OS shall not exceed ±15V.
5. Maximum voltage difference across T1+ and T1- and T2+ and T2- shall be such that the thermistor temperature does not exceed 150^{o}C (given that 1mW raises T by 1^{o}C).
6. Device is functional for $-55 \leq T_{op} \leq +125$ ^{o}C but with degraded performance. Parameters are not guaranteed in this temperature range.
7. Rate of change of temperature is applicable over the operating and storage (non-operating) temperature ranges.

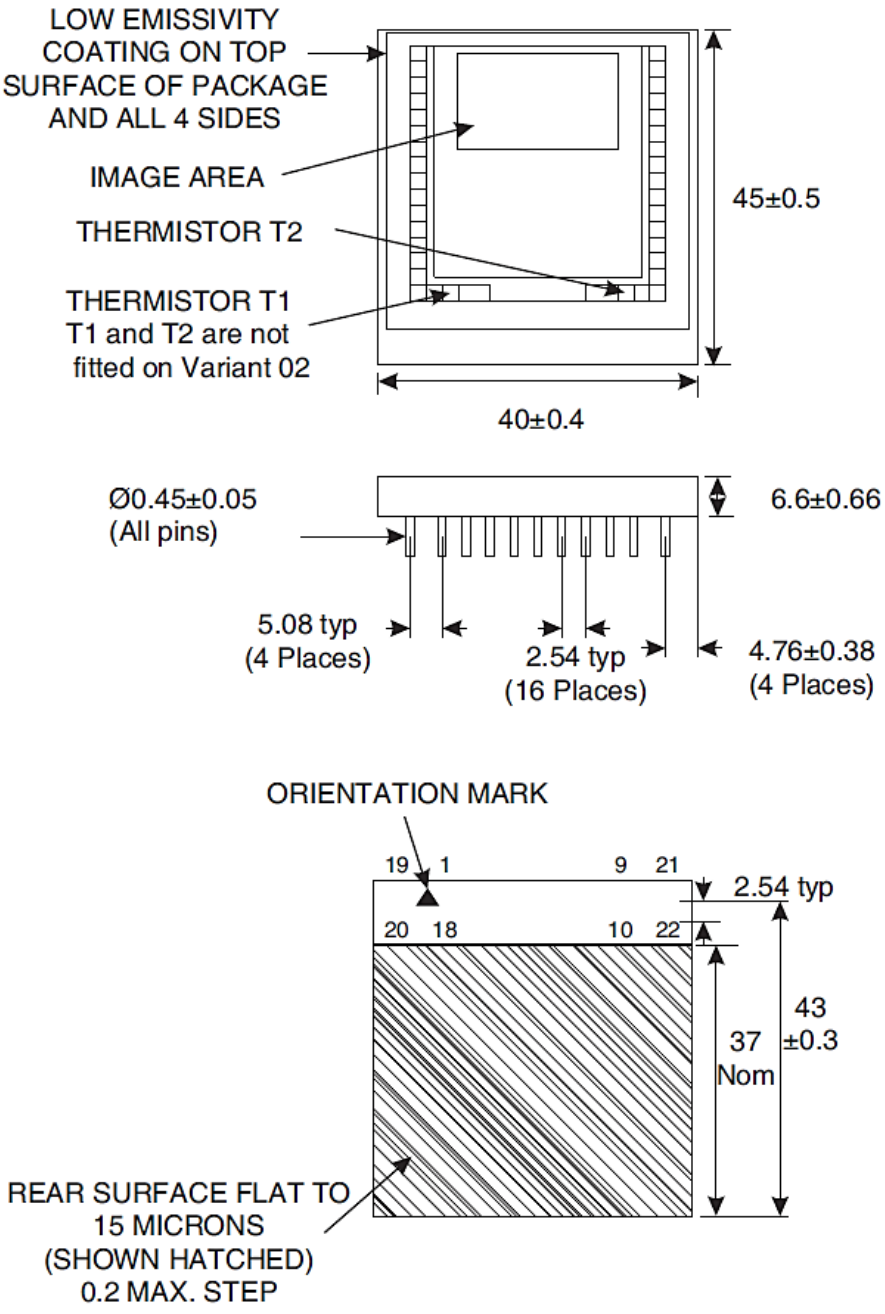
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

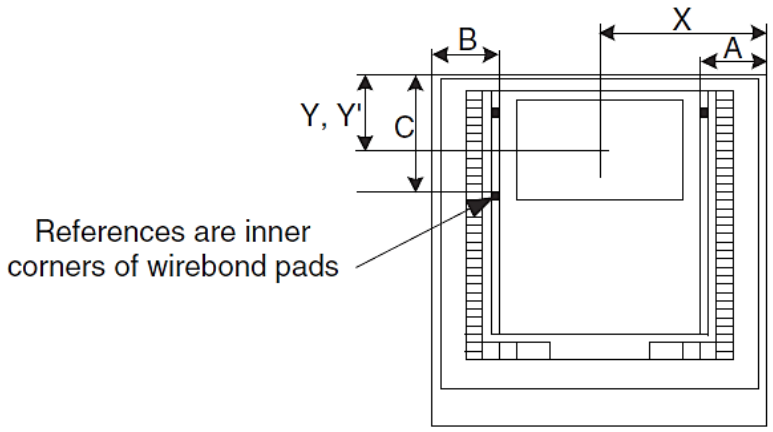
1.7.1 Pin Grid Array (PGA) - 22 Pin



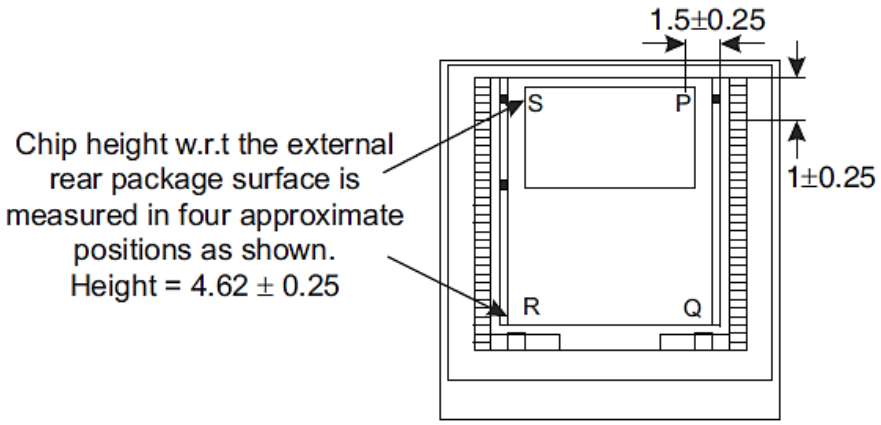
NOTES:

1. All dimensions in mm.
2. Pin numbers shown for identification purposes only.

1.7.2 Geometrical References

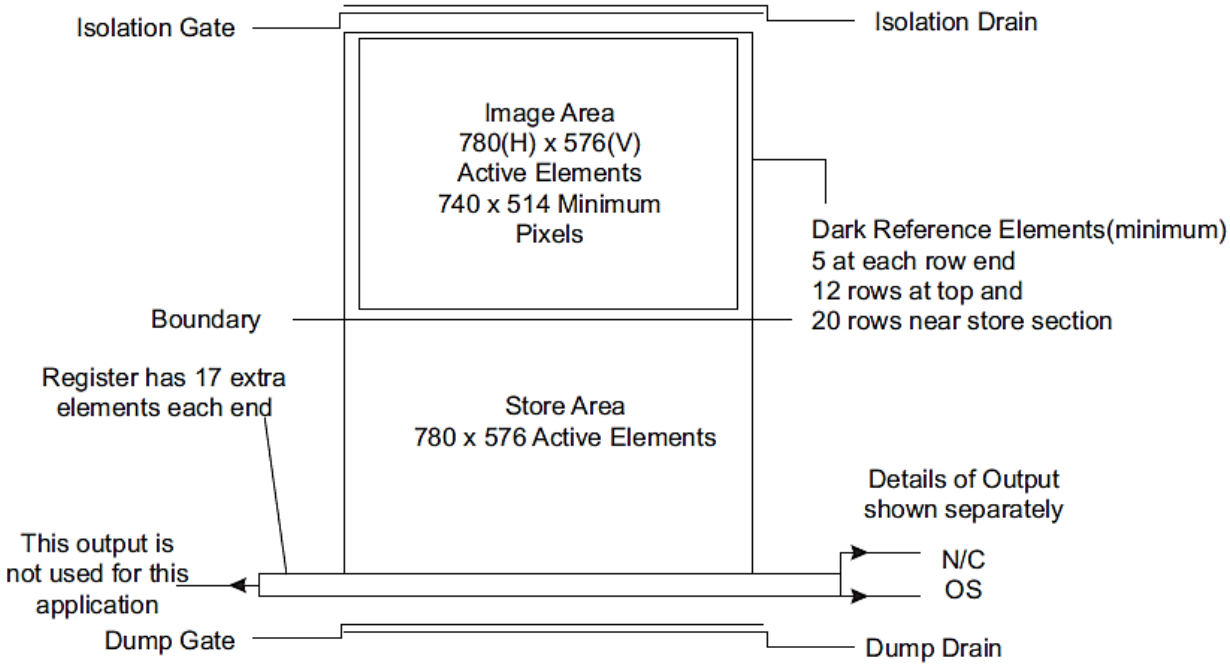


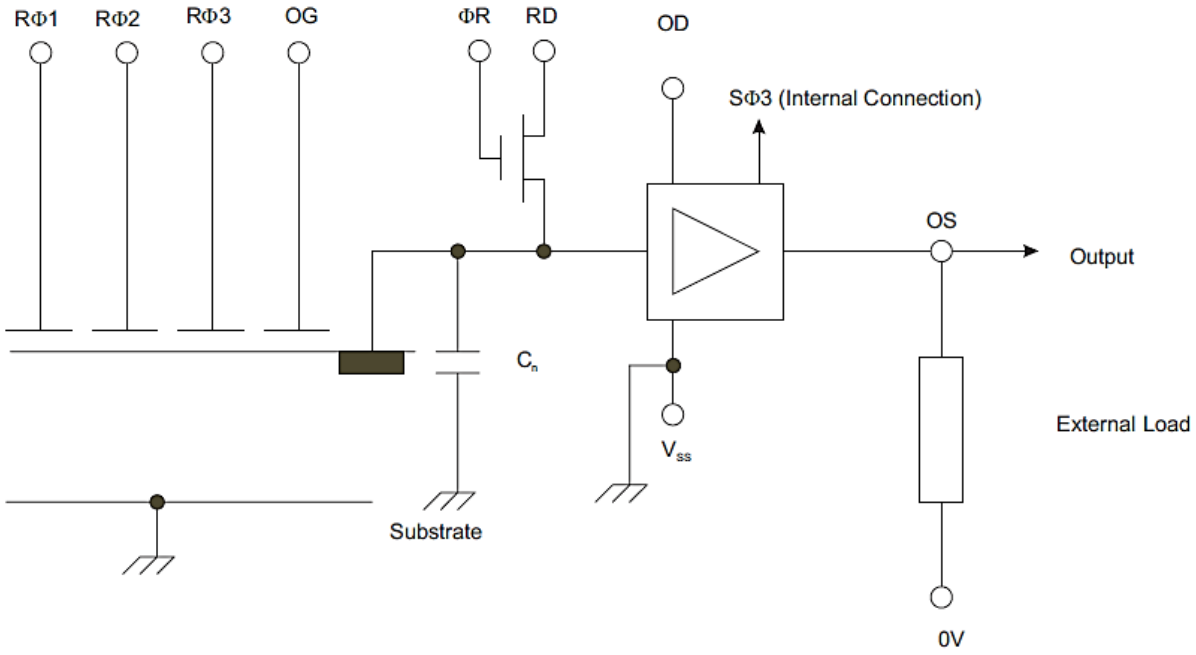
X and Y define the centre of the 576 x 780 array of active elements.
X and Y' define the centre of the minimum imaging 514 x 740 pixels.
A, B and C are measured from the optical references.
X = A + 10.10, X = 20 ± 0.45
Y = C - 6.39, Y = 9.72 ± 0.25, Y' = Y - 0.09



NOTES:
1. All dimensions in mm.

1.8 FUNCTIONAL DIAGRAM



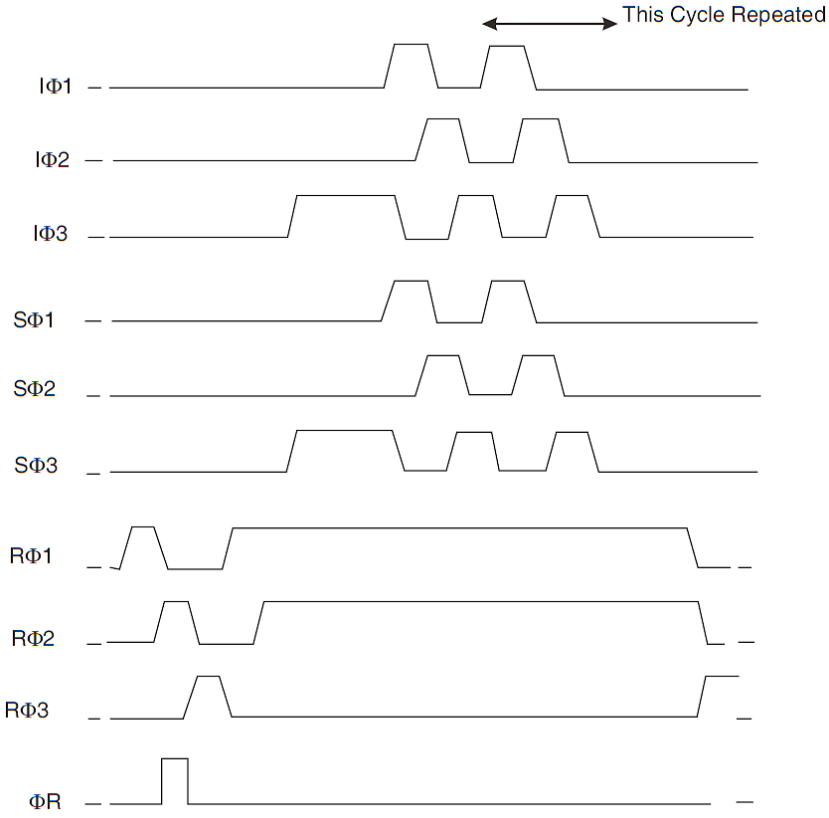


1.9 PIN ASSIGNMENT

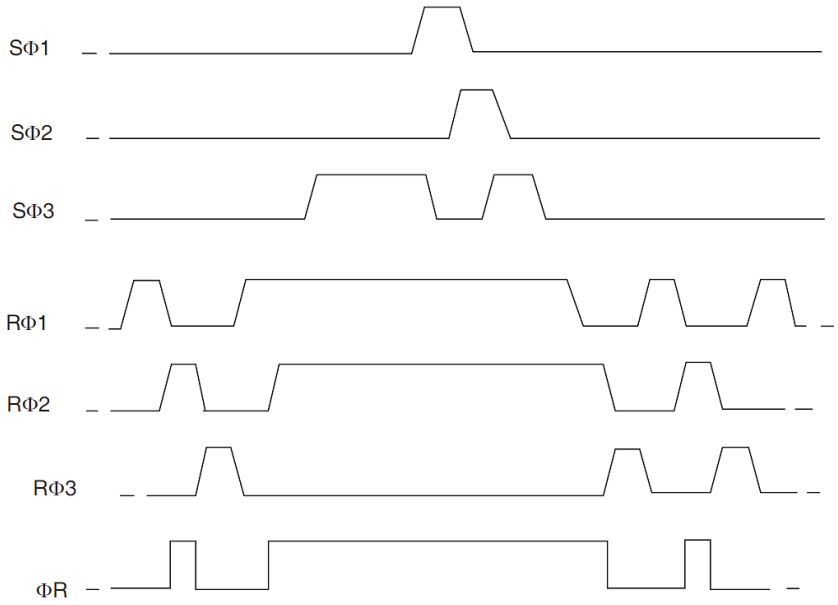
Pin	Function
1	RΦ3 Input (Readout Register Clock)
2	RΦ2 Input (Readout Register Clock)
3	SΦ3 Input (Storage Section Clock)
4	SΦ2 Input (Storage Section Clock)
5	SΦ1 Input (Storage Section Clock)
6	DG Input (Dump Gate)
7	IG Input (Isolation Gate)
8	OD Input (Output Transistor Drain)
9	OG input (Output Gate)
10	RD Input (Reset Transistor Drain)
11	OS Output (Output Transistor Source)
12	DD Input (Dump Drain)
13	V_{SS} (Substrate Bias)
14	IΦ1 Input (Image Section Clock)
15	IΦ2 Input (Image Section Clock)
16	IΦ3 Input (Image Section Clock)
17	ΦR Input (Output Reset Pulse)
18	RΦ1 Input (Readout Register Clock)
19	Variant 01 = T1 + Output (Thermistor) ; Variant 02 = No Connection
20	Variant 01 = T1 - Output (Thermistor) ; Variant 02 = No Connection
21	Variant 01 = T2 + Output (Thermistor) ; Variant 02 = No Connection
22	Variant 01 = T2 - Output (Thermistor) ; Variant 02 = No Connection

1.10 TIMING DIAGRAMS

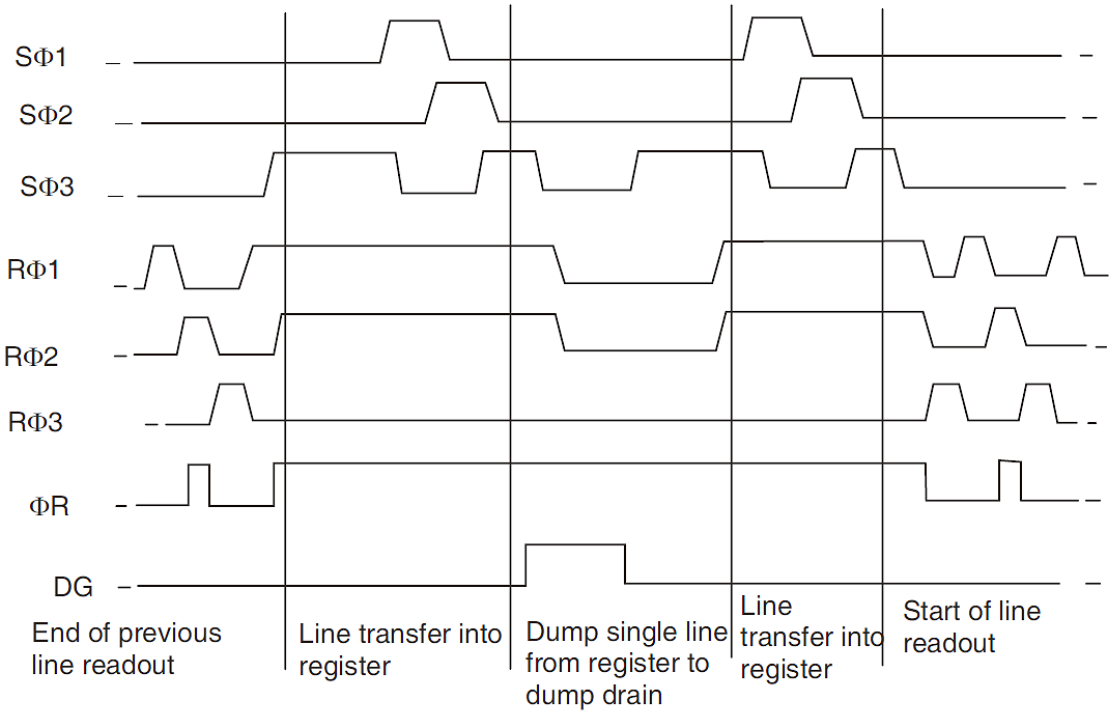
Detail of Frame Transfer – Image to Store



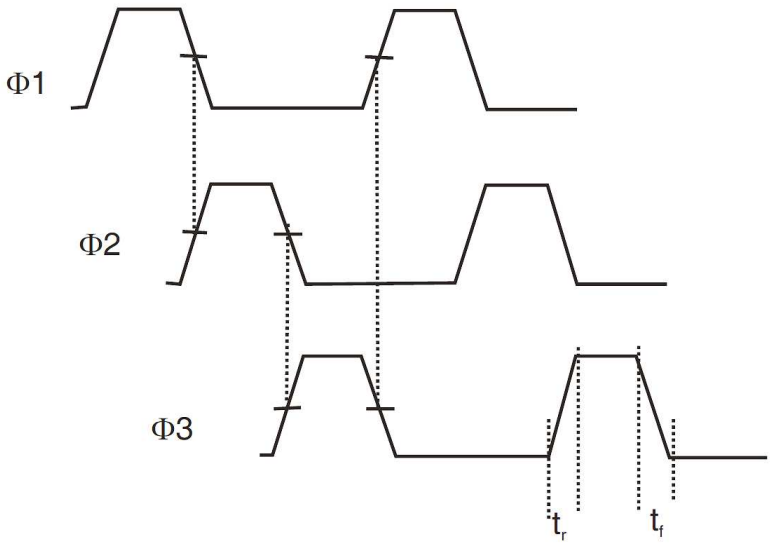
Detail of Line Transfer – Store to Readout register



Detail of Vertical Line Transfer – Single line dump



Drive Pulse Waveform

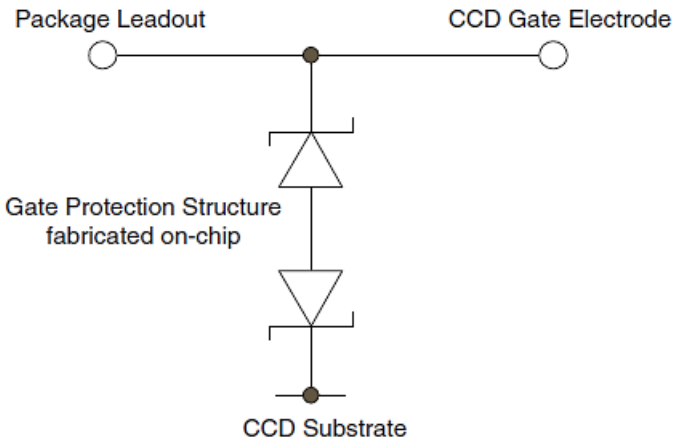


NOTES:

1. Pulses should be symmetrical and overlap at 50% points, as shown.
2. Rise and fall times (t_r, t_f), 10 to 90%, are defined in Note 2 of Notes to Electrical Measurement Tables herein.

1.11 INPUT PROTECTION NETWORK

Inputs DG, IG, OG, ΦR, IΦn, RΦn and SΦn are protected as shown:



1.12 MATERIALS AND FINISHES

(a) CCD Package
The CCD package shall be of multilayered co-fired aluminium oxide and aluminium nitride construction. The external top and side surfaces shall be gold plated over nickel and tungsten.

(b) Input Window/Lid Seal
None

(c) Terminal Material and Finish
The terminal material shall be Type D in accordance with ESCC Basic Specification No. 23500. The terminal finish shall be gold, thickness 1.524µm min over nickel, thickness 1.27µm min, 8.89µm max.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Production Control

(a) Rebonding of wire bonds is permitted as defined:
No more than three rebonds are permitted anywhere on any one device. No bondlink may be reworked more than once; i.e. there may be no more than two bond feet, or attempted bond feet, on any bond pad, whether chip or package. No more than two adjacent bond pads, on chip or package, may be subjected to rebonding.

2.1.1.2 Deviations from Special In-Process Controls - Chart F2

(a) Die Shear/Substrate Attach Strength testing is not performed.

2.1.1.3 Deviations from Qualification and Periodic Tests - Chart F4

(a) Permanence of Marking shall not be performed.
(b) Operating Life. For Periodic Tests, the duration shall be 1000 hours, with electrical measurements performed in accordance with Intermediate and End-Point Electrical Measurements herein at 0 and 1000 ±48 hours.

2.1.1.4 Deviations from Data Documentation Report

(a) Special In-Process Controls data shall be held by the manufacturer and not delivered.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT REFERENCE, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at reference, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Reference Temperature Electrical Measurements

Unless otherwise specified the measurements shall be performed at T_{ref} ±3 ^{o}C.

Characteristics	Symbols	ESCC 25000 Test Method Para.	Test Conditions	Limits		Units
				Min	Max	
Leakage Current on Input Gates	I_L	5.1	V_{IN}(Input Gates) = 20V V_{IN}(Remaining Inputs) = 0V V_{OUT} = 0V V_{SS} = 0V T_{amb} = +21 ±3 ^{o}C	-	10	nA
Power Supply Current 1	I_{OD}	5.3	Notes 1, 2	-	10	mA
Power Supply Current 2	I_{RD}	5.3	Notes 1, 2	-	100	nA
DC Output Voltage Level	V_{REF}	5.4	V_{IN}(ΦR) = 12V, V_{IN} (Remaining Inputs) = 0V	Note 3		V
Reset Pulse Feedthrough	V_{RESET}	5.5	Notes 1, 2	-	100	mV

Characteristics	Symbols	ESCC 25000 Test Method Para.	Test Conditions	Limits		Units
				Min	Max	
Offset Voltage	V_{OFFSET}	6.5	Notes, 1, 2	-	25	mV
Thermistor Resistance (Variant 01 only)	R_T	-	-	Note 4		kΩ
Charge to Voltage Conversion Factor	CVF	6.18	Notes 1, 2	0.8	1.2	µV/e
Full Well Capacity (Image Section)	V_{SAT-IM}	6.7(a): Global Method	Uniform illumination Notes 1, 2	300	-	ke
Full Well Capacity (Readout Register)	V_{SAT-RE}	6.8	Number of binned lines = 8, Uniform illumination Notes 1, 2	1200	-	ke
Linearity Error (to 240ke/p)	LE	6.6	Uniform illumination Notes 1, 2	-	1	%
Average Dark Signal	DS_{AV}	6.20	Notes 1, 2	-	125	e/pixel/s
Dark Signal Non-uniformity	DSNU	6.21	Notes 1, 2	-	50	e/pixel/s
Quantum Efficiency	QE	6.19	Uniform illumination Notes 1, 2, 5 Wavelength = 350nm 400nm 500nm 650nm 900nm	 50 80 80 75 30	 - - - - -	%
Photo Response Non-uniformity	PRNU	6.14	Uniform illumination Notes 1, 2 Wavelength = 400nm (~10nm bandwidth) 550nm (~80nm bandwidth)	 - -	 5 3	%
Total Charge Transfer Inefficiency - Vertical	VCTI	6.12	No illumination Notes 1, 2, 6	-	1.5	%
Store Shield Position	-	-	Uniform illumination Notes 1, 2, 7	-	-	-

Characteristics	Symbols	ESCC 25000 Test Method Para.	Test Conditions	Limits		Units
				Min	Max	
Photo Response Defects Pixels Columns	-	-	Notes 1, 2, 8 (Identified from the data frame of the measurement of PRNU)	 - -	 20 0	-
Defects in Darkness Pixels Columns	-	-	Notes 1, 2, 9	 - -	 60 0	-
Output Impedance	Z_{OUT}	-	Notes 1, 2, 10	-	-	-

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at temperatures defined below.

Characteristics	Symbols	ESCC 25000 Test Method Para.	Test Conditions Note 11	Limits		Units
				Min	Max	
Charge to Voltage Conversion Factor	CVF	6.18	Notes 1, 2 T_{amb} = +50 (+0 -5) °C T_{amb} = -27 (+5 -0) °C	 0.7 0.9	 1.1 1.3	µV/e
Power Supply Current 1	I_{OD}	5.3	Notes 1, 2 T_{amb} = +50 (+0 -5) °C T_{amb} = -27 (+5 -0) °C	 - -	 10 10	mA
Thermistor Resistance (Variant 01 only)	R_T	-	T_{amb} = +50 (+0 -5) °C T_{amb} = -27 (+5 -0) °C	Note 4		kΩ

2.3.3 Notes to Electrical Measurement Tables

1. The CCD shall be biased as follows during electro-optical tests:

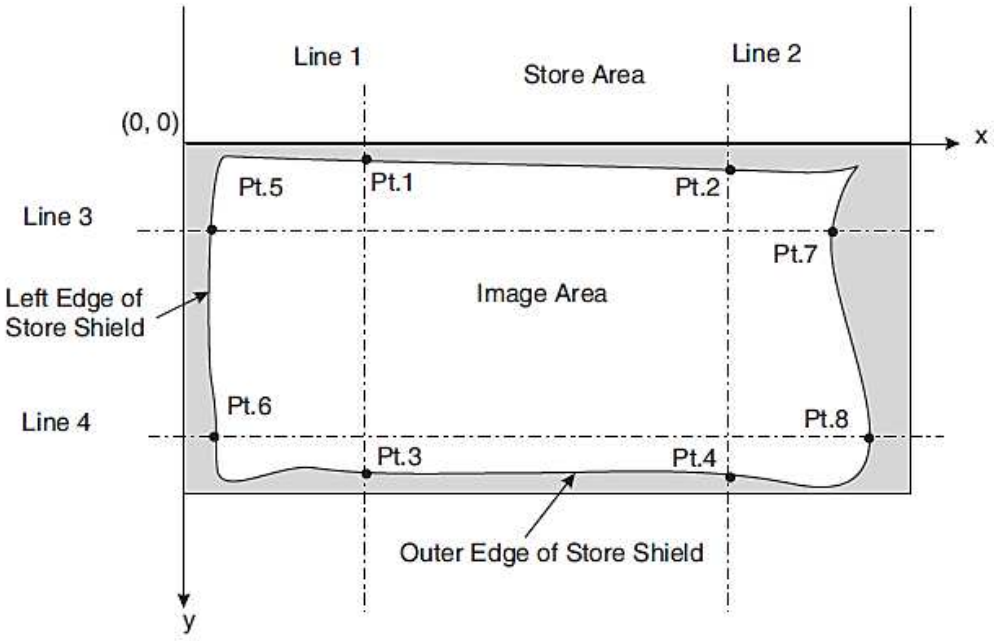
Parameter	Symbol	Conditions	Unit
Output Amplifier Drain	V_{OD}	32 (+1 -5)	V
Reset Drain Bias	V_{RD}	19 ±2	V
Substrate Bias	V_{SS}	9 (+2 -1)	V
Output Gate Bias	V_{OG}	3 ±2	V
Diode Drain	V_{DD}	25 to V_{OD}	V
Unused Register (as set on test camera)	V_{IG}	10 (+0 -10)	V

2. All Clock low levels taken as 0 ±0.5V, except Readout Clock low = 1 ±0.5V. Readout frequency ~1 MHz, External Load Resistance on test camera ~4kΩ.

Clock Description	Parameter	Conditions	Unit
Image Clocks IΦn	High Level	15 (+0 -3)	V
	Pulse Width	≥ 2	µs
	Initial Pulse Width after Static Clocks	10 (+90 -5)	
	Rise/Fall Times	0.2 (+0.3 -0.1)	
	Overlap	≥ 90	%
Store Clocks SΦn	High Level	15 (+0 -3)	V
	Pulse Width	≥ 2	µs
	Initial Pulse Width after Static Clocks	10 (+90 -5)	
	Rise/Fall Times	0.2 (+0.3 -0.1)	
	Overlap	≥ 90	%
Readout Clocks RΦn	High Level	13 (+2 -3)	V
	Rise/Fall Times	45 (+5 -35)	ns
	Overlap	100	%
Reset Pulse RD	High Level	12 (+3 -2)	V
	Pulse Width	≥ 100	ns
	Rise/Fall Times	35 (+15 -25)	
Dump Gate DG	High Level	14 (+1 -4)	V
	Rise/Fall Times	≥ 50	ns

3. DC level is typically 4 to 6 Volts below V_{OD}.
4. Thermistor resistance is measured for information only.
5. The pixel area is defined as rows 250 to 299 inclusive with a width of 740 pixels (the minimum guaranteed pixel area). The average signal shall be approximately 50% of the measured full well capacity.
6. The average signal shall be approximately 80% of the measured full well capacity. The clock sequence is modified to give frame transfer operations with the following features:
   (i) a frame transfer at normal rate but including an additional 10 line transfer cycles (overscan times). The dump gate is held high during the frame transfer operation but is taken low before the line readout commences.
   (ii) The normal line by line readout of the store section signal (576 rows) with digitisation and frame stored as normal.

7. Refer to the Functional Diagram herein. The Store Shield Position is calculated using eight points at specific places on the image area, as shown below. Each point is the location of a pixel with at least 50% of the unshielded signal level and having two immediately adjacent pixels of this value or greater.



Lines 1, 2, 3 and 4 are at 1/4 and 3/4 across the image area in each direction. Points 1, 2, 3,..., 8, with coordinates (x1, y1), (x2, y2), etc., are the locations of the 50% threshold pixels (see above). The coordinates of these points are used to calculate, in pixels, the average Left, Right, Outer and Store Edge positions and Shield Rotation as follows:

- Average Store Edge Position = (y1 + y2) / 2
- Average Outer Edge Position = 575 - (y3 + y4) / 2
- Average Left Edge Position = (x5 + x6) / 2
- Average Right Edge Position = 779 - (x7 + x8) / 2
- Average Rotation = {(x5 - x6 + x7 - x8) + (y2 - y1 + y4 - y3) x 514 / 740} / 2

8. Photo response defect pixels are those whose signal is more than 20% below the mean signal level of all of the pixels. Column defects are defined as those columns with ≥50 defective pixels.
9. Defects in darkness pixels are defined as pixels with signals above a pre-defined threshold when the device is un-illuminated. Column defects are defined as those columns with ≥50 defective pixels. The threshold for defect counting is set to be 50 times the maximum specified mean dark signal at the reference temperature.
10. The procedure for calculating Z_{OUT} is as follows:
    - Measure the output signal for a given level of illumination (nominally 50% of saturation) averaged over a 100 x 100 pixel block.
    - Shunt the amplifier output with a (known) AC coupled resistive load and repeat the output signal measurement.
    - The output impedance can then be calculated from the ratio of the two output signals:

$$\frac{1}{Z_{OUT}} = \frac{1}{R_{TEST}(refsig/shntsig-1)} - \frac{1}{R_{LOAD}}$$

Where: R_{TEST} = test resistive load (nominally 470Ω); R_{LOAD} = CCD output load resistor (nominally 4kΩ); refsig = output signal, no test load; shntsig = output signal with test load.

11. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{ref} ±3 °C.

The test methods and test conditions shall be as per the corresponding test defined in Reference Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Leakage Current on Input Gates	I_L	±1 or (1) ±100%	-	10	nA
Power Supply Current 1	I_{OD}	±25%	-	10	mA
Average Dark Signal	DS_{AV}	±100%	-	125	e/pixel/s

NOTES:

1. Whichever is the greater, referred to the initial value.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{ref} ±3 °C.

The test methods and test conditions shall be as per the corresponding test defined in Reference Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ (Note 2)	Absolute		
			Min	Max	
Leakage Current on Input Gates	I_L	±1 or (1) ± 100%	-	10	nA
Power Supply Current 1	I_{OD}	±25%	-	10	mA
Power Supply Current 2	I_{RD}	-	-	100	nA

Characteristics	Symbols	Limits			Units
		Drift Value Δ (Note 2)	Absolute		
			Min	Max	
DC Output Voltage Level	V_{REF}	-	Note 3		V
Reset Pulse Feedthrough	V_{RESET}	-	-	100	mV
Offset Voltage	V_{OFFSET}	-	-	25	mV
Charge to Voltage Conversion Factor	CVF	-	0.8	1.2	µV/e
Full Well Capacity (Image Section)	V_{SAT-IM}	-	300	-	ke
Full Well Capacity (Readout Register)	V_{SAT-RE}	-	1200	-	ke
Linearity Error (to 240ke/p)	LE	-	-	1	%
Average Dark Signal	DS_{AV}	±100%	-	125	e/pixel/s
Dark Signal Non-uniformity	DSNU	-	-	50	e/pixel/s
Quantum Efficiency (Note 4)	QE				%
Wavelength = 350nm		-	50	-	
Wavelength = 400nm		-	80	-	
Wavelength = 500nm		-	80	-	
Wavelength = 650nm		-	75	-	
Wavelength = 900nm		-	30	-	
Photo Response Non-uniformity (Note 4)	PRNU				%
Wavelength = 400nm (~10nm bandwidth)		-	-	5	
Wavelength = 550nm (~80nm bandwidth)		-	-	3	
Total Charge Transfer Inefficiency - Vertical	VCTI	-	-	1.5	%
Store Shield Position	-	-	-	-	-
Photo Response Defects (Note 4) Pixels Columns	 - -	 - -	 - -	 20 0	-

Characteristics	Symbols	Limits			Units
		Drift Value Δ (Note 2)	Absolute		
			Min	Max	
Defects in Darkness Pixels Columns	-	 - -	 - -	 60 0	-
Output Impedance	Z_{OUT}	-	-	-	-

NOTES:
1. Whichever is greater, referred to the initial value.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. DC level is typically 4 to 6 Volts below V_{OD}.
4. These parameters are not measured as part of the Mechanical and Environmental subgroups of Chart F4 of ESCC Specification No. 9020.

2.6 BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Unit
Case Temperature	T_{case}	125 (+0, -5)	^{o}C
Output Transistor Drain Bias	V_{OD}	25.5	V
Reset Transistor Drain Bias	V_{RD}	10.5	V
Dump Drain Bias	V_{DD}		
Substrate Bias	V_{SS}	0	V
Storage Section Clock	$V_{S\Phi3}$	V_{X0} (Note 3)	V
Dump Gate Bias	V_{DG}		
Isolation Gate Bias	V_{IG}		
Image Section Clock	$V_{I\Phi3}$		
Readout Register Clock	$V_{R\Phi3}$	V_{X1} (Note 3)	V
Readout Register Clock	$V_{R\Phi2}$	V_{X2} (Note 3)	V
Storage Section Clock	$V_{S\Phi2}$		
Image Section Clock	$V_{I\Phi2}$		
Output Reset Pulse	$V_{\Phi R}$		

Characteristics	Symbols	Test Conditions	Unit
Storage Section Clock	$V_{S\Phi1}$	V_{X3} (Note 3)	V
Output Gate Bias	V_{OG}		
Image Section Clock	$V_{I\Phi1}$		
Readout Register Clock	$V_{R\Phi1}$		
Constant Current Load	I_{OS}	7.5 ±1	mA
Switched Voltage Cycle Period	t_{sv}	6 ±0.1	hours
Thermistors (Variant 01 only)	V_{th}	Open	V

NOTES:
1. All voltages are ±0.2V.
2. The CCD is illuminated so that the pixel well capacities are over saturated (to ensure that a sufficient number of holes are generated to pin the silicon surface to V_{SS}).
3. $V_{X0} = V_{X1} = V_{X2} = V_{X3} = -15V$ with a 0V period of duration t_{sv} applied sequentially during each 24 hour period.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Unit
Case Temperature	T_{case}	+20 ±10	^{o}C
Output Transistor Drain Bias	V_{OD}	32 ±1	V
Dump Drain Bias	V_{DD}		
Reset Transistor Drain Bias	V_{RD}	19 ±0.5	V
Substrate Bias	V_{SS}	9 ±1	V
Output Reset Pulse	$V_{\Phi R}$	10 ±0.2	V

Characteristics	Symbols	Test Conditions	Unit
Storage Section Clocks	$V_{S\Phi n}$	0 ±0.2	V
Image Section Clocks	$V_{I\Phi n}$		
Readout Register Clocks	$V_{R\Phi n}$		
Dump Gate Bias	V_{DG}		
Isolation Gate Bias	V_{IG}		
Output Gate Bias	V_{OG}		
Thermistors (Variant 01 only)	V_{th}		
Output Transistor Source Bias	V_{OS}	Note 1	V

NOTES:
1. OS is connected to 0V via a 3.6kΩ resistor to give approximately 7mA in the CCD output transistor.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation the devices shall have successfully met Reference Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{ref} ±3 ^{o}C.

The test methods and test conditions shall be as per the corresponding test defined in Reference Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation are shown below.

Characteristics	Symbols	Limits		Units
		Min	Max	
Leakage Current on Input Gates	I_L	-	10	nA
Power Supply Current 1	I_{OD}	-	10	mA
Power Supply Current 2	I_{RD}	-	100	nA
DC Output Voltage Level	V_{REF}	Note 2		V
Offset Voltage (Note 3)	V_{OFFSET}	-	25	mV
Charge to Voltage Conversion Factor (Note 3)	CVF	0.8	1.2	µV/e
Full Well Capacity (Image Section)	V_{SAT-IM}	300	-	ke
Full Well Capacity (Readout Register)	V_{SAT-RE}	1200	-	ke

Characteristics	Symbols	Limits		Units
		Min	Max	
Linearity Error (to 240ke/p)	LE	-	2	%
Average Dark Signal (Nominal V_{SS}) (Note 4)	DS_{AV}	-	150	e/pixel/s
Dark Signal Non-uniformity (Note 3)	DSNU	-	75	e/pixel/s
Total Charge Transfer Inefficiency - Vertical	VCTI	-	2	%
Photo Response Defects Pixels Columns	-	 - -	 20 0	-
Defects in Darkness Pixels Columns (Note 5)	-	 - -	 60 0	-

NOTES:

1. The limits listed are valid for measurements during and on completion of irradiation and after annealing.
2. DC level is typically 4 to 6 Volts below V_{OD}.
3. V_{OD}, V_{RD} and V_{SS} bias voltages may require correction for irradiation induced threshold shift to perform these measurements.
4. Measurements may be performed at various V_{SS} settings to determine the threshold voltage shift after irradiation.
5. Defect Threshold to be scaled with the increased limit for Dark Signal.

APPENDIX A

AGREED DEVIATIONS FOR E2V TECHNOLOGIES

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control	Wafer Lot Acceptance Total Dose Radiation Testing. The sample size defined in ESCC Basic Specification No. 22900 shall be replaced by a minimum sample of 4 test devices, selected at random from a minimum of two different diffusion lots making a minimum of 8 samples in all.