CHARGE COUPLED DEVICES, SILICON, PHOTOSENSITIVE, FRONT ILLUMINATED, 512 X 512 IMAGE AREA, FRAME TRANSFER

BASED ON TYPE CCD57-10

ESCC Detail Specification No. 9610/005

Issue 2	April 2014

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
849	Specification upissued to incorporate editorial changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical, electro-optical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9020.
(b) ESCC 25000, Electro-optical Test Methods for Charge Coupled Devices.
(c) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 961000501D

- Detail Specification Reference: 9610005
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: D (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Reference Temperature T_{ref} (^{o}C)	Case	Weight Max (g)	Total Dose Radiation Level Letter
01	CCD57-10-*-B19	-30	DIP	10	D [10kRAD(Si)]

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Input Voltage	V_{IN}	-20 to +20	V	Notes 1, 3
Input Voltage	V_{IN}	-0.3 to +25	V	Notes 2, 3
Input Voltage, Pin OD	V_{IN}	-0.3 to +35	V	Notes 3, 4
Output Voltage, Pin OS	V_{OUT}	-0.3 to +25	V	Notes 3, 4
Operating Temperature Range	T_{op}	-55 to +50	^{o}C	Note 5
Storage Temperature Range	T_{stg}	-55 to +125	^{o}C	
Rate of Change of Temperature	-	5	^{o}C/min	Note 6

NOTES:

1. For input pins ΦR, IΦn, RΦn, SΦn, DG, OG, ABG.
2. For input pins RD, ABD.
3. With respect to V_{SS}.
4. Maximum voltage applied between OD and OS shall not exceed ±15V.
5. Device is functional for $-55 \leq T_{op} \leq +125$ ^{o}C but with degraded performance. Parameters are not guaranteed in this temperature range.
6. Rate of change of temperature is applicable over the operating and storage temperature ranges.

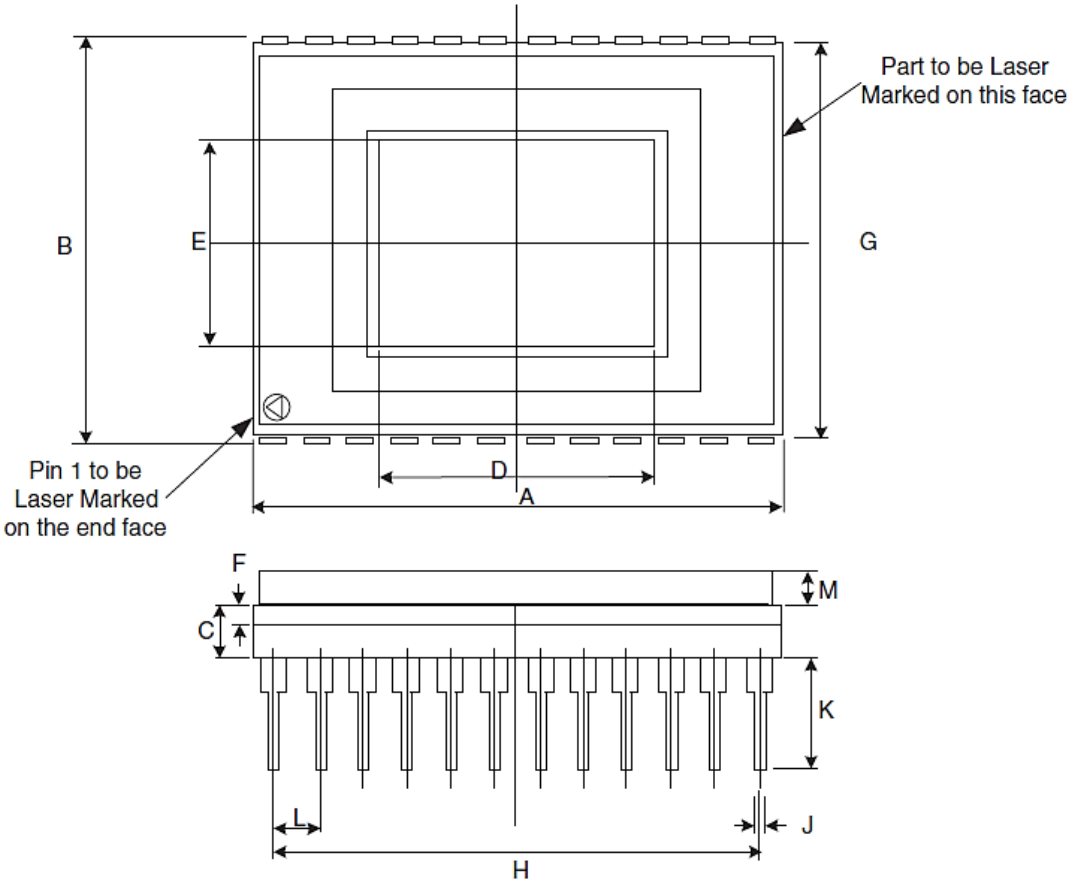
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Dual-in-Line Package (DIP) - 24 Pin

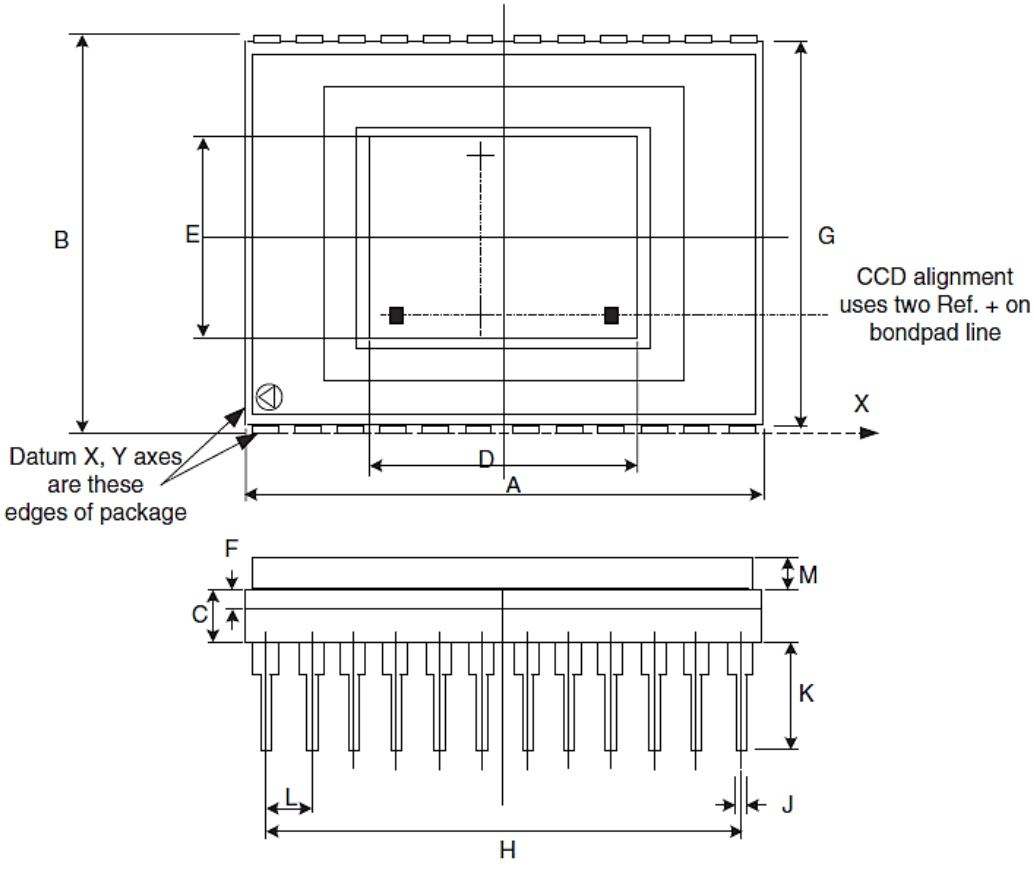


Symbol	Dimensions mm		Notes
	Min.	Max.	
A	29.64	30.24	
B	22.61	23.11	
C	2.43	2.97	
D	15.5	15.6	
E	13.1	13.2	
F	0.55	1.55	1
G	22.36	22.86	
H	27.81	28.07	2
J	0.41	0.51	3
K	5.6 Nom.		3

Symbol	Dimensions mm		Notes
	Min.	Max.	
L	2.54 BSC		4, 5
M	1.9	2.1	

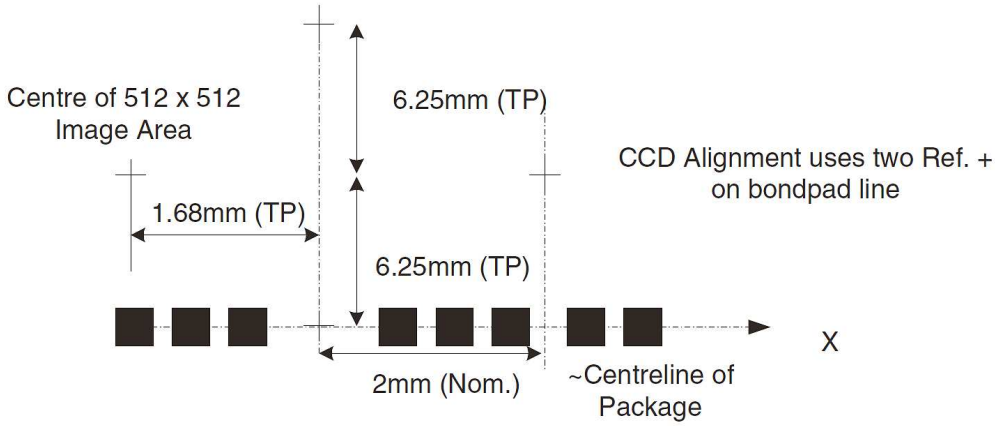
NOTES:
1. Dimension is to nominal CCD image plane.
2. 2 places.
3. All terminals.
4. 22 spaces.
5. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within 0.13mm of its true longitudinal position relative to Pin 1.

1.7.2 Geometrical References



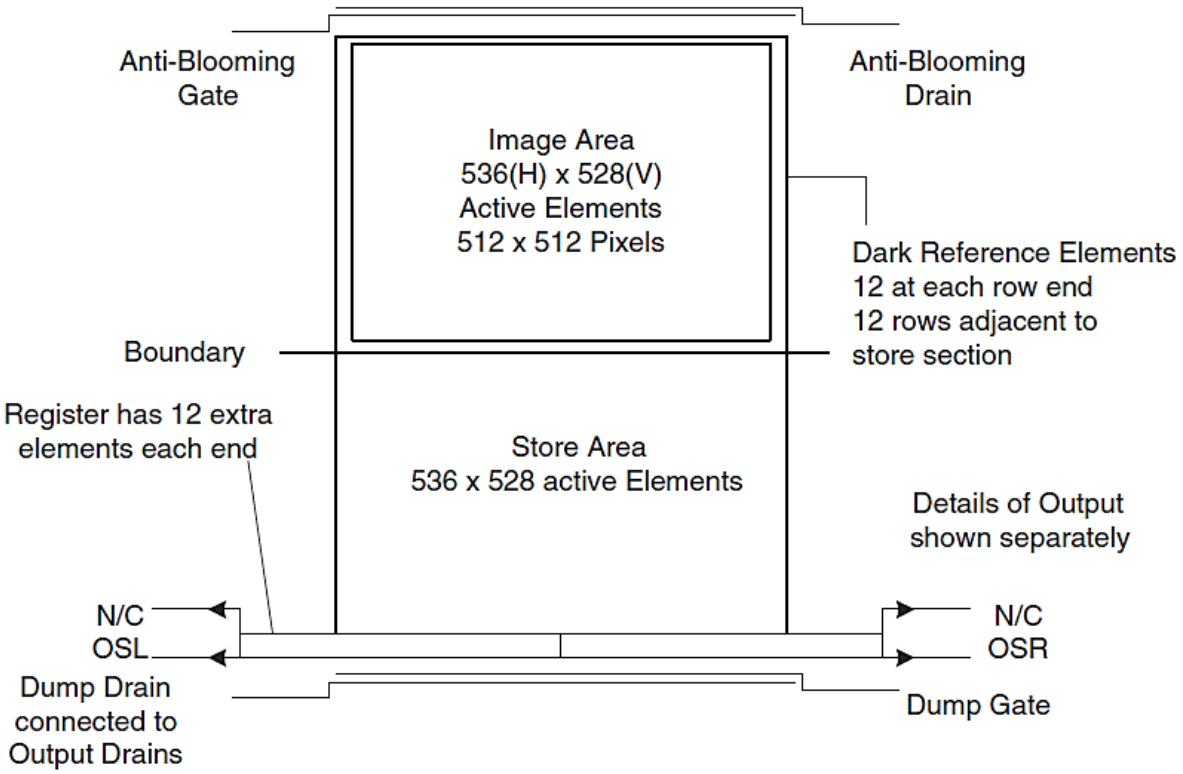
NOTES:
1. Angular alignment, CCD Reference marks to X datum edge of package = 90 ±0.5°.
2. The CCD is positioned within the package to a tolerance of ±0.2mm. Details of the CCD position/alignment are shown below.

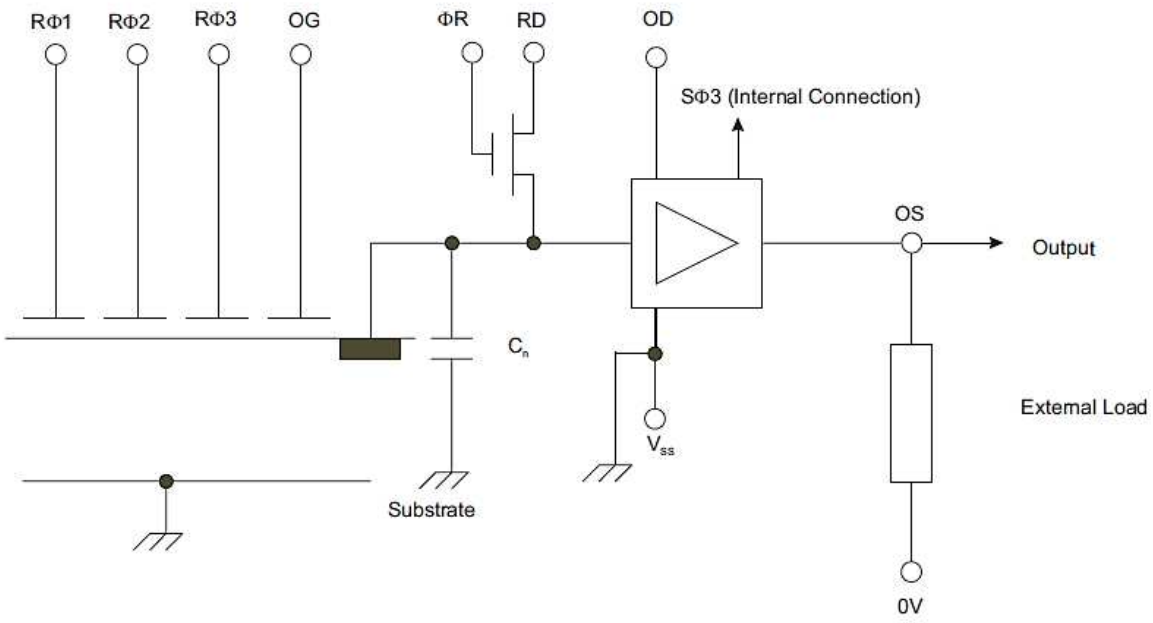
Detailed View



TP = True Position

1.8 FUNCTIONAL DIAGRAM





1.9 PIN ASSIGNMENT

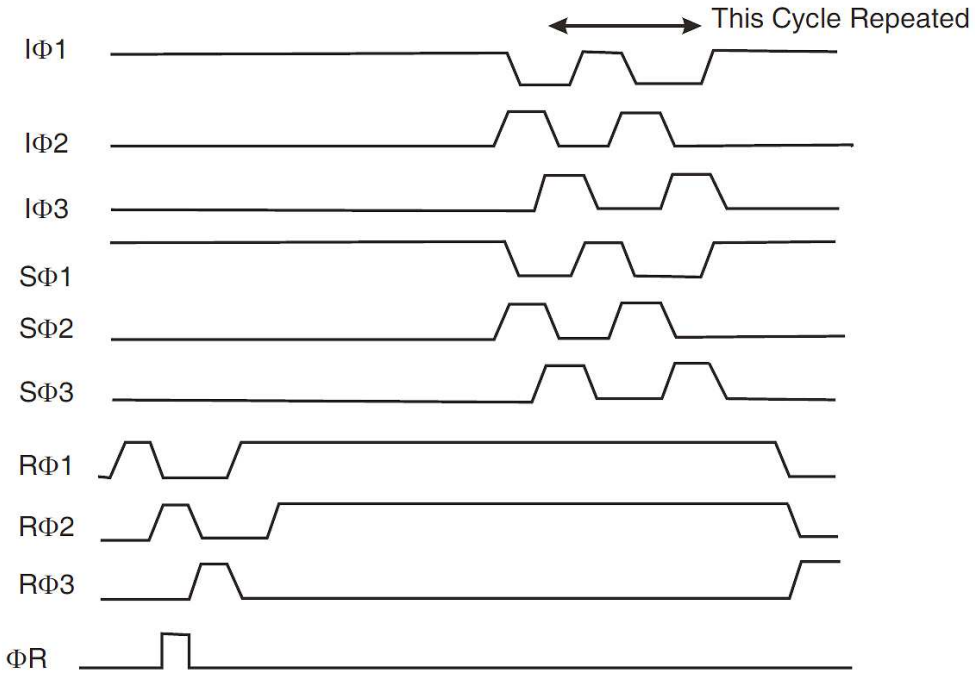
Pin	Function
1	ABD Input (Anti-Blooming Drain)
2	IΦ3 Input (Image Section Clock)
3	IΦ2 Input (Image Section Clock)
4	IΦ1 Input (Image Section Clock)
5	OG Input (Output Gate)
6	OSL Output (Output Transistor Source - Left Amplifier)
7	V_{SS} (Substrate Bias)
8	ΦR Input (Output Reset Pulse)
9	RΦ2L Input (Readout Register Clock - Left Half)
10	RΦ1L Input (Readout Register Clock - Left Half)
11	OD Input (Output Transistor Drain)
12	-
13	-

Pin	Function
14	RD Input (Reset Transistor Drain)
15	RΦ1R Input (Readout Register Clock - Right Half)
16	RΦ2R Input (Readout Register Clock - Right Half)
17	RΦ3 Input (Readout Register Clock)
18	V_{SS} (Substrate Bias, Ground)
19	OSR Output (Output Transistor Source - Right Amplifier)
20	DG Input (Dump Gate)
21	SΦ1 Input (Storage Section Clock)
22	SΦ2 Input (Storage Section Clock)
23	SΦ3 Input (Storage Section Clock)
24	ABG Input (Anti-Blooming Gate)

1.10 TIMING DIAGRAMS

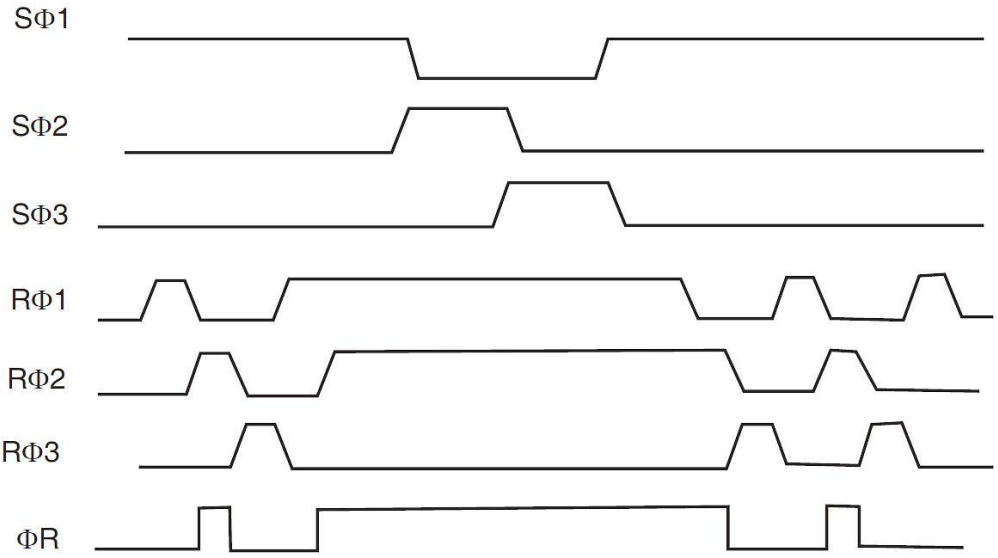
Frame Transfer Clock Diagram

Detail of Frame Transfer – Image to Store



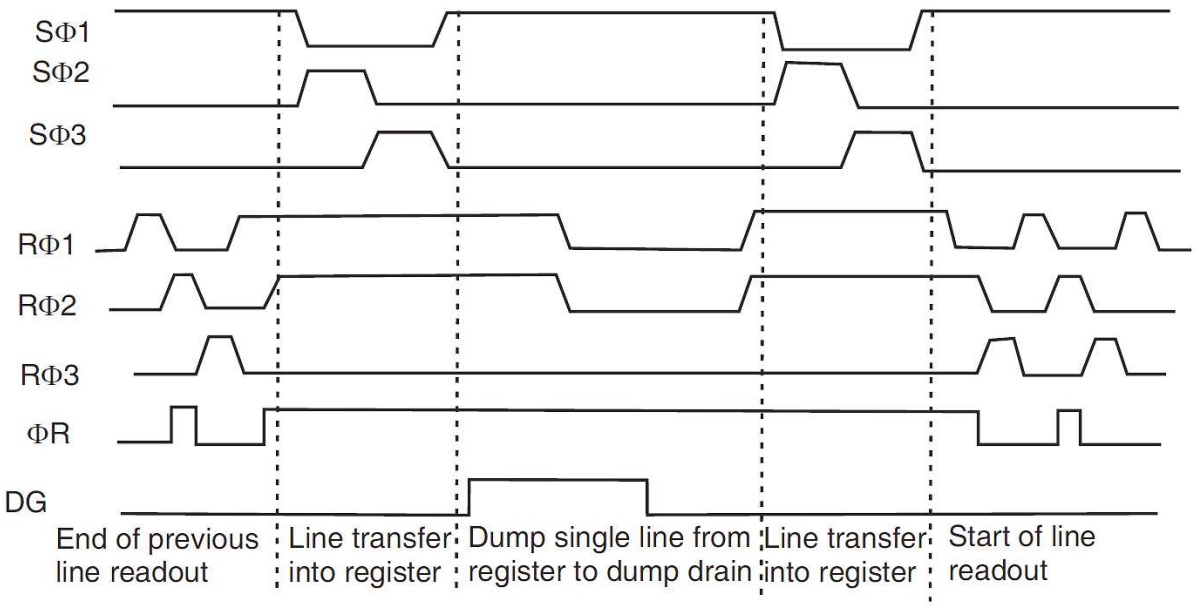
Line Transfer Clock Diagram

Detail of Line Transfer – Store to Readout Register

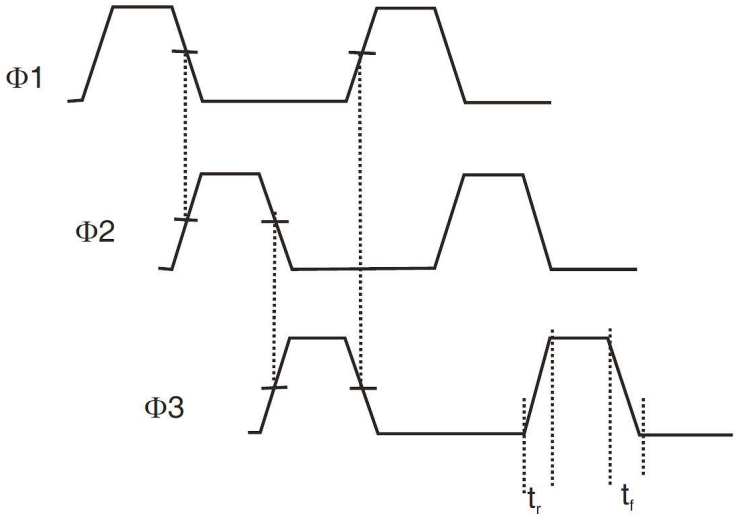


Operation of CCD Dump Gate for Single Line Dumping

Detail of Vertical Line Transfer – Single Line Dump



Drive Pulse Waveforms

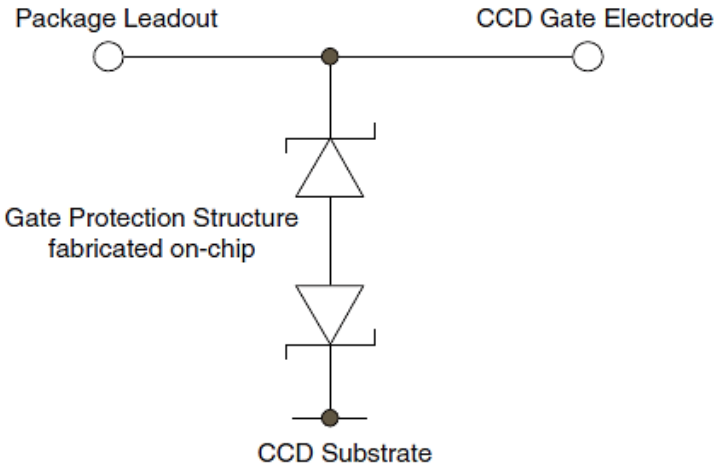


NOTES:

1. Pulses should be symmetrical and overlap at 50% points, as shown.
2. Rise and fall times (t_r, t_f), 10 to 90%, are defined in Note 2 of Notes to Electrical Measurement Tables herein.

1.11 INPUT PROTECTION NETWORK

Inputs IΦn, RΦn, SΦn, ΦR, OG, DG and ABG are protected as shown:



1.12 MATERIALS AND FINISHES

(a) CCD Package
The CCD package shall be of multilayered co-fired aluminium oxide construction.

(b) Input Window/Lid Seal
None

(c) Terminal Material and Finish
The terminal material shall be Type G in accordance with ESCC Basic Specification No. 23500. The terminal finish shall be gold, thickness 1.524µm min over nickel, thickness 1.27µm min, 8.89µm max.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Production Control

(a) Rebonding of wire bonds is permitted as defined:
No more than three rebonds are permitted anywhere on any one device. No bondlink may be reworked more than once; i.e. there may be no more than two bond feet, or attempted bond feet, on any bond pad, whether chip or package. No more than two adjacent bond pads, on chip or package, may be subjected to rebonding.

2.1.1.2 Deviations from Qualification and Periodic Tests - Chart F4

(a) Permanence of Marking shall not be performed.
(b) Operating Life. For Periodic Tests, the duration shall be 1000 hours, with electrical measurements performed in accordance with Intermediate and End-Point Electrical Measurements herein at 0 and 1000 ±48 hours.

2.1.1.3 Deviations from Data Documentation Report

(a) Special In-Process Controls data shall be held by the manufacturer and not delivered.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT REFERENCE, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at reference, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Reference Temperature Electrical Measurements

Unless otherwise specified the measurements shall be performed at T_{ref} ±3 °C.

Characteristics	Symbols	ESCC 25000 Test Method Para.	Test Conditions	Limits		Units
				Min	Max	
Leakage Current on Input Gates	I_L	5.1	V_{IN}(Input Gates) = 15V V_{IN}(Remaining Inputs) = 0V V_{OUT} = 0V V_{SS} = 0V T_{amb} = +21 ±3 °C	-	10	nA
Charge to Voltage Conversion Factor	CVF	6.18	Notes 1, 2	4	7	µV/e
Temporal Noise	V_N	6.4	No illumination Notes 1, 2 Pixel frequency = 18.5 kHz	-	4	e_{RMS}
Full Well Capacity (Image Section)	V_{SAT-IM}	6.7(a): Global Method	Uniform illumination Notes 1, 2	65 Note 3	-	ke
Average Dark Signal	DS_{AV}	6.20	Notes 1, 2	-	125	e/pixel/s
Dark Signal Non-uniformity	DSNU	6.21	Notes 1, 2	-	15	e/pixel/s
Quantum Efficiency	QE	6.19	Uniform illumination Notes 1, 2, 4 Wavelength = 500nm 650nm 900nm	 15 38 18	 - - -	%
Photo Response Non-uniformity	PRNU	6.14	Uniform illumination Notes 1, 2 Wavelength = 650nm	-	4	%
Photo Response Defects Pixels Columns	-	-	Notes 1, 2, 5 (Identified from the data frame of the measurement of PRNU)	 - -	 10 1	-
Defects in Darkness Pixels Columns	-	-	Notes 1, 2, 6	 - -	 15 0	-
Power Supply Current	I_{OD}	5.3	Notes 1, 2	-	10	mA

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at temperatures defined below.

Characteristics	Symbols	ESCC 25000 Test Method Para.	Test Conditions Note 7	Limits		Units
				Min	Max	
Charge to Voltage Conversion Factor	CVF	6.18	Notes 1, 2 T_{amb} = -55 (+5 -0) ^{o}C	4	7	µV/e
Power Supply Current	I_{OD}	5.3	Notes 1, 2 T_{amb} = +50 (+0 -5) ^{o}C T_{amb} = -55 (+5 -0) ^{o}C	- -	10 10	mA

2.3.3 Notes to Electrical Measurement Tables

1. The CCD shall be biased as follows during electro-optical tests:

Parameter	Symbol	Conditions	Unit
Output Amplifier Drain	V_{OD}	30 (+2, -3)	V
Reset Drain Bias	V_{RD}	18 (+3, -1)	V
Substrate Bias	V_{SS}	9 ±2	V
Output Gate Bias	V_{OG}	3 ±2	V
Anti-Blooming Drain	V_{ABD}	19 (+5, -2)	V
Anti-Blooming Gate	V_{ABG}	0 (+5, -0)	V

2. All Clock Low Levels taken as 0 ±0.5V, except Readout Clock Low = 1 ±0.5V. Readout frequency ~34 kHz (except for Noise measurement ~18.5 kHz), External Load Resistance on test camera ~5.6kΩ.

Clock Description	Parameter	Conditions	Unit
Image Clocks IΦn	High Level	12 (+3 -2)	V
	Line Transfer Time	≥ 1	µs
	Pulse Width	35 TYPICAL	
	Rise/Fall Times	≥ 100	ns
	Overlap	≥ 90	%

Clock Description	Parameter	Conditions	Unit
Store Clocks SΦn	High Level	12 (+3 -2)	V
	Line Transfer Time	≥ 1	ms
	Pulse Width	35 TYPICAL	
	Rise/Fall Times	≥ 100	ns
	Overlap	≥ 90	%
Readout Clocks RΦn	High Level	11 (+4 -1)	V
	Rise/Fall Times	≥ 50	ns
	Overlap	100	%
Reset Pulse	High Level	12 (+3 -2)	V
	Rise/Fall Times	≥ 50	ns
Dump Gate DG	High Level	14 (+1 -4)	V

3. The actual Full Well Capacity achievable is dependent upon the bias applied to the V_{ABD} terminal (Anti-Blooming Drain) of the device. It is noted that in the event of a significant shift in the device internal threshold voltage due to irradiation, it may be necessary to reoptimise the anti-blooming bias conditions to maintain well capacity.
4. The average response of the complete normal image area shall be measured. The average signal shall be approximately 50% of the measured full well capacity.
5. Photo response defect pixels are those whose signal is more than 20% below the mean signal level of all of the pixels. Column defects are defined as those columns with ≥ 10 defective pixels.
6. Defects in darkness pixels are defined as pixels with signals above a pre-defined threshold when the device is un-illuminated. Column defects are defined as those columns with ≥ 10 defective pixels. The threshold for defect counting is set to be 25 times the maximum specified mean dark signal at the reference temperature.
7. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{ref} ±3 ^{o}C.

The test methods and test conditions shall be as per the corresponding test defined in Reference Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Leakage Current on Input Gates	I_L	±1 or (1) ±100%	-	10	nA
Average Dark Signal	DS_{AV}	±100%	-	125	e/pixel/s

NOTES:
1. Whichever is the greater, referred to the initial value.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{ref} ±3 ^{o}C.

The test methods and test conditions shall be as per the corresponding test defined in Reference Temperature Electrical Measurements.

Characteristics	Symbols	Limits			Units
		Drift Value Δ (Note 2)	Absolute		
			Min	Max	
Leakage Current on Input Gates	I_L	±1 or (1) ±100%	-	10	nA
Charge to Voltage Conversion Factor	CVF	-	4	7	µV/e
Temporal Noise	V_N	-	-	4	e_{RMS}
Full Well Capacity (Image Section)	V_{SAT-IM}	-	Note 4		ke
Average Dark Signal	DS_{AV}	-	-	125	e/pixel/s
Dark Signal Non-uniformity	DSNU	-	-	15	e/pixel/s
Quantum Efficiency (Note 3)	QE				%
Wavelength = 500nm		-	15	-	
Wavelength = 650nm		-	38	-	
Wavelength = 900nm		-	18	-	

Characteristics	Symbols	Limits			Units
		Drift Value Δ (Note 2)	Absolute		
			Min	Max	
Photo Response Non-uniformity (Note 3) Wavelength = 650nm	PRNU	-	-	4	%
Photo Response Defects (Note 3) Pixels Columns	 - -	 - -	 - -	 10 1	
Defects in Darkness Pixels Columns	-	 - -	 - -	 15 0	
Power Supply Current	I_{OD}	-	-	10	mA

NOTES:
1. Whichever is the greater, referred to the initial value.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. These parameters are not measured as part of the Mechanical and Environmental subgroups of Chart F4 of ESCC Generic Specification No. 9020.
4. The limit for qualification and qualification maintenance is 65ke minimum. Measurements made during Lot Verification Testing are for information only. The V_{ABD} bias may require resetting to optimise the Full Well Capacity after Operating Life.

2.6 BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Unit
Case Temperature	T_{case}	+125 (+0 -5)	^{o}C
Output Transistor Drain Bias	V_{OD}	24	V
Anti-Blooming Drain Bias	V_{ABD}	12	V
Reset Transistor Drain Bias	V_{RD}		
Dump Gate Bias	V_{DG}	V_{X0} (Note 3)	V
Anti-Blooming Gate Bias	V_{ABG}		
Image Section Clock	$V_{I\Phi3}$	V_{X1} (Note 3)	V
Readout Register Clock	$V_{R\Phi3}$		
Storage Section Clock	$V_{S\Phi3}$		

Characteristics	Symbols	Test Conditions	Unit
Image Section Clock	$V_{I\Phi1}$	V_{X2} (Note 3)	V
Readout Register Clocks	$V_{R\Phi2L}$		
	$V_{R\Phi2R}$		
Storage Section Clock	$V_{S\Phi1}$		
Output Reset Pulse	$V_{\Phi R}$		
Output Gate Bias	V_{OG}	V_{X3} (Note 3)	V
Image Section Clock	$V_{I\Phi2}$		
Storage Section Clock	$V_{S\Phi2}$		
Readout Register Clocks	$V_{R\Phi1L}$		
	$V_{R\Phi1R}$		
Substrate Bias	V_{SS}	0	V
Constant Current Load	I_{OS}	5 ±1	mA
Switched Voltage Cycle Period	t_{sv}	6 ±0.1	hours

NOTES:
1. All voltages are ±0.2V.
2. The CCD is illuminated so that the pixel well capacities are over saturated (to ensure that a sufficient number of holes are generated to pin the silicon surface to V_{SS}).
3. $V_{X0} = V_{X1} = V_{X2} = V_{X3} = -15V$ with a 0V period of duration t_{sv} applied sequentially during each 24 hour period.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Unit
Case Temperature	T_{case}	+20 ±10	^{o}C
Output Transistor Drain Bias	V_{OD}	30 ±1	V

Characteristics	Symbols	Test Conditions	Unit
Anti-Blooming Drain Bias	V_{ABD}	18 ±0.5	V
Reset Transistor Drain Bias	V_{RD}		
Output Reset Pulse	$V_{\Phi R}$	10 ±0.2	V
Substrate Bias	V_{SS}	9 ±1	V
Image Section Clocks	$V_{I\Phi n}$	0 ±0.2	V
Storage Section Clocks	$V_{S\Phi n}$		
Readout Register Clocks	$V_{R\Phi n}$		
Dump Gate Bias	V_{DG}		
Anti-Blooming Gate Bias	V_{ABG}		
Output Gate Bias	V_{OG}		
Output Transistor Source Bias	V_{OS}	Note 1	V

NOTES:

1. OSL and OSR are connected to 0V via a 5.6kΩ resistor to give approximately 5mA in the CCD output transistor.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation the devices shall have successfully met Reference Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{ref} ±3 ^{o}C.

The test methods and test conditions shall be as per the corresponding test defined in Reference Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation are shown below.

Characteristics	Symbols	Limits		Units
		Min	Max	
Leakage Current on Input Gates	I_L	-	10	nA
Charge to Voltage Conversion Factor (Note 2)	CVF	4	7	µV/e
Temporal Noise (Note 2)	-	-	4	e_{RMS}
Full Well Capacity (Image Section)	V_{SAT-IM}	Note 3		ke
Average Dark Signal (Note 4)	DS_{AV}	-	150	e/pixel/s

Characteristics	Symbols	Limits		Units
		Min	Max	
Dark Signal Non-uniformity (Note 2)	DSNU	-	25	e/pixel/s
Photo Response Defects Pixels Columns	-	 - -	 10 1	-
Defects in Darkness Pixels Columns (Note 5)	-	 - -	 15 0	-

NOTES:

1. The limits listed are valid for measurements during and on completion of irradiation and after annealing.
2. V_{OD}, V_{RD} and V_{SS} bias voltages may require correction for irradiation induced threshold shift to perform these measurements.
3. Measurements shall only be made on completion of irradiation and after annealing. Measurements shall be made for information only. The V_{ABD} bias may require resetting to optimise the Full Well Capacity after irradiation.
4. Measurements may be performed at various V_{SS} settings to determine the threshold voltage shift after irradiation.
5. Defect Threshold to be scaled with the increased limit for Dark Signal.

APPENDIX A

AGREED DEVIATIONS FOR E2V TECHNOLOGIES

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control	Wafer Lot Acceptance Total Dose Radiation Testing. The sample size defined in ESCC Basic Specification No. 22900 shall be replaced by a minimum sample of 4 test devices, selected at random from a minimum of two different diffusion lots making a minimum of 8 samples in all.