



Pages 1 to 23

**INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS DUAL
D-TYPE FLIP-FLOP WITH FULLY BUFFERED OUTPUTS**

BASED ON TYPE 4013B

ESCC Detail Specification No. 9203/023

| | |
|---------|----------|
| Issue 3 | May 2009 |
|---------|----------|



Document Custodian: European Space Agency - see <https://escies.org>

LEGAL DISCLAIMER AND COPYRIGHT

European Space Agency, Copyright © 2009. All rights reserved.

The European Space Agency disclaims any liability or responsibility, to any person or entity, with respect to any loss or damage caused, or alleged to be caused, directly or indirectly by the use and application of this ESCC publication.

This publication, without the prior permission of the European Space Agency and provided that it is not used for a commercial purpose, may be:

- copied in whole, in any medium, without alteration or modification.
- copied in part, in any medium, provided that the ESCC document identification, comprising the ESCC symbol, document number and document issue, is removed.

DOCUMENTATION CHANGE NOTICE

(Refer to <https://escies.org> for ESCC DCR content)

| DCR No. | CHANGE DESCRIPTION |
|------------------|--|
| 255, 447, 485 | Specification up issued to incorporate editorial and technical changes per DCRs. |

TABLE OF CONTENTS

| | | |
|--------------|--|------------------|
| 1. | <u>GENERAL</u> | <u>5</u> |
| 1.1 | Scope | 5 |
| 1.2 | Applicable Documents | 5 |
| 1.3 | Terms, Definitions, Abbreviations, Symbols and Units | 5 |
| 1.4 | The ESCC Component Number and Component Type Variants | 5 |
| 1.4.1 | The ESCC Component Number | 5 |
| 1.4.2 | Component Type Variants | 5 |
| 1.5 | Maximum Ratings | 6 |
| 1.6 | Handling Precautions | 6 |
| 1.7 | Physical Dimensions and Terminal Identification | 6 |
| 1.7.1 | Flat Package (FP) - 14 Pin | 7 |
| 1.7.2 | Dual-in-line Package (DIP) - 14 Pin | 8 |
| 1.7.3 | Chip Carrier Package (CCP) - 20 Terminal | 9 |
| 1.7.4 | Small Outline Ceramic Package (SO) - 14 Pin | 11 |
| 1.7.5 | Notes to Physical Dimensions and Terminal Identification | 12 |
| 1.8 | Functional Diagram | 12 |
| 1.9 | Pin Assignment | 13 |
| 1.10 | Truth Table | 13 |
| 1.11 | Input Protection Network | 14 |
| 2. | <u>REQUIREMENTS</u> | <u>14</u> |
| 2.1 | General | 14 |
| 2.1.1 | Deviations from the Generic Specification | 14 |
| 2.2 | Marking | 14 |
| 2.3 | Electrical Measurements at Room, High and Low Temperatures | 14 |
| 2.3.1 | Room Temperature Electrical Measurements | 15 |
| 2.3.2 | High and Low Temperatures Electrical Measurements | 17 |
| 2.3.3 | Notes to Electrical Measurement Tables | 19 |
| 2.4 | Parameter Drift Values | 20 |
| 2.5 | Intermediate and End-Point Electrical Measurements | 20 |
| 2.6 | High Temperature Reverse Bias Burn-in Conditions | 21 |
| 2.6.1 | N-Channel HTRB | 21 |
| 2.6.2 | P-Channel HTRB | 22 |
| 2.7 | Power Burn-in Conditions | 22 |
| 2.8 | Operating Life Conditions | 22 |
| APPENDIX 'A' | | 23 |

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920302301

- Detail Specification Reference: 9203023
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

| Variant Number | Based on Type | Case | Terminal Material and /or Finish | Weight max g |
|----------------|---------------|------|----------------------------------|--------------|
| 01 | 4013B | FP | G2 | 0.7 |
| 02 | 4013B | FP | G4 | 0.7 |
| 03 | 4013B | DIP | G2 | 2.2 |
| 04 | 4013B | DIP | G4 | 2.2 |
| 07 | 4013B | CCP | 2 | 0.6 |
| 08 | 4013B | SO | G2 | 0.7 |
| 09 | 4013B | SO | G4 | 0.7 |

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

| Characteristics | Symbols | Maximum Ratings | Units | Remarks |
|--|-----------|------------------------|-------------|--------------------|
| Supply Voltage | V_{DD} | -0.5 to 18 | V | Note 1 |
| Input Voltage | V_{IN} | -0.5 to $V_{DD} + 0.5$ | V | Note 1 Power on |
| Input Current | I_{IN} | ± 10 | mA | - |
| Device Power Dissipation (Continuous) | P_D | 200 | mW | - |
| Power Dissipation per Output | P_{DSO} | 100 | mW | - |
| Operating Temperature Range | T_{op} | -55 to +125 | $^{\circ}C$ | T_{amb} |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}C$ | - |
| Soldering Temperature For FP, DIP and SO For CCP | T_{sol} | +265 +245 | $^{\circ}C$ | Note 2 Note 3 |

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 15V$.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

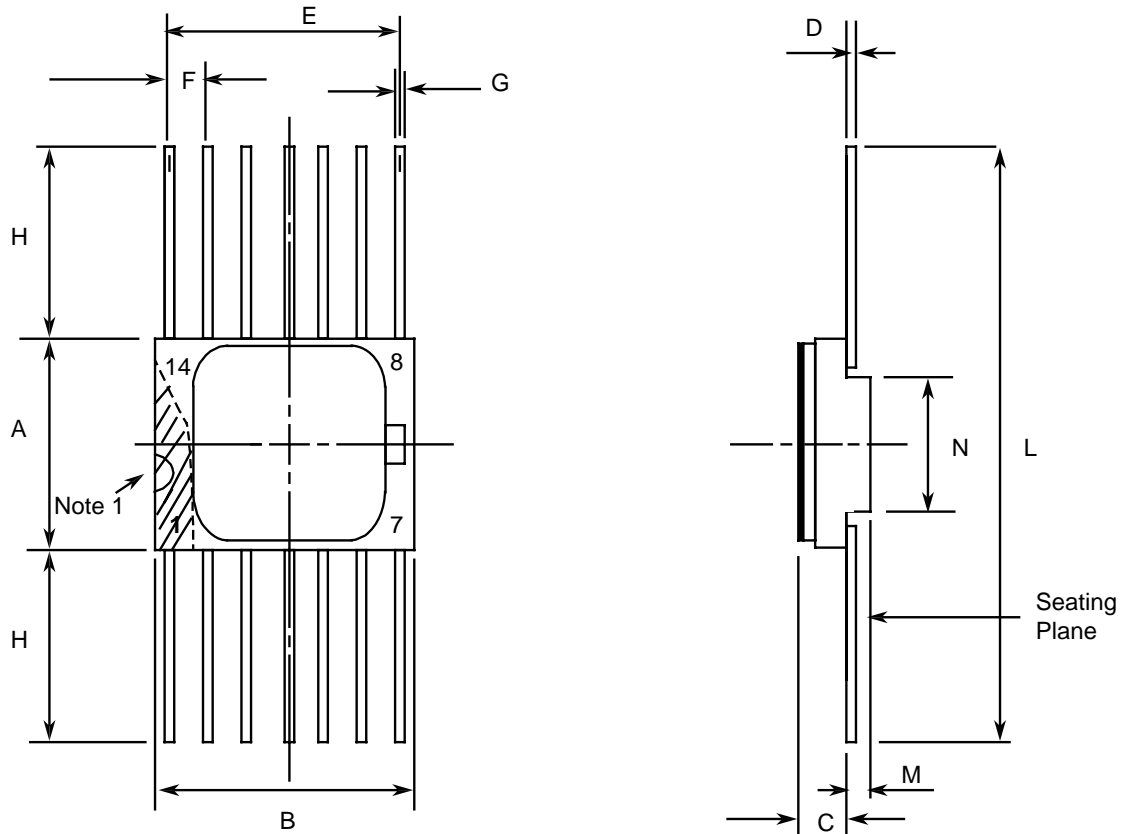
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

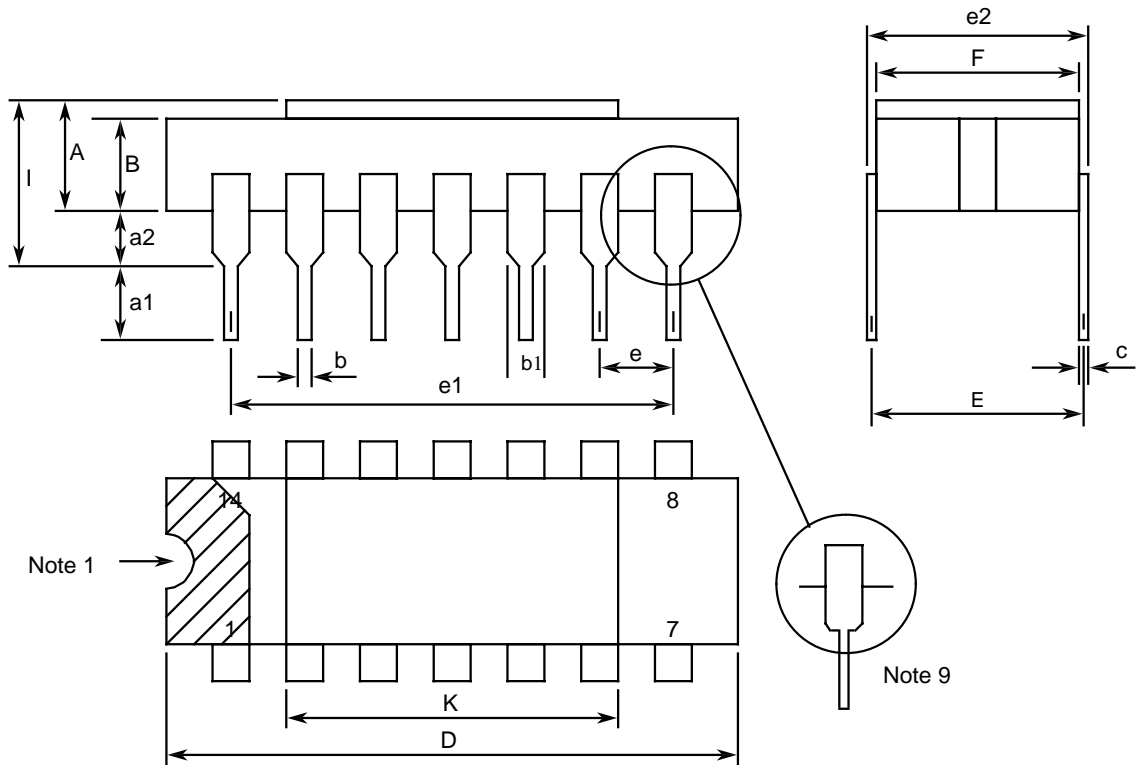
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 14 Pin



| Symbols | Dimensions mm | | Notes |
|---------|---------------|-------|-------|
| | Min | Max | |
| A | 6.75 | 7.06 | |
| B | 9.76 | 10.14 | |
| C | 1.49 | 1.95 | |
| D | 0.1 | 0.15 | 5 |
| E | 7.5 | 7.75 | |
| F | 1.27 BSC | | 3, 6 |
| G | 0.38 | 0.48 | 5 |
| H | 6 | - | 5 |
| L | 18.75 | 22 | |
| M | 0.33 | 0.43 | |
| N | 4.32 TYPICAL | | |

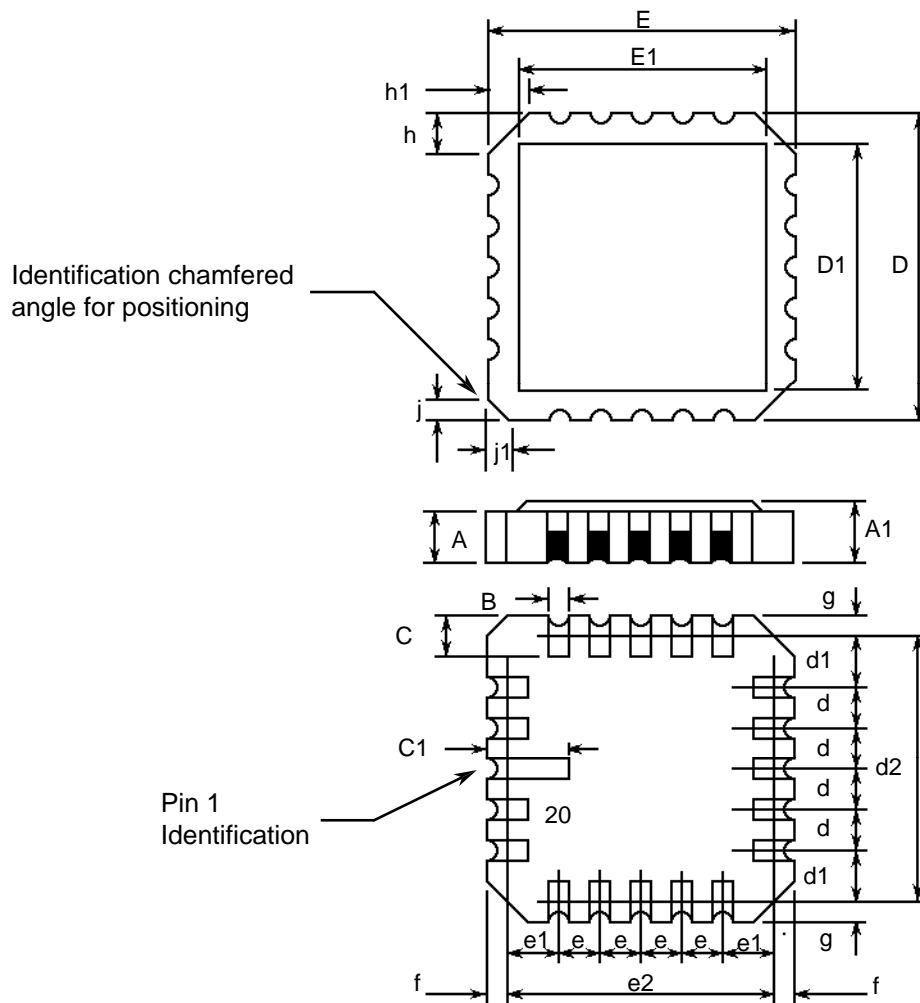
1.7.2 Dual-in-line Package (DIP) - 14 Pin



| Symbols | Dimensions mm | | Notes |
|---------|---------------|-------|-------|
| | Min | Max | |
| A | 2.1 | 2.54 | |
| a1 | 3 | 3.7 | |
| a2 | 0.63 | 1.14 | 2 |
| B | 1.82 | 2.23 | |
| b | 0.4 | 0.5 | 5 |
| b1 | 1.27 TYPICAL | | 5 |
| c | 0.2 | 0.3 | 5 |
| D | 18.79 | 19.2 | |
| E | 7.36 | 7.87 | |
| e | 2.54 BSC | | 4, 6 |
| e1 | 15.11 | 15.37 | |
| e2 | 7.62 | 8.12 | |
| F | 7.11 | 7.75 | |
| I | - | 3.7 | |

| Symbols | Dimensions mm | | Notes |
|---------|---------------|------|-------|
| | Min | Max | |
| K | 10.9 | 12.1 | |

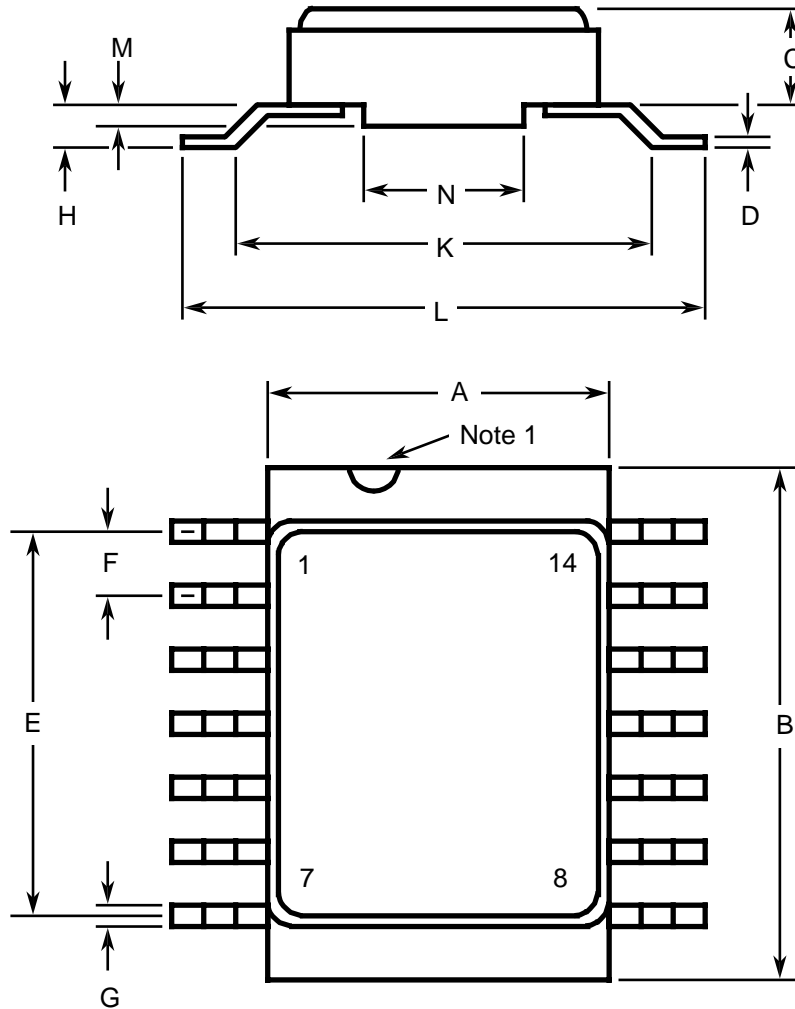
1.7.3 Chip Carrier Package (CCP) - 20 Terminal



| Symbols | Dimensions mm | | Notes |
|---------|---------------|------|-------|
| | Min | Max | |
| A | 1.14 | 1.95 | |
| A1 | 1.63 | 2.36 | |
| B | 0.55 | 0.72 | 5 |
| C | 1.06 | 1.47 | 5 |
| C1 | 1.91 | 2.41 | |

| Symbols | Dimensions mm | | Notes |
|---------|---------------|------|-------|
| | Min | Max | |
| D | 8.67 | 9.09 | |
| D1 | 7.21 | 7.52 | |
| d, d1 | 1.27 BSC | | 3 |
| d2 | 7.62 BSC | | |
| E | 8.67 | 9.09 | |
| E1 | 7.21 | 7.52 | |
| e, e1 | 1.27 BSC | | 3 |
| e2 | 7.62 BSC | | |
| f, g | - | 0.76 | |
| h, h1 | 1.01 TYPICAL | | 8 |
| j, j1 | 0.51 TYPICAL | | 7 |

1.7.4 Small Outline Ceramic Package (SO) - 14 Pin



| Symbols | Dimensions mm | | Notes |
|---------|---------------|-------|-------|
| | Min | Max | |
| A | 6.75 | 7.06 | |
| B | 9.76 | 10.14 | |
| C | 1.49 | 1.95 | |
| D | 0.1 | 0.15 | 5 |
| E | 7.5 | 7.75 | |
| F | 1.27 BSC | | 3, 6 |
| G | 0.38 | 0.48 | 5 |
| H | 0.6 | 0.9 | 5 |
| K | 9 TYPICAL | | |
| L | 10 | 10.65 | |

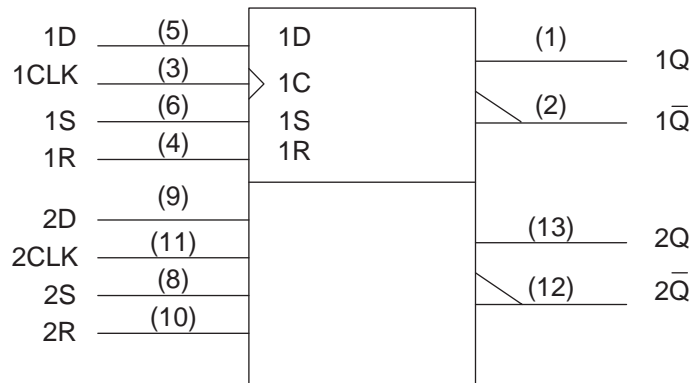
| Symbols | Dimensions mm | | Notes |
|---------|---------------|------|-------|
| | Min | Max | |
| M | 0.33 | 0.43 | |
| N | 4.31 TYPICAL | | |

1.7.5 Notes to Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ± 0.13 mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25 mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 12 spaces.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only.



1.9 PIN ASSIGNMENT

| Pin | Function | | Pin | Function | |
|-----|--------------------|--------------------|-----|--------------------|--------------------|
| | FP, DIP and SO | CCP | | FP, DIP and SO | CCP |
| 1 | 1Q Output | - | 11 | 2CLK Input (Clock) | - |
| 2 | 1 \bar{Q} Output | 1Q Output | 12 | 2 \bar{Q} Output | 2S Input (Set) |
| 3 | 1CLK Input (Clock) | - | 13 | 2Q Output | - |
| 4 | 1R Input (Reset) | 1 \bar{Q} Output | 14 | V _{DD} | 2D Input (Data) |
| 5 | 1D Input (Data) | 1CLK Input (Clock) | 15 | - | 2R Input (Reset) |
| 6 | 1S Input (Set) | 1R Input (Reset) | 16 | - | 2CLK Input (Clock) |
| 7 | V _{SS} | 1D Input (Data) | 17 | - | 2 \bar{Q} Output |
| 8 | 2S Input (Set) | - | 18 | - | - |
| 9 | 2D Input (Data) | 1S Input (Set) | 19 | - | 2Q Output |
| 10 | 2R Input (Reset) | V _{SS} | 20 | - | V _{DD} |

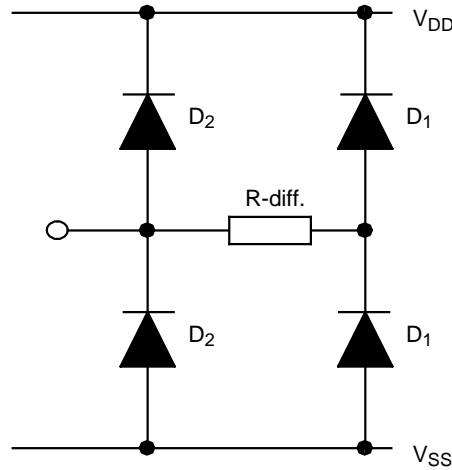
1.10 TRUTH TABLE

- Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
- ↑ = Transition, Low to High; ↓ = Transition, High to Low.
- Q₀ or \bar{Q}_0 = The level of Q or \bar{Q} respectively before the indicated steady state input conditions are established.

EACH FLIP-FLOP

| INPUTS | | | | OUTPUTS | |
|--------|---|---|---|----------------|-------------|
| CLK | D | R | S | Q | \bar{Q} |
| ↑ | L | L | L | L | H |
| ↑ | H | L | L | H | L |
| ↓ | X | L | L | Q ₀ | \bar{Q}_0 |
| X | X | H | L | L | H |
| X | X | L | H | H | L |
| X | X | H | H | H | H |

1.11 INPUT PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb}=+22 \pm 3^{\circ}C$.

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|--|-----------|-------------------------|---|--------|-----|---------|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table without Load $V_{IL}=0V, V_{IH}=3V$ $V_{DD}=3V, V_{SS}=0V$ Note 2 | - | - | - |
| Functional Test 2 | - | 3014 | Verify Truth Table without Load $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 2 | - | - | - |
| Quiescent Current | I_{DD} | 3005 | $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 3 | - | 500 | nA |
| Low Level Input Current | I_{IL} | 3009 | V_{IN} (Under Test)=0V $V_{DD}=15V, V_{SS}=0V$ | - | -50 | nA |
| High Level Input Current | I_{IH} | 3010 | V_{IN} (Under Test)=15V $V_{DD}=15V, V_{SS}=0V$ | - | 50 | nA |
| Low Level Output Voltage 1 | V_{OL1} | 3007 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 50 | mV |
| Low Level Output Voltage 2 (Noise Immunity) | V_{OL2} | 3007 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OL}=0A$ $V_{DD}=5V, V_{SS}=0V$ | - | 500 | mV |
| Low Level Output Voltage 3 (Noise Immunity) | V_{OL3} | 3007 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 1.5 | V |
| High Level Output Voltage 1 | V_{OH1} | 3006 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 14.95 | - | V |
| High Level Output Voltage 2 (Noise Immunity) | V_{OH2} | 3006 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OH}=0A$ $V_{DD}=5V, V_{SS}=0V$ | 4.5 | - | V |
| High Level Output Voltage 3 (Noise Immunity) | V_{OH3} | 3006 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 13.5 | - | V |
| Low Level Output Current 1 | I_{OL1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OL}=0.4V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 | 510 | - | μA |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---|-----------|----------------------------|---|--------|-----|---------|
| | | | | Min | Max | |
| Low Level Output Current 2 | I_{OL2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OL}=1.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 | 3.4 | - | mA |
| High Level Output Current 1 | I_{OH1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OH}=4.6V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 | -510 | - | μA |
| High Level Output Current 2 | I_{OH2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OH}=13.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 | -3.4 | - | mA |
| Threshold Voltage N-Channel | V_{THN} | - | 1CLK Input at Ground All Other Inputs: $V_{IN}=5V$ $V_{DD}=5V, I_{SS}=-10\mu A$ | -0.7 | -3 | V |
| Threshold Voltage P-Channel | V_{THP} | - | 1CLK Input at Ground All Other Inputs: $V_{IN}=-5V$ $V_{SS}=-5V, I_{DD}=10\mu A$ | 0.7 | 3 | V |
| Input Clamp Voltage 1, to V_{SS} | V_{IC1} | - | I_{IN} (Under Test) = -100 μA V_{DD} =Open, $V_{SS}=0V$ All Other Pins Open | - | -2 | V |
| Input Clamp Voltage 2, to V_{DD} | V_{IC2} | - | V_{IN} (Under Test)=6V $R=30k\Omega, V_{SS}$ =Open All Other Pins Open Note 5 | 3 | - | V |
| Input Capacitance | C_{IN} | 3012 | V_{IN} (Not Under Test)=0V $V_{DD}=V_{SS}=0V$ $f = 100$ kHz to 1 MHz Note 6 | - | 7.5 | pF |
| Propagation Delay Low to High, 1CLK to 1Q | t_{PLH} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 250 | ns |
| Propagation Delay High to Low, 1CLK to 1Q | t_{PHL} | 3003 | V_{IN} (Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=5V,$ $V_{DD}=5V, V_{SS}=0V$ Note 7 | - | 250 | ns |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|---------------------------------|------------------|-------------------------|---|--------|-----|-------|
| | | | | Min | Max | |
| Transition Time Low to High, 1Q | t _{TLH} | 3004 | V _{IN} (Under Test)=Pulse Generator V _{IN} (Remaining Inputs)=Truth Table V _{IL} =0V, V _{IH} =5V, V _{DD} =5V, V _{SS} =0V Note 7 | - | 150 | ns |
| Transition Time High to Low, 1Q | t _{THL} | 3004 | V _{IN} (Under Test)=Pulse Generator V _{IN} (Remaining Inputs)=Truth Table V _{IL} =0V, V _{IH} =5V, V _{DD} =5V, V _{SS} =0V Note 7 | - | 150 | ns |
| Maximum Clock Frequency, 1CLK | f _{CLK} | - | V _{IN} (1CLK)=Pulse Generator V _{IN} (Remaining Inputs)=Truth Table V _{IL} =0V, V _{IH} =5V, V _{DD} =5V, V _{SS} =0V Notes 8, 9 | 3.5 | - | MHz |

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5)^oC and T_{amb}=- 55(+5-0)^oC.

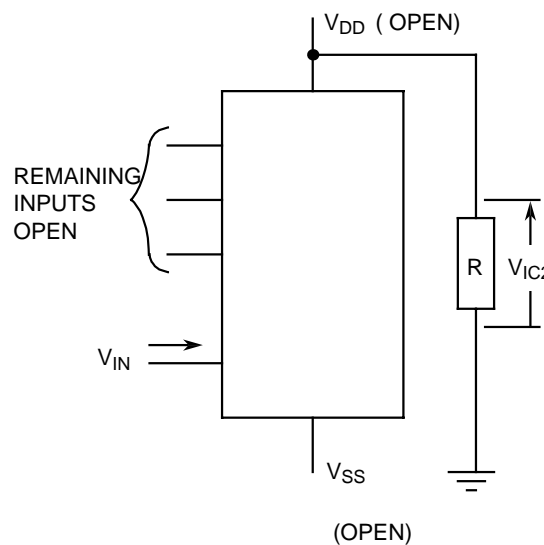
| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|-------------------------|-----------------|-------------------------|--|--------|-------------|-------|
| | | | | Min | Max | |
| Functional Test 1 | - | 3014 | Verify Truth Table without Load V _{IL} =0V, V _{IH} =3V V _{DD} =3V, V _{SS} =0V Note 2 | - | - | - |
| Functional Test 2 | - | 3014 | Verify Truth Table without Load V _{IL} =0V, V _{IH} =15V V _{DD} =15V, V _{SS} =0V Note 2 | - | - | - |
| Quiescent Current | I _{DD} | 3005 | V _{IL} =0V, V _{IH} =15V V _{DD} =15V, V _{SS} =0V Note 3 T _{amb} =+125 ^o C T _{amb} =- 55 ^o C | - - | 15 0.5 | μA |
| Low Level Input Current | I _{IL} | 3009 | V _{IN} (Under Test)=0V V _{DD} =15V, V _{SS} =0V T _{amb} =+125 ^o C T _{amb} =- 55 ^o C | - - | -100 -50 | nA |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|--|-----------|----------------------------|--|--------------|-----------|---------|
| | | | | Min | Max | |
| High Level Input Current | I_{IH} | 3010 | V_{IN} (Under Test)=15V $V_{DD}=15V, V_{SS}=0V$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | - - | 100 50 | nA |
| Low Level Output Voltage 1 | V_{OL1} | 3007 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 50 | mV |
| Low Level Output Voltage 2 (Noise Immunity) | V_{OL2} | 3007 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OL}=0A$ $V_{DD}=5V, V_{SS}=0V$ | - | 500 | mV |
| Low Level Output Voltage 3 (Noise Immunity) | V_{OL3} | 3007 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OL}=0A$ $V_{DD}=15V, V_{SS}=0V$ | - | 1.5 | V |
| High Level Output Voltage 1 | V_{OH1} | 3006 | $V_{IL}=0V, V_{IH}=15V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 14.95 | - | V |
| High Level Output Voltage 2 (Noise Immunity) | V_{OH2} | 3006 | $V_{IL}=1.5V, V_{IH}=3.5V,$ $I_{OH}=0A$ $V_{DD}=5V, V_{SS}=0V$ | 4.5 | - | V |
| High Level Output Voltage 3 (Noise Immunity) | V_{OH3} | 3006 | $V_{IL}=4V, V_{IH}=11V,$ $I_{OH}=0A$ $V_{DD}=15V, V_{SS}=0V$ | 13.5 | - | V |
| Low Level Output Current 1 | I_{OL1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OL}=0.4V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | 360 640 | - - | μA |
| Low Level Output Current 2 | I_{OL2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OL}=1.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | 2.4 4.2 | - - | mA |
| High Level Output Current 1 | I_{OH1} | - | $V_{IL}=0V, V_{IH}=5V,$ $V_{OH}=4.6V$ $V_{DD}=5V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | -360 -640 | - - | μA |
| High Level Output Current 2 | I_{OH2} | - | $V_{IL}=0V, V_{IH}=15V,$ $V_{OH}=13.5V$ $V_{DD}=15V, V_{SS}=0V$ Note 4 $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | -2.4 -4.2 | - - | mA |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions Note 1 | Limits | | Units |
|-----------------------------|-----------|-------------------------|--|--------------|--------------|-------|
| | | | | Min | Max | |
| Threshold Voltage N-Channel | V_{THN} | - | 1CLK Input at Ground All Other Inputs: $V_{IN}=5V$ $V_{DD}=5V, I_{SS}=-10\mu A$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | -0.3 -0.7 | -3.5 -3.5 | V |
| Threshold Voltage P-Channel | V_{THP} | - | 1CLK Input at Ground All Other Inputs: $V_{IN}=-5V$ $V_{SS}=-5V, I_{DD}=10\mu A$ $T_{amb}=+125^{\circ}C$ $T_{amb}=-55^{\circ}C$ | 0.3 0.7 | 3.5 3.5 | V |

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with $V_{OH} \geq V_{DD} - 0.5V$, $V_{OL} \leq 0.5V$. The maximum time to output comparator strobe = 300 μ s.
3. Quiescent Current shall be tested using the following input conditions:
 - (a) Inputs 1CLK = 1R = 1D = 2CLK = 2R = 2D = V_{IH} ; Inputs 1S = 2S = V_{IL}
 - (b) Inputs 1CLK = 1R = 1D = 2CLK = 2R = 2D = V_{IL} ; Inputs 1S = 2S = V_{IH}
 - (c) All inputs = V_{IL}
 - (d) All inputs = V_{IH}
4. Interchange of forcing and measuring parameters is permitted.
5. Input Clamp Voltage 2 to V_{DD} , V_{IC2} , shall be tested on each input as follows:-



6. Guaranteed but not tested.
7. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
The pulse generator shall have the following characteristics:

$V_{GEN} = 0$ to V_{DD} ; $f_{GEN} = 500\text{kHz}$; t_r and $t_f \leq 15$ ns (10% to 90%); duty cycle = 50%; $Z_{out} = 50\Omega$. Output load capacitance $C_L = 50\text{pF} \pm 5\%$ including scope probe, wiring and stray capacitance without component in the test fixture. Output load resistance $R_L = 200\text{k}\Omega \pm 5\%$.

Propagation delay shall be measured referenced to the 50% input and output voltages.

Transition time shall be measured referenced to the 10% and 90% output voltage.

8. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
9. A pulse, having the following conditions, shall be applied to the 1CLK input: $V_P = 0\text{V}$ to V_{DD} . Maximum clock frequency of f_{CLK} requirement is considered met if proper output state changes occur with the pulse repetition rate set to that given in the Limits column.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3^\circ\text{C}$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|-----------------------------|-----------|----------------------|----------|-----|---------------|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Quiescent Current | I_{DD} | ± 75 | - | 500 | nA |
| Low Level Output Current 1 | I_{OL1} | $\pm 15\%$ (2) | 510 | - | μA |
| High Level Output Current 1 | I_{OH1} | $\pm 15\%$ (2) | -510 | - | μA |
| Threshold Voltage N-Channel | V_{THN} | ± 0.3 | -0.7 | -3 | V |
| Threshold Voltage P-Channel | V_{THP} | ± 0.3 | 0.7 | 3 | V |

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Percentage of limit value if voltage is the measuring parameter.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3^\circ\text{C}$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|---|-----------|-------------------------|----------|-----|---------|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Functional Test 1 | - | - | - | - | - |
| Quiescent Current | I_{DD} | ± 75 | - | 500 | nA |
| Low Level Input Current | I_{IL} | - | - | -50 | nA |
| High Level Input Current | I_{IH} | - | - | 50 | nA |
| Low Level Output Voltage 1 | V_{OL1} | - | - | 50 | mV |
| Low Level Output Voltage 2 (Noise Immunity) | V_{OL2} | - | - | 500 | mV |
| High Level Output Voltage 1 | V_{OH1} | - | 14.95 | - | V |
| High Level Output Voltage 2 (Noise Immunity) | V_{OH2} | - | 4.5 | - | V |
| Low Level Output Current 1 | I_{OL1} | $\pm 15\%$ (3) | 510 | - | μA |
| Low Level Output Current 2 | I_{OL2} | $\pm 15\%$ (3) | 3.4 | - | mA |
| High Level Output Current 1 | I_{OH1} | $\pm 15\%$ (3) | -510 | - | μA |
| High Level Output Current 2 | I_{OH2} | $\pm 15\%$ (3) | -3.4 | - | mA |
| Threshold Voltage N-Channel | V_{THN} | ± 0.3 | -0.7 | -3 | V |
| Threshold Voltage P-Channel | V_{THP} | ± 0.3 | 0.7 | 3 | V |

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. Percentage of limit value if voltage is the measuring parameter.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|---|-----------|-----------------|-------------|
| Ambient Temperature | T_{amb} | +125 (+0 -5) | $^{\circ}C$ |
| Outputs 1Q, 1 \bar{Q} , 2Q, 2 \bar{Q} | V_{OUT} | Open | V |
| Inputs 1S, 2D, 2R, 2CLK | V_{IN} | V_{SS} | V |
| Inputs 1CLK, 1R, 1D, 2S | V_{IN} | V_{DD} | V |
| Positive Supply Voltage | V_{DD} | 15 (+0 -0.5) | V |
| Negative Supply Voltage | V_{SS} | 0 | V |
| Duration | t | 72 | Hours |

NOTES:

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

| Characteristics | Symbols | Test Conditions | Units |
|---|------------------|-----------------|-------|
| Ambient Temperature | T _{amb} | +125 (+0 -5) | °C |
| Outputs 1Q, 1 \bar{Q} , 2Q, 2 \bar{Q} | V _{OUT} | Open | V |
| Inputs 1S, 2D, 2R, 2CLK | V _{IN} | V _{DD} | V |
| Inputs 1CLK, 1R, 1D, 2S | V _{IN} | V _{SS} | V |
| Positive Supply Voltage | V _{DD} | 15 (+0 -0.5) | V |
| Negative Supply Voltage | V _{SS} | 0 | V |
| Duration | t | 72 | Hours |

NOTES:

1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

| Characteristics | Symbols | Test Conditions | Units |
|---|--|--------------------------------|-------|
| Ambient Temperature | T _{amb} | +125 (+0 -5) | °C |
| Outputs 1Q, 1 \bar{Q} , 2Q, 2 \bar{Q} | V _{OUT} | V _{DD} /2 | V |
| Inputs 1R, 1S, 2R, 2S | V _{IN} | V _{SS} | V |
| Inputs 1CLK, 2CLK | V _{IN} | V _{GEN1} | V |
| Inputs 1D, 2D | V _{IN} | V _{GEN2} | V |
| Pulse Voltage | V _{GEN} | 0V to V _{DD} | V |
| Pulse Frequency Square Wave | f _{GEN1} f _{GEN2} | ≥50k ≥25k 50% Duty Cycle | Hz |
| Positive Supply Voltage | V _{DD} | 15 (+0 -0.5) | V |
| Negative Supply Voltage | V _{SS} | 0 | V |

NOTES:

1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|--|--|
| <p>Deviations from Screening Tests - Chart F3</p> | <p>External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p> <p>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.</p> <p>Solderability is not applicable unless specifically stipulated in the Purchase Order.</p> |
| <p>Deviations from Qualification and Periodic Tests - Chart F4</p> | <p>External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p> |
| <p>Deviations from High and Low Temperatures Electrical Measurements</p> | <p>High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p> |
| <p>Deviations from Room Temperature Electrical Measurements</p> | <p>All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p> |