INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS, CELL-BASED ARRAY

BASED ON TYPE ATC18RHA

ESCC Detail Specification No. 9202/080

Issue 3	October 2014

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DCR No.	CHANGE DESCRIPTION
867	Specification upissued to incorporate editorial and technical changes per DCR. Specification produced using MSWord. Changes in presentation are possible.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 920208001RXYZ

- Detail Specification Reference: 9202080
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)
- Manufacturer Specific ASIC Identification: XYZ (as applicable) where:
  XYZ : Individual 3 character code allocated by the Manufacturer to a specific ASIC design.

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
01	ATC18RHA95_216	1M	3.3V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]
02	ATC18RHA95_216	1M	3.3V	MQFP-F196	D2 (Note 2)	10	R [100kRAD(Si)]
03	ATC18RHA95_216	1M	3.3V	MQFP-F160	D2 (Note 2)	7	R [100kRAD(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
04	ATC18RHA95_324	2.2M	3.3V	MQFP-T352	D2 (Note 2)	27	R [100kRAD(Si)]
05	ATC18RHA95_324	2.2M	3.3V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]
06	ATC18RHA95_324	2.2M	3.3V	MQFP-F196	D2 (Note 2)	10	R [100kRAD(Si)]
07	ATC18RHA95_324	2.2M	3.3V	MQFP-F160	D2 (Note 2)	7	R [100kRAD(Si)]
08	ATC18RHA95_324	2.2M	3.3V	LGA-349	(Note 3)	7	R [100kRAD(Si)]
09	ATC18RHA95_404	3.5M	3.3V	MQFP-T352	D2 (Note 2)	27	R [100kRAD(Si)]
10	ATC18RHA95_404	3.5M	3.3V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]
11	ATC18RHA95_404	3.5M	3.3V	LGA-625	(Note 3)	9	R [100kRAD(Si)]
12	ATC18RHA95_404	3.5M	3.3V	AIN LGA-625	(Note 4)	29	R [100kRAD(Si)]
13	ATC18RHA95_404	3.5M	3.3V	LGA-472	(Note 3)	9	R [100kRAD(Si)]
14	ATC18RHA95_404	3.5M	3.3V	LGA-349	(Note 3)	7	R [100kRAD(Si)]
15	ATC18RHA95_504	5.5M	3.3V	MQFP-T352	D2 (Note 2)	27	R [100kRAD(Si)]
16	ATC18RHA95_504	5.5M	3.3V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]
17	ATC18RHA95_504	5.5M	3.3V	LGA-625	(Note 3)	9	R [100kRAD(Si)]
18	ATC18RHA95_504	5.5M	3.3V	AIN LGA-625	(Note 4)	29	R [100kRAD(Si)]
19	ATC18RHA95_504	5.5M	3.3V	LGA-472	(Note 3)	9	R [100kRAD(Si)]
20	ATC18RHA95_504	5.5M	3.3V	LGA-349	(Note 3)	7	R [100kRAD(Si)]
21	ATC18RHA95_544	6.5M	3.3V	LGA-625	(Note 3)	9	R [100kRAD(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
22	ATC18RHA95_544	6.5M	3.3V	AIN LGA-625	(Note 4)	29	R [100kRAD(Si)]
23	ATC18RHA95_544	6.5M	3.3V	LGA-472	(Note 3)	9	R [100kRAD(Si)]
24	ATC18RHA95_216	1M	2.5V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]
25	ATC18RHA95_216	1M	2.5V	MQFP-F196	D2 (Note 2)	10	R [100kRAD(Si)]
26	ATC18RHA95_216	1M	2.5V	MQFP-F160	D2 (Note 2)	7	R [100kRAD(Si)]
27	ATC18RHA95_324	2.2M	2.5V	MQFP-T352	D2 (Note 2)	27	R [100kRAD(Si)]
28	ATC18RHA95_324	2.2M	2.5V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]
29	ATC18RHA95_324	2.2M	2.5V	MQFP-F196	D2 (Note 2)	10	R [100kRAD(Si)]
30	ATC18RHA95_324	2.2M	2.5V	MQFP-F160	D2 (Note 2)	7	R [100kRAD(Si)]
31	ATC18RHA95_324	2.2M	2.5V	LGA-349	(Note 3)	7	R [100kRAD(Si)]
32	ATC18RHA95_404	3.5M	2.5V	MQFP-T352	D2 (Note 2)	27	R [100kRAD(Si)]
33	ATC18RHA95_404	3.5M	2.5V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]
34	ATC18RHA95_404	3.5M	2.5V	LGA-625	(Note 3)	9	R [100kRAD(Si)]
35	ATC18RHA95_404	3.5M	2.5V	AIN LGA-625	(Note 4)	29	R [100kRAD(Si)]
36	ATC18RHA95_404	3.5M	2.5V	LGA-472	(Note 3)	9	R [100kRAD(Si)]
37	ATC18RHA95_404	3.5M	2.5V	LGA-349	(Note 3)	7	R [100kRAD(Si)]
38	ATC18RHA95_504	5.5M	2.5V	MQFP-T352	D2 (Note 2)	27	R [100kRAD(Si)]
39	ATC18RHA95_504	5.5M	2.5V	MQFP-F256	D2 (Note 2)	14	R [100kRAD(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
40	ATC18RHA95_504	5.5M	2.5V	LGA-625	(Note 3)	9	R [100kRAD(Si)]
41	ATC18RHA95_504	5.5M	2.5V	AIN LGA-625	(Note 4)	29	R [100kRAD(Si)]
42	ATC18RHA95_504	5.5M	2.5V	LGA-472	(Note 3)	9	R [100kRAD(Si)]
43	ATC18RHA95_504	5.5M	2.5V	LGA-349	(Note 3)	7	R [100kRAD(Si)]
44	ATC18RHA95_544	6.5M	2.5V	LGA-625	(Note 3)	9	R [100kRAD(Si)]
45	ATC18RHA95_544	6.5M	2.5V	AIN LGA-625	(Note 4)	29	R [100kRAD(Si)]
46	ATC18RHA95_544	6.5M	2.5V	LGA-472	(Note 3)	9	R [100kRAD(Si)]
47	ATC18RHA95_324	2.2M	3.3V	MCGA-349	R (Note 2)	9	R [100 kRads(Si)]
48	ATC18RHA95_404	3.5M	3.3V	MCGA-349	R (Note 2)	9	R [100 kRads(Si)]
49	ATC18RHA95_404	3.5M	3.3V	MCGA-472	R (Note 2)	12	R [100 kRads(Si)]
50	ATC18RHA95_504	5.5M	3.3V	MCGA-349	R (Note 2)	9	R [100 kRads(Si)]
51	ATC18RHA95_504	5.5M	3.3V	MCGA-472	R (Note 2)	12	R [100 kRads(Si)]
52	ATC18RHA95_544	6.5M	3.3V	MCGA-472	R (Note 2)	12	R [100 kRads(Si)]
53	ATC18RHA95_324	2.2M	2.5V	MCGA-349	R (Note 2)	9	R [100 kRads(Si)]
54	ATC18RHA95_404	3.5M	2.5V	MCGA-349	R (Note 2)	9	R [100 kRads(Si)]
55	ATC18RHA95_404	3.5M	2.5V	MCGA-472	R (Note 2)	12	R [100 kRads(Si)]
56	ATC18RHA95_504	5.5M	2.5V	MCGA-349	R (Note 2)	9	R [100 kRads(Si)]
57	ATC18RHA95_504	5.5M	2.5V	MCGA-472	R (Note 2)	12	R [100 kRads(Si)]

Variant Number	Based on Type	Typical Equivalent NAND2 Gate Count	Interface Circuitry Supply Voltage (Note 1)	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 5)
58	ATC18RHA95_544	6.5M	2.5V	MCGA-472	R (Note 2)	12	R [100 kRads(Si)]

NOTES:

1. The component is specified for operation at a nominal interface circuitry single supply voltage V_{CC} = 3.3V or 2.5V (See Room Temperature Electrical Measurements).
2. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
3. The terminal material shall be tungsten and the finish shall be 0.03µm to 0.1µm gold plating over 3.2µm minimum nickel underplating.
4. The terminal material shall be tungsten and the finish shall be 2.5µm minimum gold plating over 3.2µm minimum nickel underplating.
5. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.4.3 Manufacturer Specific ASIC Identification

An ASIC Sheet shall be produced by the Manufacturer, after negotiation with the Orderer, that, as a minimum, specifies all the requirements unique to the specific ASIC design that are identified herein as being specified in the ASIC Sheet. The ASIC Sheet shall be held under configuration control by the Manufacturer. For identification and traceability purposes the Manufacturer shall allocate a unique Manufacturer Specific ASIC Identification to the ASIC Sheet and the specific ASIC design as specified in The ESCC Component Number herein.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.3 to 2 -0.3 to 4	V	Note 1, 2 Note 2, 3
Input Voltage	V_{IN}	-0.3 to 4	V	Note 2, 3
Input Current	I_{IN}	 ±60 ±10	mA	 Power Input Pins Signal Input Pins
Device Power Dissipation (Continuous)	P_D	See ASIC Sheet	W	
Supply Current	I_{DDop}	See ASIC Sheet	mA	
Minimum Guaranteed Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Junction Temperature	T_j	+175	^oC	
Thermal Resistance Junction to Case	$R_{th(j-c)}$	See ASIC Sheet	$^oC/W$	
Soldering Temperature MQFP case MCGA/LGA case	T_{sol}	 +300 +220	^oC	 Note 4 Note 5

NOTES:
1. Applicable to the core circuitry.
2. With reference to V_{SS} = 0V.
3. Applicable to the interface circuitry.
4. For Variants with a Multilayer Quad Flat Package case (MQFP-F160, MQFP-F196, MQFP-F256 & MQFP-T352), duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
5. For Variants with a Land Grid Array case or a Multilayer Column Grid Array case (LGA-349, LGA-472, LGA-625, AIN LGA-625, MCGA-349 & MCGA-472), during reflow.

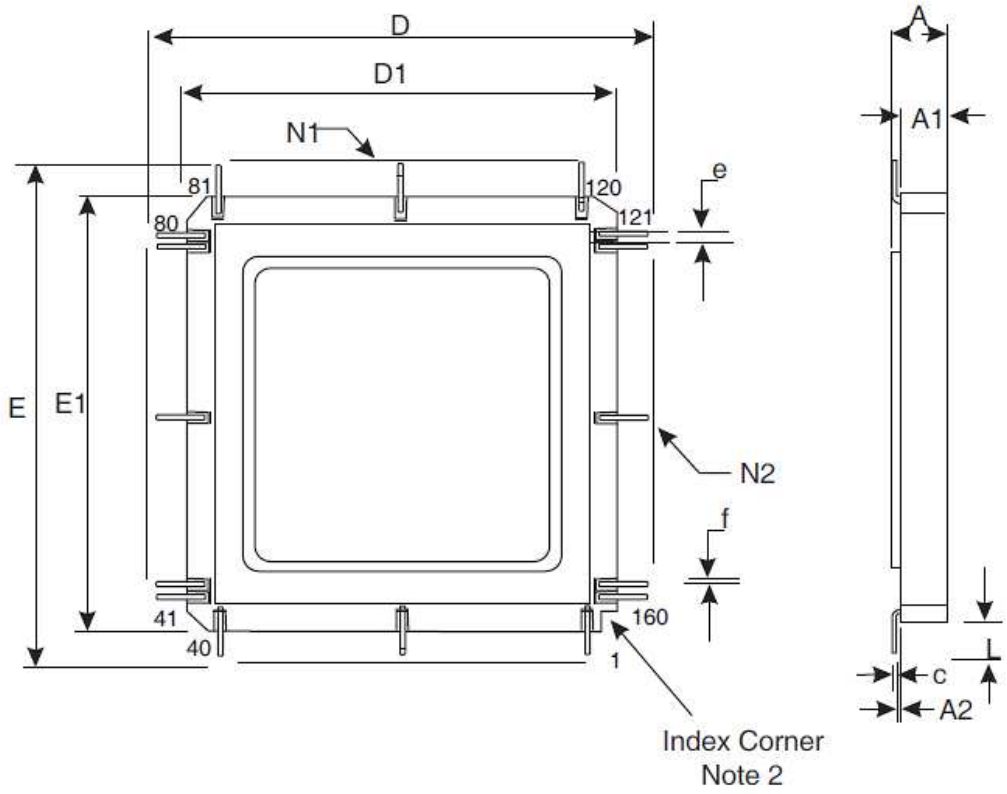
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

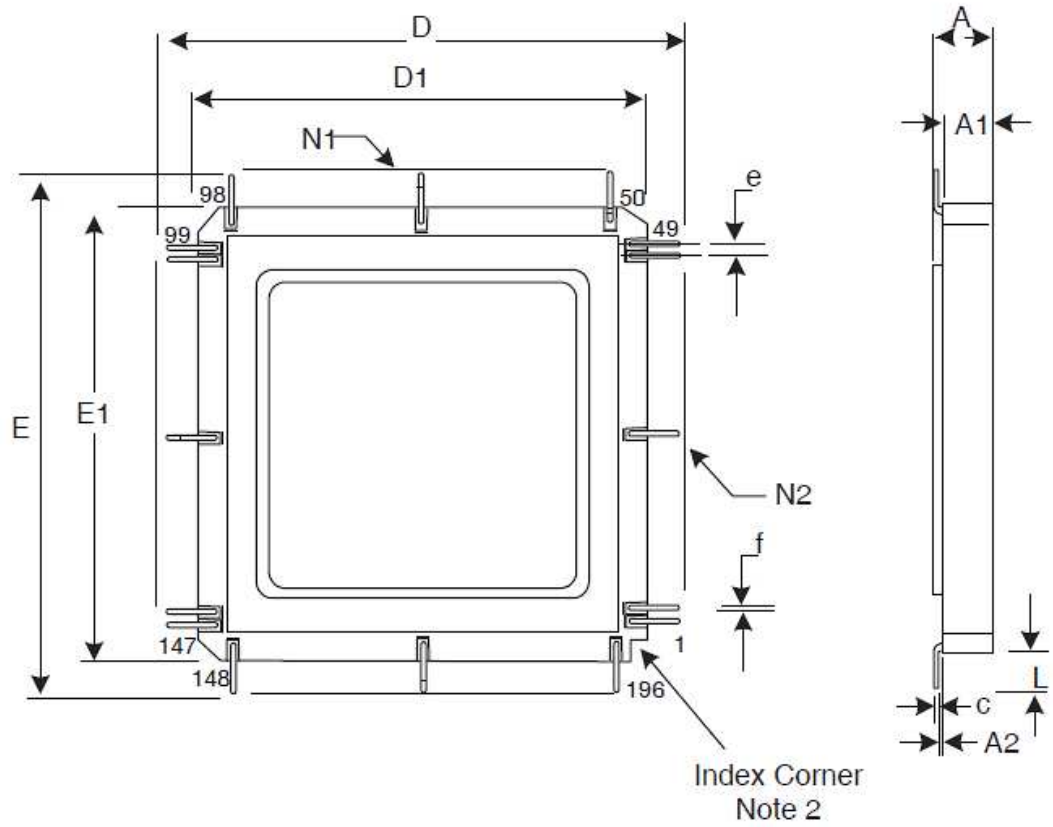
1.7.1 Multilayer Quad Flat Package (MQFP-F160) - 160 Flat Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.96	2.66	
A1	1.7	2.1	
A2	0.1	0.3	
c	0.1	0.2	1
D/E	37.9	39.3	
D1/E1	26.9	27.5	
e	0.650 BSC		1
f	0.25	0.35	1
L	5.5	5.9	1
N1/N2	40		Each side

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

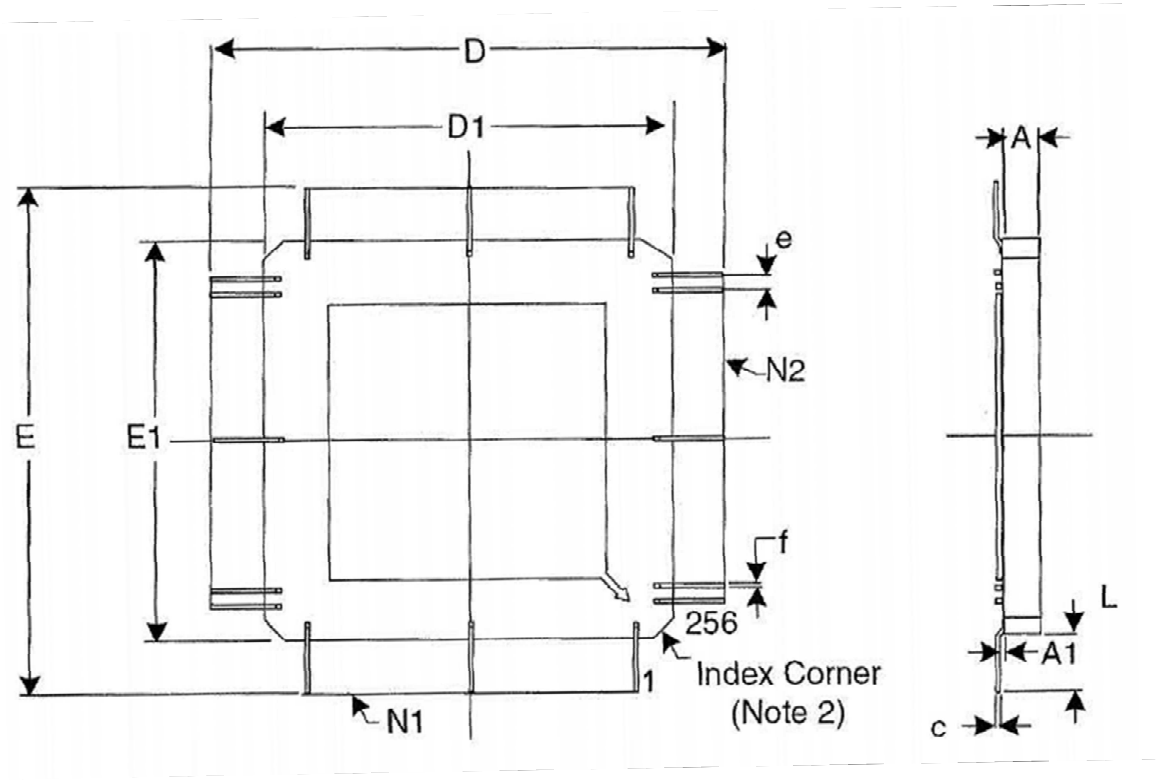
1.7.2 Multilayer Quad Flat Package (MQFP-F196) - 196 Flat Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.13	2.65	
A1	1.83	2.24	
A2	0.202	0.204	
c	0.102	0.203	1
D/E	46.73	47.94	
D1/E1	34.03	34.54	
e	0.635 BSC		1
f	0.15	0.25	1
L	6.35	6.7	1
N1/N2	49		Each side

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

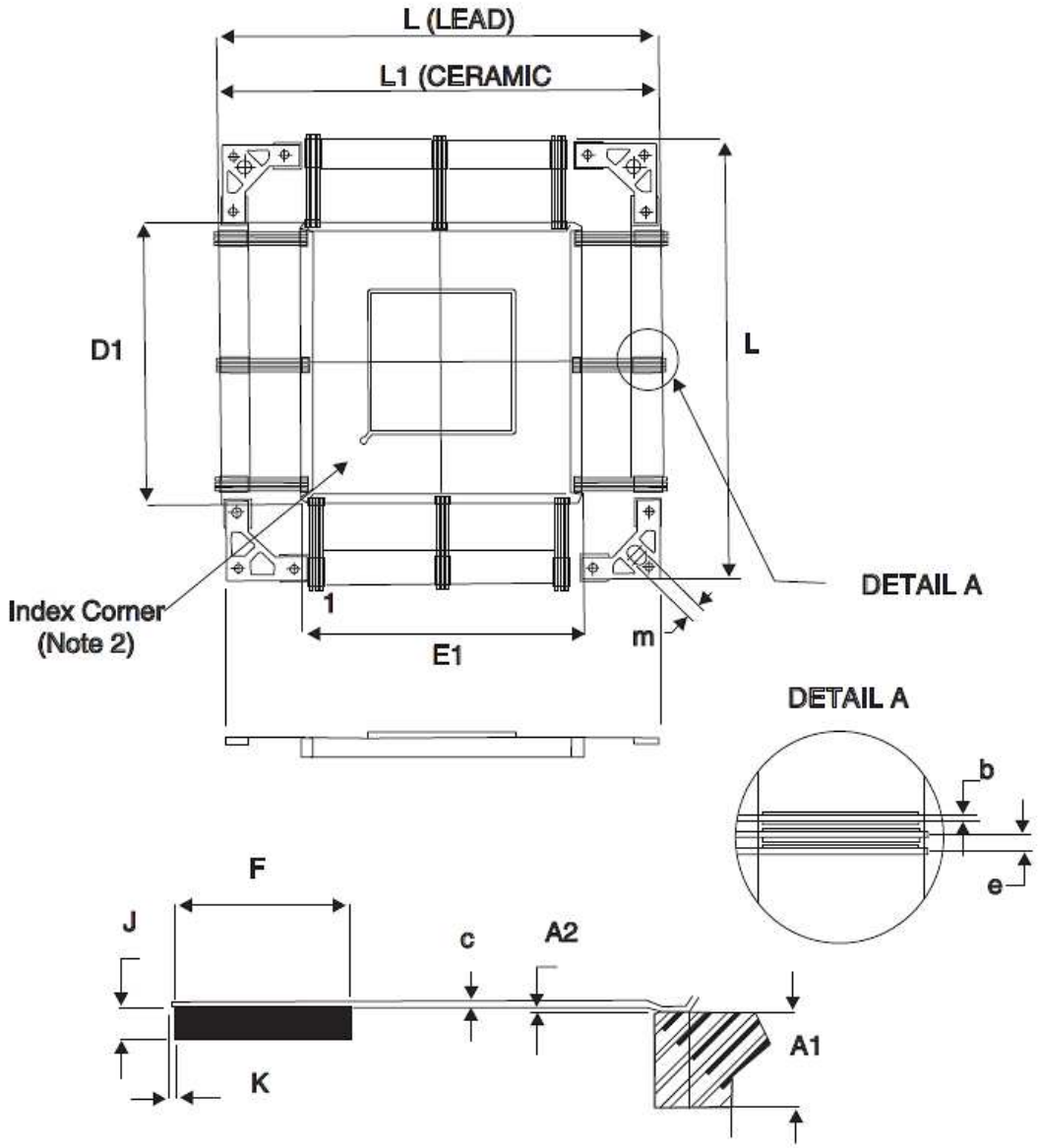
1.7.3 Multilayer Quad Flat Package (MQFP-F256) - 256 Flat Leads



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.06	2.56	
A1	0.05	0.36	
c	0.1	0.2	1
D/E	53.23	55.74	
D1/E1	36.83	37.34	
e	0.508 BSC		1
f	0.15	0.25	1
L	8.2	9.2	1
N1/N2	31.9	32.11	3

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.
3. Each side (64 leads per side); this dimension is derived from 63 x dimension e.

1.7.4 Multilayer Quad Flat Package (MQFP-T352) - 352 Tied Leads

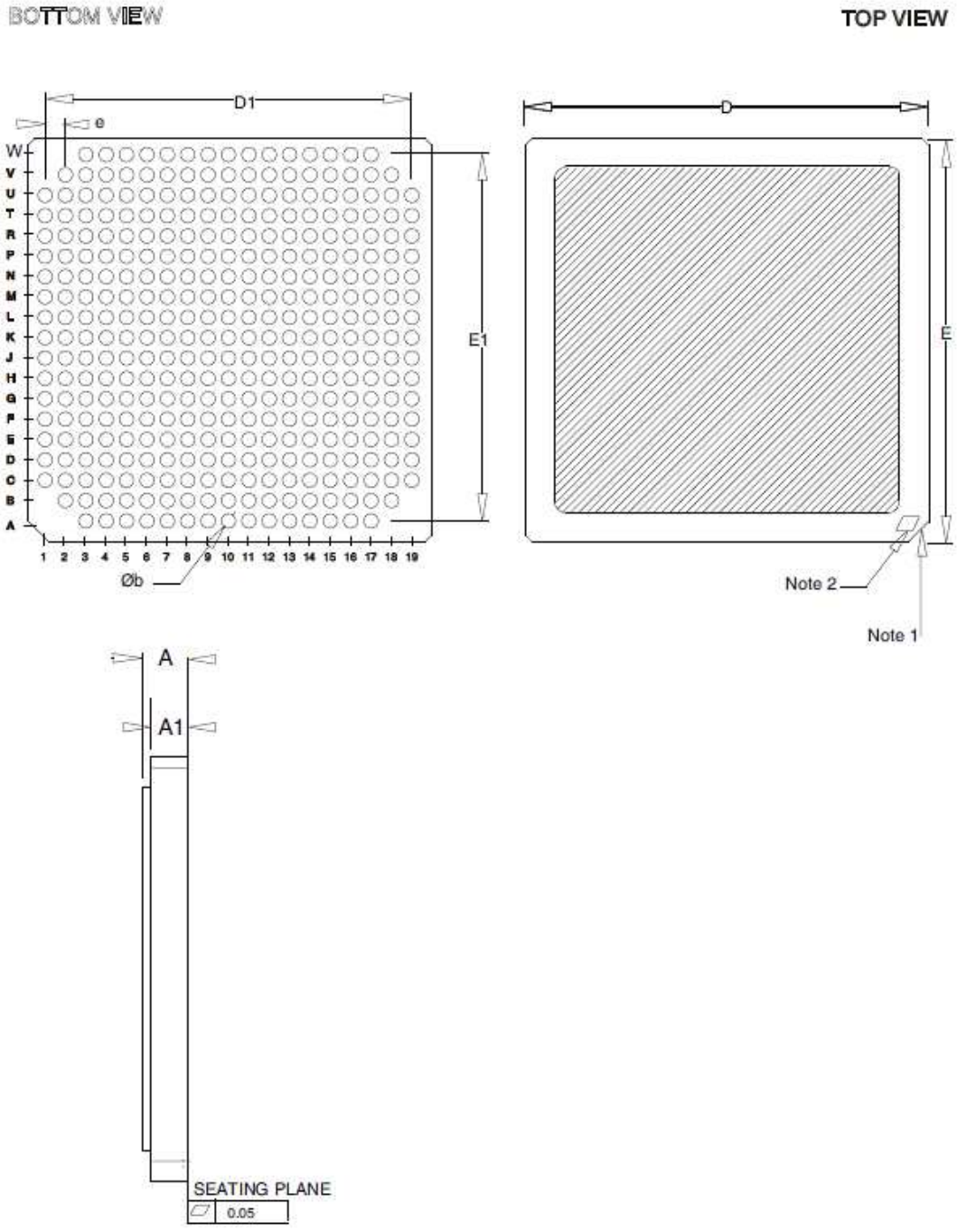


Symbols	Dimensions mm		Notes
	Min	Max	
A1	2.35	3.15	
A2	0.05	0.35	
b	0.19	0.25	1
c	0.11	0.2	1
D1/E1	47.52	48.48	
e	0.50 BSC		1
F	4.5	5.5	

Symbols	Dimensions mm		Notes
	Min	Max	
G	2.5	2.6	
J	0.75	1.05	
K	-	0.5	1
L	74.85	76.4	
L1	74.6	75.4	
m	2.5	2.65	
N1/N2	88		Each side

NOTES:
1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.5 Land Grid Array (LGA-349) - 349 Pads

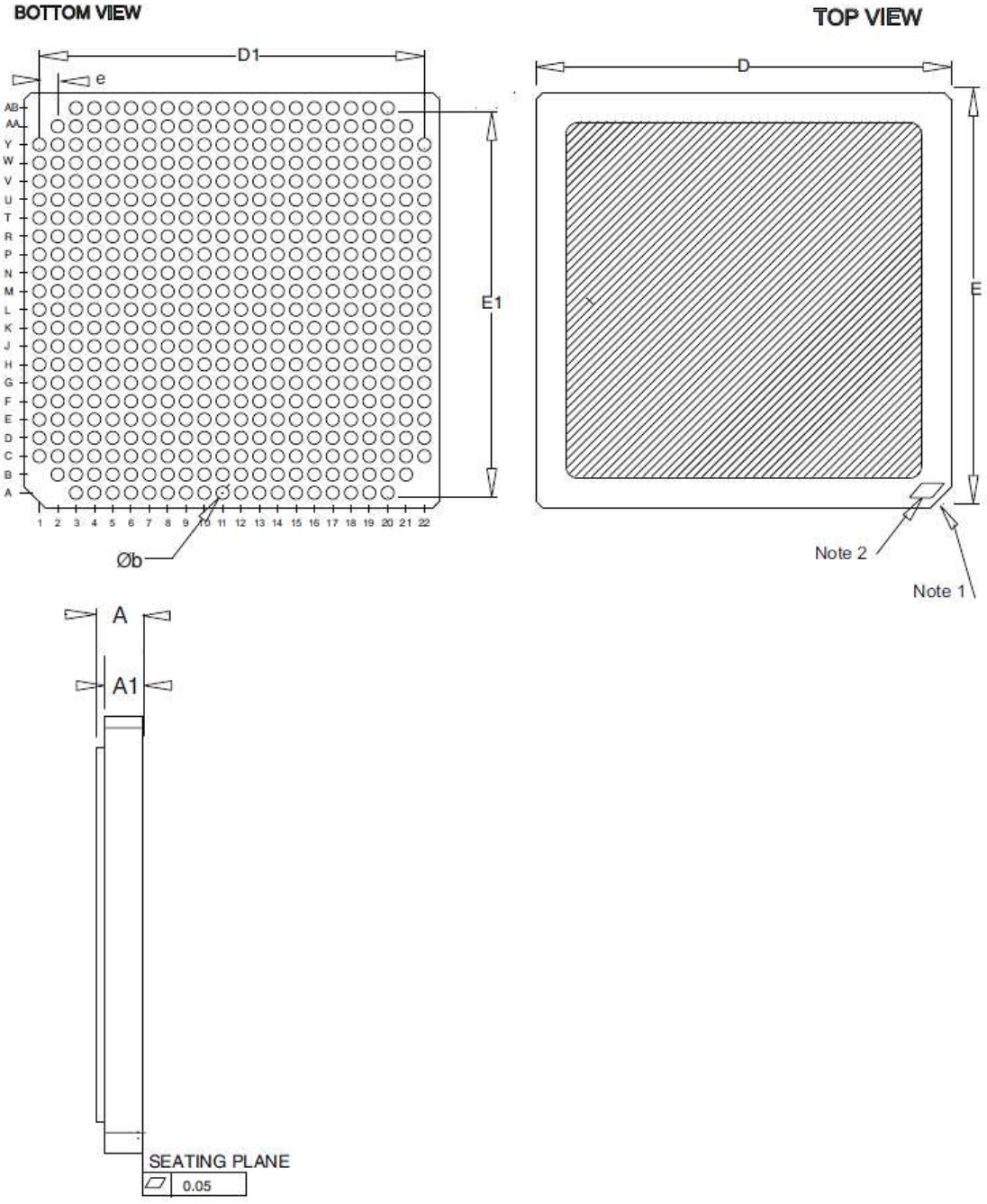


Symbols	Dimensions mm		Notes
	Min	Max	
A	-	3.24	
A1	2.27	2.77	
Øb	0.81	0.91	3
D/E	24.85	25.15	

Symbols	Dimensions mm		Notes
	Min	Max	
D1/E1	22.86 BSC		
e	1.27 BSC		3

NOTES:
1. Index corner. Terminal identification is specified by reference to the index corner as shown.
2. A terminal identification mark shall be located at the index corner as shown.
3. Applies to all pads.

1.7.6 Land Grid Array (LGA-472) - 472 Pads

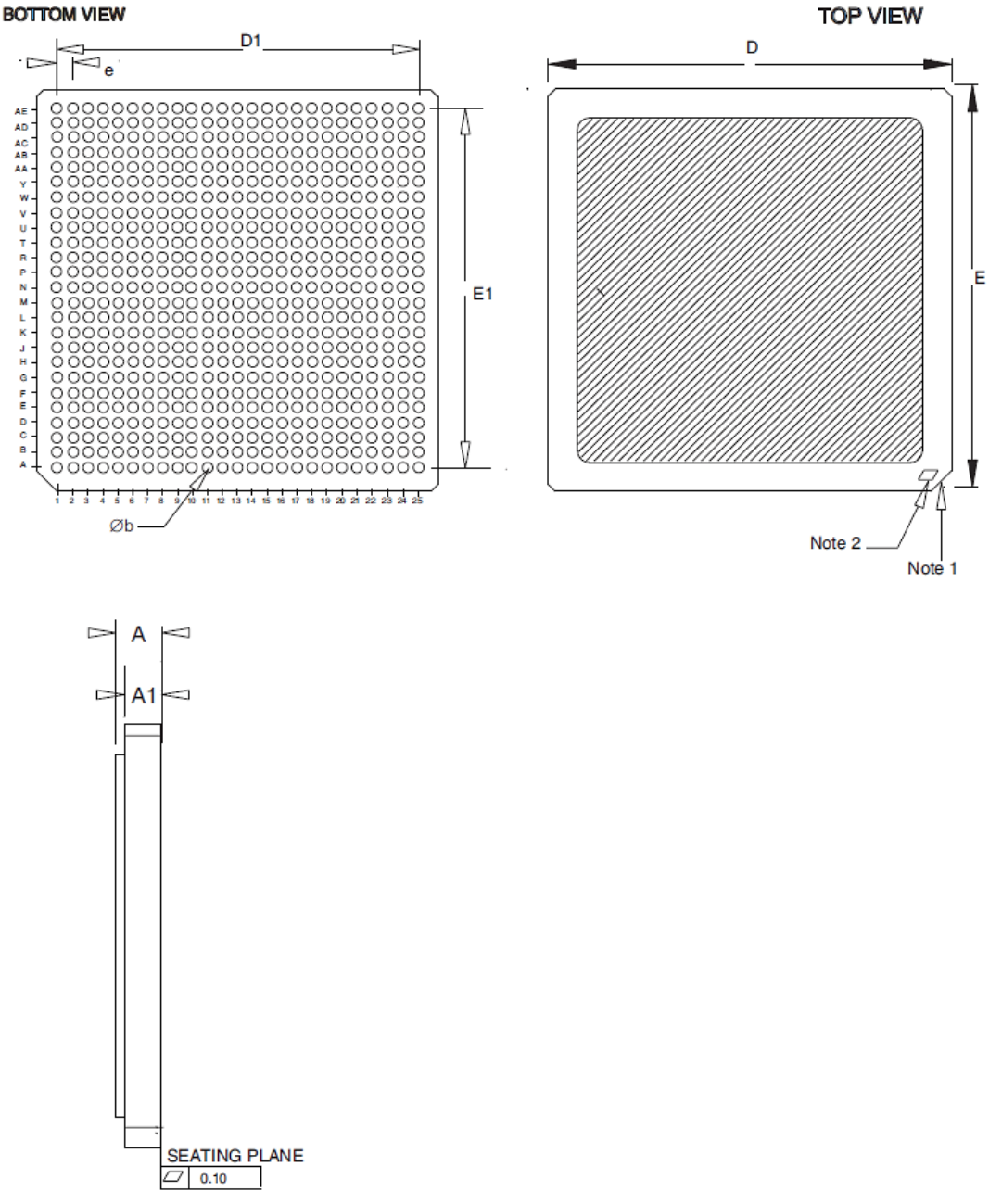


Symbols	Dimensions mm		Notes
	Min	Max	
A	-	3.24	
A1	2.27	2.77	
Øb	0.81	0.91	3
D/E	28.85	29.15	

Symbols	Dimensions mm		Notes
	Min	Max	
D1/E1	26.67 BSC		
e	1.27 BSC		3

NOTES:
1. Index corner. Terminal identification is specified by reference to the index corner as shown.
2. A terminal identification mark shall be located at the index corner as shown.
3. Applies to all pads.

1.7.7 Land Grid Array (LGA-625) - 625 Pads



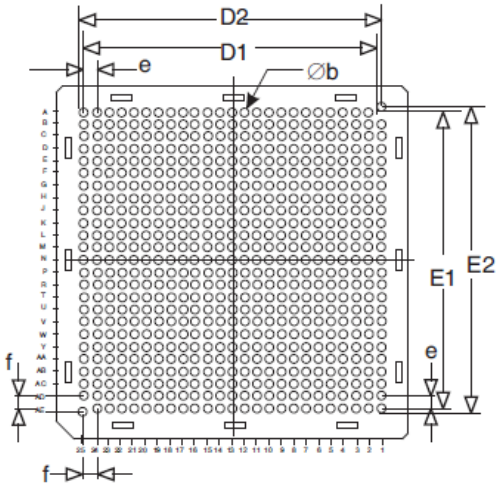
Symbols	Dimensions mm		Notes
	Min	Max	
A	-	3.24	
A1	2.27	2.77	
Øb	0.63	0.73	3
D/E	28.85	29.15	
D1/E1	24.00 BSC		
e	1.00 BSC		3

NOTES:

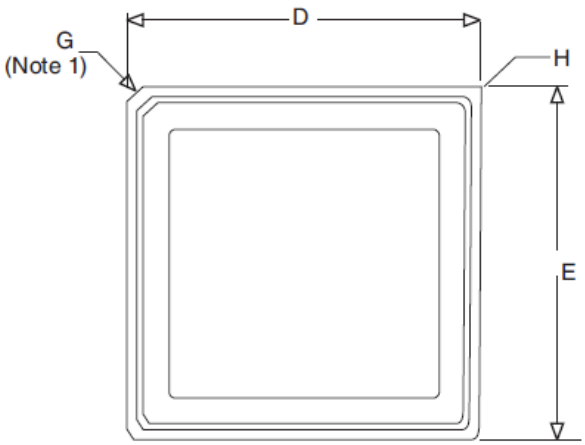
1. Index corner. Terminal identification is specified by reference to the index corner as shown.
2. A terminal identification mark shall be located at the index corner as shown.
3. Applies to all pads.

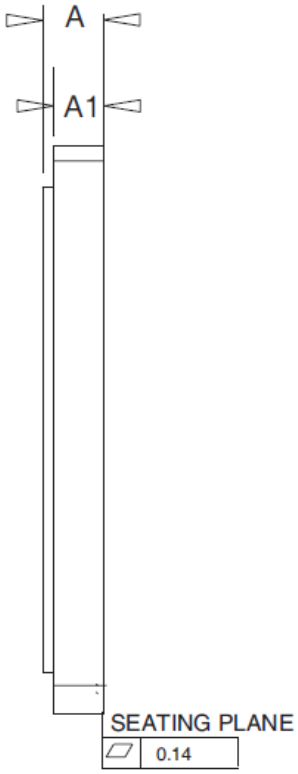
1.7.8 Land Grid Array (AIN LGA-625) - 625 Pads

BOTTOM VIEW



TOP VIEW





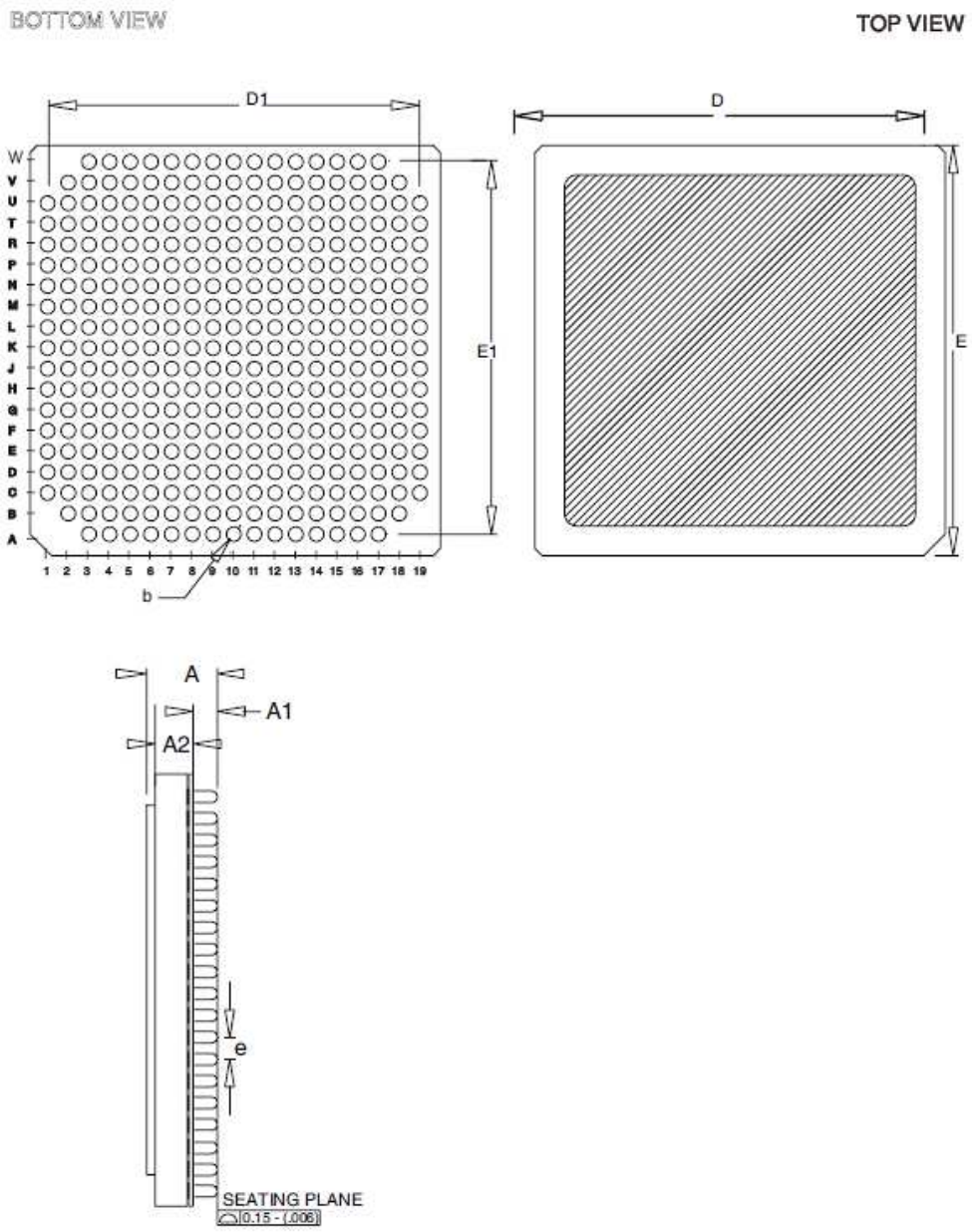
Symbols	Dimensions mm		Notes
	Min	Max	
A	-	7.05	
A1	5.4	6.6	
Øb	0.8	0.9	2
D/E	28.85	29.15	

Symbols	Dimensions mm		Notes
	Min	Max	
D1/E1	30.48 BSC		
D2/E2	31.00 BSC		3
e	1.27 BSC		4
f	1.53 BSC		3
G	1.5 x 45° chamfer		1
H	0.5 x 45° chamfer		5

NOTES:

1. Index corner. Terminal identification is specified by reference to the index corner as shown.
2. Applies to all pads.
3. Applies to pads A1 and AE25 only.
4. Applies to all pads except A1 and AE25.
5. 3 non-index corners.

1.7.9 Multilayer Column Grid Array (MCGA-349) - 349 Columns

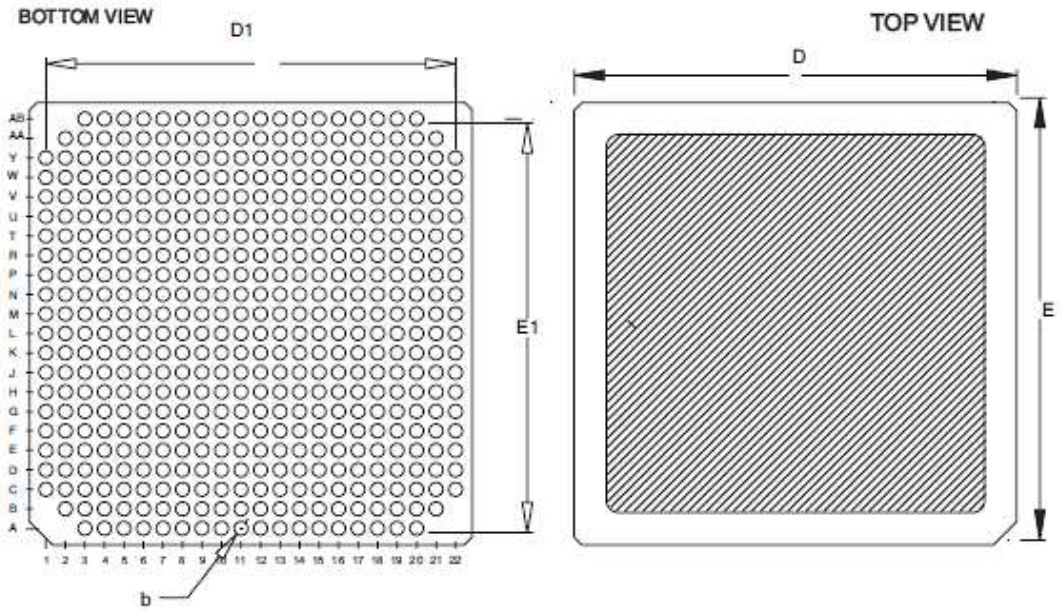


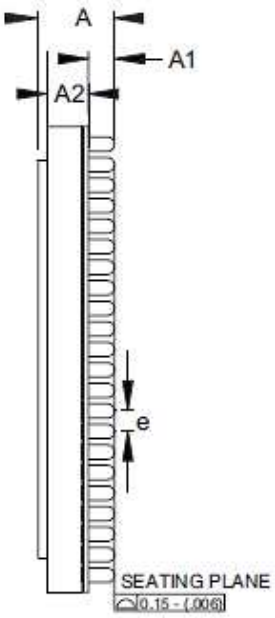
Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.4	3.45	
b	0.79	0.99	1
D/E	24.8	25.2	
D1/E1	22.86 BSC		

Symbols	Dimensions mm		Notes
	Min	Max	
e	1.27 BSC		1

NOTES:
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.10 Multilayer Column Grid Array (MCGA-472) - 472 Columns





Symbols	Dimensions mm		Notes
	Min	Max	
A	4.3	5.9	
A1	1.4	1.85	
A2	2.6	3.45	
b	0.79	0.99	1
D/E	28.77	29.23	
D1/E1	26.67 BSC		
e	1.27 BSC		1

NOTES:
1. Applies to all columns.
2. Terminal identification is specified by reference to the index corner as shown.

1.8 FUNCTIONAL DIAGRAM

See ASIC Sheet.

NOTES:
1. For all packages the lid is internally connected to the ground terminal as specified in the ASIC Sheet.

1.9 PIN ASSIGNMENT

See ASIC Sheet.

1.10 INSTRUCTION SET AND TIMING DIAGRAMS

See ASIC Sheet.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

As a minimum the information to be marked on the component shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number.
(c) Traceability information.

The complete marking shall be as specified in the ASIC Sheet.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3 ºC.

2.3.1.1 Room Temperature Electrical Measurements for Components Specified at Supply Voltage V_{CC} = 3.3V (Variants 01 to 23)

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \leq V_{DD} \leq 1.95V$ $3V \leq V_{CC} \leq 3.6V$	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet V_{CC} = 3V	-	-	-
Functional Test 2	-	3014	See ASIC Sheet V_{CC} = 3.3V	-	-	-
Functional Test 3	-	3014	See ASIC Sheet V_{CC} = 3.6V	-	-	-
Supply Current, Stand-by	I_{CCSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{CCOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	$V_{IN} = V_{SS}$, CMOS Buffers	-1	1	µA
Low Level Input Current with Pull-up	I_{ILPU}	3009	$V_{IN} = V_{SS}$, CMOS Buffers	-400	-	µA
Low Level Input Current with Pull-down	I_{ILPD}	3009	$V_{IN} = V_{SS}$, CMOS Buffers	-5	5	µA
High Level Input Current	I_{IH}	3010	$V_{IN} = V_{CC}$, CMOS Buffers	-1	1	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \le V_{DD} \le 1.95V$ $3V \le V_{CC} \le 3.6V$	Limits		Units
				Min	Max	
High Level Input Current with Pull-up	I_{IHPU}	3010	$V_{IN} = V_{CC}$, CMOS Buffers	-5	5	µA
High Level Input Current with Pull-down	I_{IHPD}	3010	$V_{IN} = V_{CC}$, CMOS Buffers	-	600	µA
Low Level Input Voltage	V_{IL}	-	V_{CC} = 3V, CMOS Buffers PCI Buffers	 - -	 0.8 $0.3*V_{CC}$	V
High Level Input Voltage	V_{IH}	-	V_{CC} = 3.6V, CMOS Buffers PCI Buffers	 2 $0.5*V_{CC}$	 - -	V
Low Level Output Voltage	V_{OL}	3007	V_{CC} = 3V, I_{OL} = 2, 4, 8, 12, 16mA	-	0.4	V
High Level Output Voltage	V_{OH}	3006	V_{CC} = 3V, I_{OH} = -2, -4, -6, -8, -10mA	V_{CC}-0.4	-	V
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT} = V_{SS}$	-1	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT} = 3.6V	-1	1	µA
Input Leakage Current, Cold Sparing	I_{ICS}	-	V_{IN} = 0 to V_{CC}	-1	1	µA
Output Leakage Current, Cold Sparing	I_{OCS}	-	V_{OUT} = 0 to V_{CC}	-1	1	µA
Output Short Circuit Current, to V_{CC}	I_{OSN}	-	nn = 1 $V_{OUT} = V_{CC}$ Notes 2, 3	-	23	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	nn = 1 $V_{OUT} = V_{SS}$ Notes 2, 3	-	23	mA
High Level Output Current	I_{OH}	-	PCI Buffers $V_{OH} = V_{CC}$-0.4V	16	-	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \le V_{DD} \le 1.95V$ $3V \le V_{CC} \le 3.6V$	Limits		Units
				Min	Max	
Low Level Output Current	I_{OL}	-	PCI Buffers $V_{OL} = 0.4V$	16	-	mA
Differential Output Voltage	V_{OD}	-	LVDS Transmitter buffers	247	454	mV
Common Mode Output Voltage	V_{OS}	-	LVDS Transmitter buffers	1125	1375	mV
Input Capacitance	C_{IN}	3012	Note 3	-	7	pF
Timings	-	3003	See ASIC Sheet			ns

2.3.1.2 Room Temperature Electrical Measurements for Components Specified at Supply Voltage V_{CC} = 2.5V (Variants 24 to 46)

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \le V_{DD} \le 1.95V$ $2.3V \le V_{CC} \le 2.7V$	Limits		Units
				Min	Max	
Functional Test 1	-	3014	See ASIC Sheet $V_{CC} = 2.3V$	-	-	-
Functional Test 2	-	3014	See ASIC Sheet $V_{CC} = 2.5V$	-	-	-
Functional Test 3	-	3014	See ASIC Sheet $V_{CC} = 2.7V$	-	-	-
Supply Current, Stand-by	I_{CCSB}	3005	See ASIC Sheet			mA
Supply Current, Operating	I_{CCOP}	3005	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	3009	$V_{IN} = V_{SS}$, CMOS Buffers	-1	1	µA
Low Level Input Current with Pull-up	I_{ILPU}	3009	$V_{IN} = V_{SS}$, CMOS Buffers	-260	-	µA
Low Level Input Current with Pull-down	I_{ILPD}	3009	$V_{IN} = V_{SS}$, CMOS Buffers	-5	5	µA
High Level Input Current	I_{IH}	3010	$V_{IN} = V_{CC}$, CMOS Buffers	-1	1	µA
High Level Input Current with Pull-up	I_{IHPU}	3010	$V_{IN} = V_{CC}$, CMOS Buffers	-5	5	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1 $1.65V \leq V_{DD} \leq 1.95V$ $2.3V \leq V_{CC} \leq 2.7V$	Limits		Units
				Min	Max	
High Level Input Current with Pull-down	I_{IHPD}	3010	$V_{IN} = V_{CC}$, CMOS Buffers	-	360	µA
Low Level Input Voltage	V_{IL}	-	V_{CC} = 2.3V, CMOS Buffers	-	0.7	V
High Level Input Voltage	V_{IH}	-	V_{CC} = 2.7V, CMOS Buffers	2	-	V
Low Level Output Voltage	V_{OL}	3007	V_{CC} = 2.3V, I_{OL} = 1.5, 3, 6, 9, 12mA	-	0.4	V
High Level Output Voltage	V_{OH}	3006	V_{CC} = 2.3V, I_{OH} = -1.5, -3, -6, -9, -12mA	V_{CC}-0.4	-	V
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{OUT} = V_{SS}$	-1	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{OUT} = 2.7V	-1	1	µA
Input Leakage Current, Cold Sparing	I_{ICS}	-	V_{IN} = 0 to V_{CC}	-1	1	µA
Output Leakage Current, Cold Sparing	I_{OCS}	-	V_{OUT} = 0 to V_{CC}	-1	1	µA
Output Short Circuit Current, to V_{CC}	I_{OSN}	-	nn = 1 $V_{OUT} = V_{CC}$ Notes 3, 4	-	14	mA
Output Short Circuit Current, to V_{SS}	I_{OSP}	-	nn = 1 $V_{OUT} = V_{SS}$ Notes 3, 4	-	14	mA
Differential Output Voltage	V_{OD}	-	LVDS Transmitter buffers	247	454	mV
Common Mode Output Voltage	V_{OS}	-	LVDS Transmitter buffers	1125	1375	mV
Input Capacitance	C_{IN}	3012	Note 3	-	7	pF
Timings	-	3003	See ASIC Sheet			ns

2.3.2 Notes to Electrical Measurements Tables

1. Unless otherwise specified: all inputs and outputs shall be tested for each characteristic; Inputs not under test shall be V_{IN} = V_{SS}, V_{CC} or V_{DD} and outputs not under test shall be open; V_{SS} = 0V.
2. I_{OS} max = 23, 46, 92, 138, 184mA for nn = 1, 2, 4, 6, 8 respectively
3. Tested at initial design and after major process changes, otherwise guaranteed.
4. I_{OS} max = 14, 28, 56, 84, 112mA for nn = 1, 2, 4, 6, 8 respectively

2.3.3 High and Low Temperatures Electrical Measurements

Unless otherwise specified the measurements shall be performed at T_{amb} = +125 (+0 -5) ºC and T_{amb} = -55 (+5 -0) ºC. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 ºC.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Supply Current, Stand-by	I_{DDSB}	See ASIC Sheet			mA
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}	±0.1	-	1	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.1	-	-1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.1	-	1	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.6	-	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 ºC. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS
See ASIC Sheet.

2.7 OPERATING LIFE CONDITIONS
Unless otherwise specified the conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing
Continuous bias shall be applied during irradiation testing as specified in the ASIC Sheet.

The total dose level applied shall be as specified in the component type variant information herein, in the ASIC Sheet or in the Purchase Order.

2.8.2 Electrical Measurements for Total Dose Radiation Testing
Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ±3 ºC.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are specified in the ASIC Sheet.