MONOLITHIC MICROWAVE

INTEGRATED CIRCUITS (MMICs)

ESCC Generic Specification No. 9010

Issue 3	October 2014

Document Custodian: European Space Agency – see https://escies.org

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DCR No.	CHANGE DESCRIPTION
847	Specification upissued to incorporate technical changes per DCR.

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1 INTRODUCTION

1.1 SCOPE

This specification defines the general requirements for the qualification approval, capability approval, procurement, including lot acceptance testing, and delivery of Monolithic Microwave Integrated Circuit (MMIC) components or naked dice for space applications.

This specification contains the appropriate inspection and test schedules and also specifies the data documentation requirements.

1.2 APPLICABILITY

This specification is primarily applicable to the granting of qualification approval or capability approval to a component or naked dice in accordance with ESCC Basic Specification No. 20100 or 24300 and the procurement of such components or naked dice from qualified Manufacturers.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect on the date of placing the purchase order.

2.1 ESCC SPECIFICATIONS

- No. 20100, Requirements for the Qualification of Standard Electronic Components for Space Application.
- No. 20400, Internal Visual Inspection.
- No. 20500, External Visual Inspection.
- No. 20600, Preservation, Packaging and Despatch of ESCC Electronic Components.
- No. 20900, Radiographic Inspection.
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 21400, Scanning Electron Microscope Inspection of Semiconductor Dice.
- No. 21700, General Requirements for the Marking of ESCC Components.
- No. 22800, ESCC Non-conformance Control System.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23500, Lead Materials and Finishes for Components tor Space Application.
- No. 24300, Requirements for the Capability Approval of Electronic Component Technologies for Space Application.
- No. 24600, Minimum Quality System Requirements.
- No. 24800, Resistance to Solvents of Marking, Materials and Finishes.

With the exception of ESCC Basic Specifications Nos. 20100, 21700, 22800, 24300 and 24600, where Manufacturers' specifications are equivalent to, or more stringent than, the ESCC Basic Specifications listed above, they may be used in place of the latter, subject to the approval of the ESCC Executive.

Such replacements shall be clearly identified in the applicable Process Identification Document (PID) and listed in an appendix to the appropriate Detail Specification.

Unless otherwise stated herein, references within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

- ESA PSS-01-702, A Thermal Vacuum Test tor the Screening of Space Materials.
- MIL-STD-883, Test Methods and Procedures tor Micro-electronics.
- IEC Publication No. 410, Sampling Plans and Procedures tor Inspection by Attributes.
- TCV and DEC Test Document (Detail Specification format).

2.3 ORDER OF PRECEDENCE

For the purpose of interpretation and in case of conflict with regard to documentation, the following order of precedence shall apply:

(a) ESCC Detail Specification.
(b) ESCC Generic Specification.
(c) ESCC Basic Specification.
(d) Other documents, it referenced herein.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following definitions shall apply:

- Component: Items which are to be delivered after encapsulation
- Naked dice: Items which are to be delivered without encapsulation
- TCV: Technology characterisation vehicle
- DEC: Dynamic evaluation circuit.
- Wafer Lot: A batch of wafers which is limited to the capacity of the metallisation deposition equipment and to which a unique identification has been allocated from the commencement of processing.

4 REQUIREMENTS

4.1 GENERAL

The test requirements tor the component type qualification approval of a component shall comprise wafer lot acceptance (see Para. 5.2), final production tests (see Chart II(b)), burn-in and electrical measurements to testing level 'B' (see Chart III(b)) and qualification testing (see Chart IV).

The requirements for approval of a capability domain and the qualification of a component (type approval testing) within an approved domain are given in ESCC Basic Specification No. 24300.

The test requirements for procurement of components shall comprise wafer lot acceptance (see Para. 5.2) with radiation tests (see Para. 5.2.3) if specified by the Orderer, final production tests (see Chart II(b)), burn-in and electrical measurements to testing level 'B' or 'C' as required (see Chart III(b)) together with, when applicable, a level of lot acceptance testing (see Chart V) to be specified by the Orderer.

The test requirements for procurement of naked dice released within an approved domain and already submitted to Type Approval shall be limited to wafer lot acceptance (see Para. 5.2), wafer screening (see Chart II(a)) and wafer acceptance testing (see Chart III(a)).

The test requirements for procurement of naked dice of a qualified component type shall comprise wafer lot acceptance (see Para. 5.2) and wafer screening (see Chart II(a)); additionally a sample of 15 components shall be submitted to final production tests (see Chart II(b)), burn-in and electrical measurements (see Chart III(b)) and lot acceptance level 2 testing (see Chart V).

Chart I(b) summarises the requirements for procurement of both components and naked dice.

If a Manufacturer elects to eliminate a final production test by substituting an in-process control or statistical process control procedure, the Manufacturer is still responsible for delivering components or naked dice that meet all of the performance, quality and reliability requirements defined in this specification and the Detail Specification.

4.1.1 Specifications

For qualification or capability approval, procurement (including lot acceptance testing) and delivery of components or naked dice in conformity with this specification, the applicable specifications listed in Section 2 of this document shall apply in total unless otherwise specified herein or in the Detail Specification.

4.1.2 Conditions and Methods of Test

The conditions and methods of test shall be in accordance with this specification, the ESCC Basic Specifications referenced herein and the Detail Specification.

4.1.3 Manufacturer's Responsibility for Performance of Tests and Inspections

The Manufacturer shall be responsible for the performance of tests and inspections required by the applicable specifications. These tests and inspections shall be performed at the plant of the Manufacturer of the components or naked dice unless it is agreed by the ESCC Executive prior to commencing qualification testing, or procurement, to use an approved external facility.

4.1.4 Inspection Rights

The ESCC Executive (for qualification or capability approval or for a procurement) reserves the right to monitor any of the tests and inspections scheduled in the applicable specifications.

4.1.5 Pre-encapsulation Inspection

The Manufacturer shall notify the Orderer at least 2 working weeks before the commencement of pre-encapsulation inspection.

The Orderer shall indicate immediately whether or not he intends to witness the inspection.

4.2 QUALIFICATION APPROVAL REQUIREMENTS ON A MANUFACTURER

To obtain and maintain the component type qualification approval of a component, or family of components, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 20100.

To obtain and maintain the approval of a capability domain, and the qualification of a component in an approved domain, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 24300.

4.3 DELIVERABLE COMPONENTS AND NAKED DICE

Components and naked dice delivered to this specification shall be processed and inspected in accordance with the relevant Process Identification Document (PID). Each delivered component and naked dice shall be traceable to its production lot. Components and naked dice delivered to this specification shall have completed satisfactorily all tests to the testing level and lot acceptance level specified in the purchase order (see Para. 4.3.2).

ESCC qualified components and naked dice delivered to this specification shall be produced from lots that are capable of passing all tests, and sequences of tests, that are defined in Charts IV and V. The Manufacturer shall not knowingly supply components or naked dice that cannot meet this requirement. In the event that, subsequent to delivery and prior to operational use, a component or naked dice is found to be in a condition such that it could not have passed these tests at the time of manufacture, this shall be grounds for rejection of the delivered lot.

Components and naked dice failing inspections and tests of the higher testing level (i.e. level 'B') shall not be supplied against any order for components or naked dice of the lower testing level.

Components or naked dice produced from lots where samples have failed the specified level of radiation testing shall not be delivered against orders requiring a lower level of radiation testing unless data is available to demonstrate that the samples passed that lower level. Should such data not be available, components or naked dice shall not be delivered against orders requiring a lower level of radiation testing unless a sample is first retested to that lower level.

4.3.1 Lot Failure

Lot failure may occur during wafer screening (Chart II(a)), wafer acceptance testing (Chart III(a)), final production tests (Chart II(b)), burn-in and electrical measurements (Chart III(b)), qualification testing (Chart IV), capability approval testing (ESCC Basic Specification No. 24300) or lot acceptance testing (Chart V).

Should such failure occur, the non-conformance procedure shall be initiated in accordance with ESCC Basic Specification No. 22800.

Should such failure occur during procurement, the Manufacturer shall notify the Orderer by telex within 2 working days, giving details of the number and mode of failure and the suspected cause.

In the case where qualification or capability approval has been granted to the component or naked dice, he shall, at the same time by the same means, inform the ESCC Executive in order that the latter may consider its implications.

No further testing shall be performed on the failed components or naked dice except on instruction from the Orderer. The Orderer shall inform the Manufacturer and the ESCC Executive within 2 working days of receipt of the telex, by the same means, what action shall be taken.

In the case when lot failure occurs during qualification or capability approval testing, the Manufacturer shall immediately notify the ESCC Executive who will define a course of action to be followed. No further testing shall be performed on the failed components.

4.3.2 Testing and Lot Acceptance Levels

This specification defines six levels of radiation testing (see ESCC Basic Specification No. 22900), 2 levels of testing severity which are designated by the letters 'B' and 'C' (see Chart I(a)) and 3 levels of lot acceptance testing (see Chart V).

The lot acceptance levels are designated 1, 2 and 3, and are comprised of tests as follows:

- Level 3 (LA3) - Electrical Subgroup
- Level 2 (LA2) - Endurance Subgroup
  plus Electrical Subgroup
- Level 1 (LA1) - Environmental and Mechanical Subgroup
  plus Endurance Subgroup
  plus Electrical Subgroup

The required level of radiation testing, testing level and lot acceptance level shall be specified in the purchase order.

4.4 MARKING

All components and naked dice procured and delivered to this specification from a source qualified according to ESCC Basic Specification No. 20100 or No. 24300 shall be marked in accordance with ESCC Basic Specification No. 21700. Thus, they shall bear the ESA symbol to signify their conformance to the ESCC qualification approval requirements and full compliance with the requirements of this specification and the Detail Specification.

Components and naked dice procured from sources which are not ESCC qualified, provided that they fully comply with the procurement requirements of this specification and the Detail Specification, may bear the ESCC marking **with the exception of the ESA symbol**.

4.5 MATERIALS AND FINISHES

All non-metallic materials and finishes, that are not within a hermetically sealed enclosure, of the components and naked dice specified herein shall meet the outgassing requirements as outlined in ESA PSS-01-702.

Specific requirements for materials and finishes are specified in the Detail Specification.

5 PRODUCTION CONTROL

5.1 GENERAL

The minimum requirements for production control, which are equally applicable to procurement, are defined in the Process Identification Document (PID).

5.2 WAFER LOT ACCEPTANCE

5.2.1 Process Monitoring Review

For all wafers, a review of the statistical process control (SPC) data shall be performed against the statistical limits and sigmas specified in the PID.

5.2.1.1 Process Control Failure

A wafer shall be rejected if one or more process control data parameters exceed the allowed distribution as specified in the PID.

5.2.2 Scanning Electron Microscope (SEM) Inspection

Components and naked dice supplied to this specification shall be produced from the wafer lots that have been subjected to, and successfully met, the scanning electron microscope inspection requirements in accordance with ESCC Basic Specification No. 21400.

5.2.3 Total Dose Radiation Testing

During qualification and maintenance of qualification:

– If specified in the Detail Specification, components and naked dice shall be produced from a wafer lot which has been subjected to and successfully met the radiation requirements contained in ESCC Basic Specification No. 22900.

During procurement:

– When required by the purchase order, components and naked dice shall be produced from a wafer lot which has been subjected to and successfully met the radiation requirements contained in ESCC Basic Specification No. 22900.

5.2.4 Documentation

Documentation of wafer lot acceptance shall be in accordance with the requirements of Para. 10.5 of this specification and shall only be supplied if specified in the purchase order.

5.3 WAFER SCREENING (CHART II(a))

5.3.1 General

All dice to be used for qualification, approval of a capability domain or for delivery shall be subjected to the wafer screening tests specified in Chart II(a) of this specification.

Unless otherwise specified in the Detail Specification, the tests shall be performed in the order shown.

5.3.2 Test Methods and Conditions

The applicable test methods and conditions are specified in the paragraphs referenced in Chart II(a) of this specification.

5.3.3 Acceptance Criteria

A wafer shall be counted as a limit failure if one or more parameters on any of the 5 sample dice probed exceeds the limits specified in Table 3 of the Detail Specification.

If a failure occurs, further measurements shall be performed to General Inspection Level I, AQL 1.0 of IEC Publication No. 410 on the remaining dice of the wafer containing the failed die. If a further failure occurs, the wafer shall be rejected.

5.3.4 Rebonding

The rebonding of wires during assembly is not permitted.

5.3.5 Documentation

Documentation shall be supplied as specified in Para. 10.6 of this specification.

5.4 WAFER ACCEPTANCE TESTING (CHART III(a))

5.4.1 General

All naked dice for delivery from an approved Capability Domain shall be subjected to wafer acceptance testing in accordance with Chart III(a).

For capability approval testing, wafer acceptance testing shall be performed prior to component final production tests.

Unless otherwise specified in the Detail Specification, the tests shall be performed in the order shown.

5.4.2 Lot Sample Selection for Wafer Acceptance Testing

A minimum of 3 TCVs per wafer with a minimum of 12 TCVs per wafer lot shall be randomly selected.

As an addition, 3 DECs per wafer with a minimum of 12 DECs per wafer lot may be randomly selected if it considered necessary to verify the stability of RF performance.

5.4.3 Test Methods and Conditions

The applicable test methods and conditions are specified in the paragraphs referenced in Chart II(a) of this specification.

5.4.4 Acceptance Criteria

5.4.4.1 Parameter Drift Failure

The acceptable delta limits are shown in the Table 4 of the TCV and DEC Test Document. Wafer acceptance testing shall be considered as failed and wafer(s) rejected if the changes during TCV and DEC burn-in tests are greater than the delta values specified.

5.4.4.2 Parameter Limit Failure

A TCV or DEC shall be counted as a limit failure if one or more parameters exceed the limits shown in Tables 2 or 3 of the TCV and DEC Test Document.

Any TCV or DEC which exhibits a limit failure prior to the burn-in sequence shall be rejected and replaced.

5.4.4.3 Other Failures

A TCV or DEC shall be counted as a failure in any of the following cases:

- Mechanical failure.
- Handling failure.
- Lost TCV or DEC.

5.4.5 Failed Wafers and Wafer Release

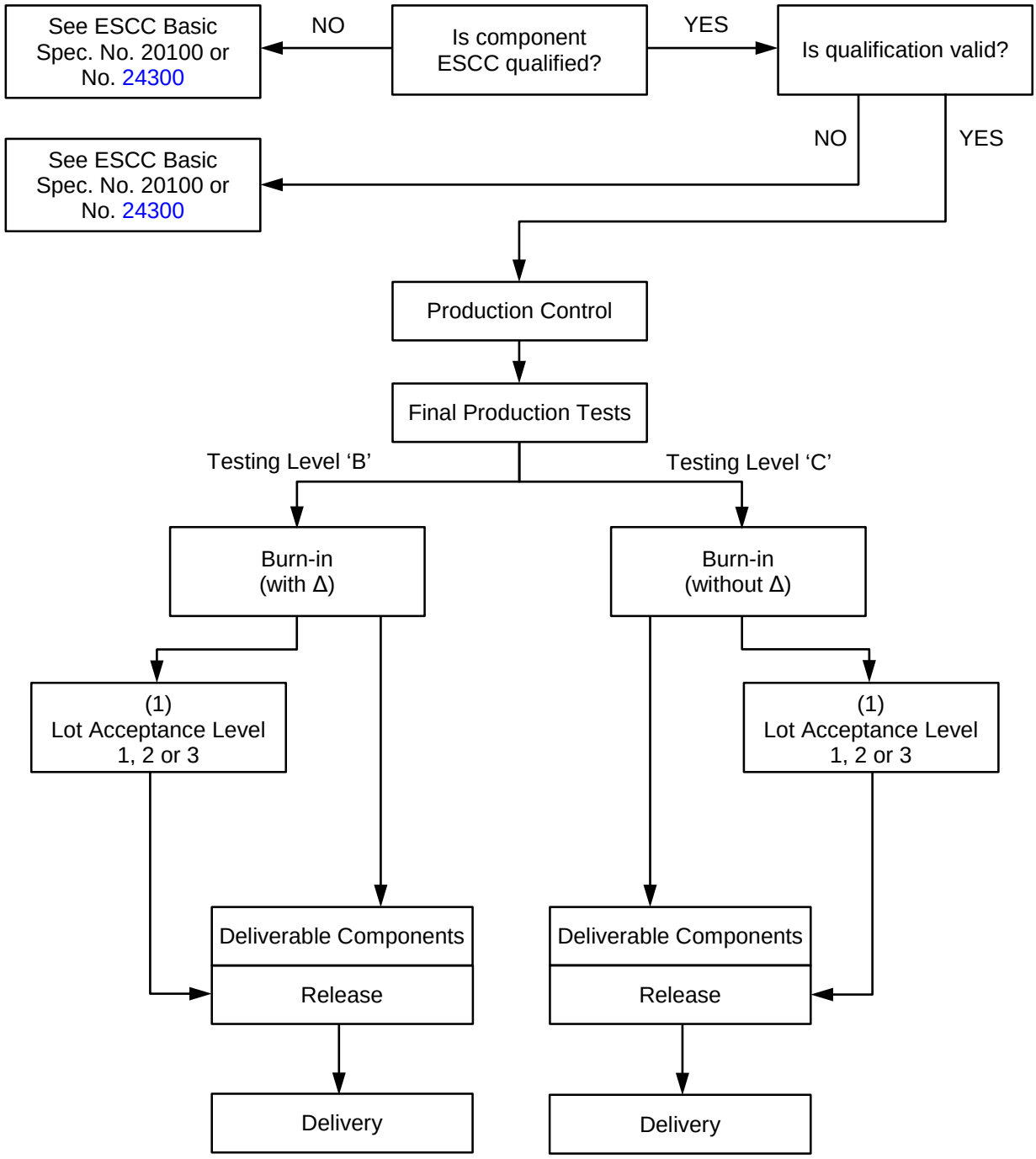
Wafer acceptance testing shall be considered as failed and wafer(s) rejected if one or more of the failure modes described in Para. 5.4.4 of this specification is observed.

All unmarked dice from wafers which have successfully passed the wafer acceptance testing may be released for further production.

5.4.6 Documentation

Data documentation shall be in accordance with Para. 10.7 of this specification.

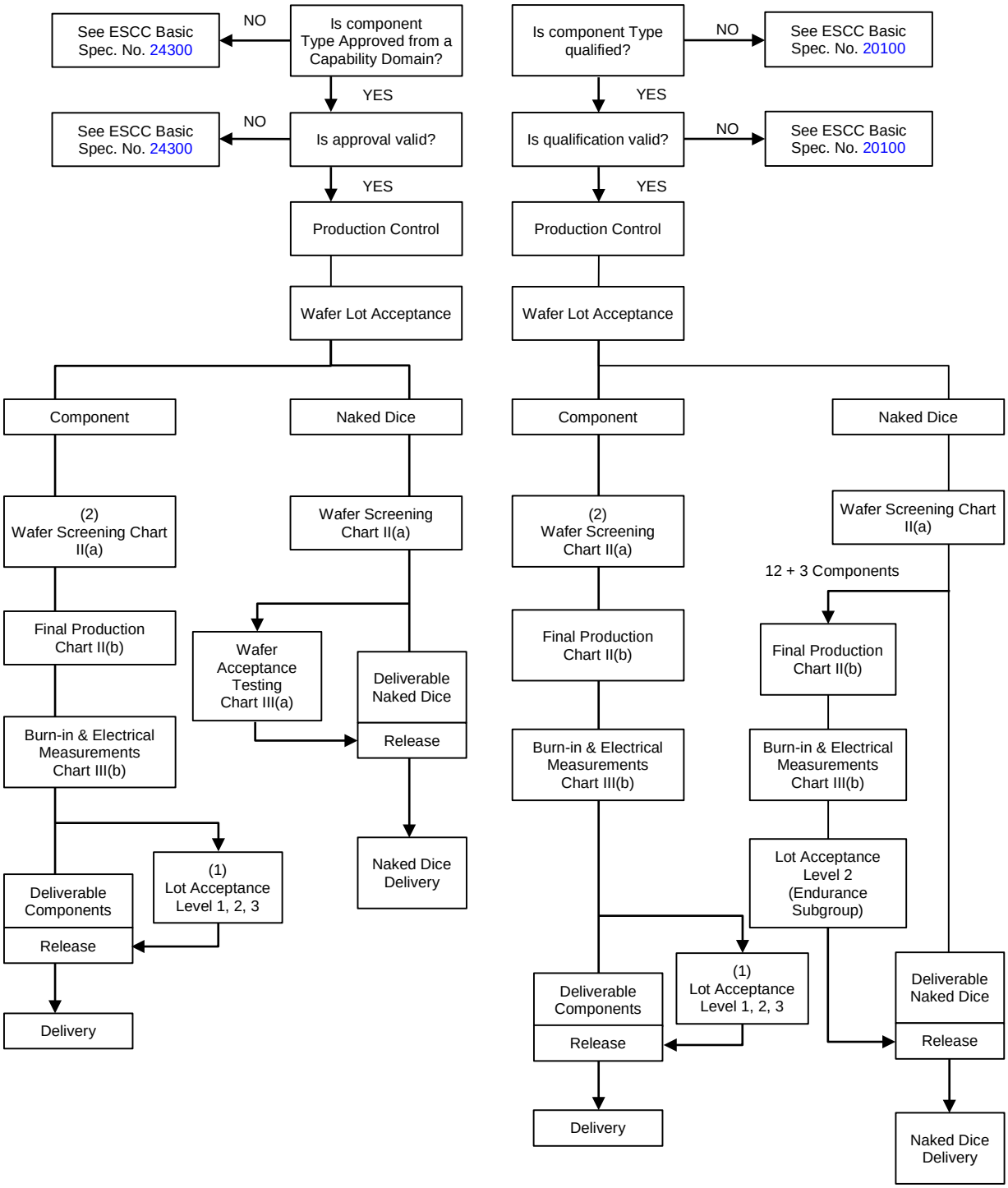
CHART I(a) - TESTING LEVELS



NOTES

1. When applicable.

CHART I(b) - PROCUREMENT PROCEDURES



NOTES

1. When applicable.
2. The performance of these tests is left to the Manufacturer's discretion.

6 FINAL PRODUCTION TESTS

6.1 GENERAL

Unless otherwise specified in the Detail Specification, all components or packaged test structures used for qualification testing, for approval testing of a capability domain and all components for delivery, including those submitted to lot acceptance tests, shall be subjected to tests and inspections in accordance with Chart II(b).

Unless otherwise specified in the Detail Specification, the tests shall be performed in the order shown.

Any components that do not meet these requirements shall be removed from the lot and at no future time be re-submitted to the requirements of this specification.

6.2 TEST METHODS AND CONDITIONS

The applicable test methods and conditions are specified in the paragraphs referenced in Chart II(b) of this specification.

6.3 DOCUMENTATION

Documentation of final production test data shall be in accordance with the requirements of Para. 10.8 of this specification.

7 BURN-IN AND ELECTRICAL MEASUREMENTS

7.1 GENERAL

Unless otherwise specified in the Detail Specification, all components or packaged test structures used for qualification testing, for approval testing of a capability domain and all components for delivery, including those submitted to lot acceptance tests, shall be subjected to tests and inspections in accordance with Chart III(b).

Unless otherwise specified in the Detail Specification, the tests shall be performed in the order shown.

The applicable test methods and conditions are specified in the paragraphs referenced in Chart III(b). Components of testing level 'B' shall be serialised prior to the tests and inspections.

7.2 FAILURE CRITERIA

7.2.1 Parameter Drift Failure

The acceptable delta limits are shown in Table 4 of the Detail Specification. A component of testing level 'B' shall be counted as a parameter drift failure if the changes during high temperature reverse bias burn-in or during power burn-in are larger than the delta (Δ) values specified.

7.2.2 Parameter Limit Failure

A component shall be counted as a limit failure if one or more parameters exceed the limits shown in Tables 2 or 3 of the Detail Specification.

Any component which exhibits a limit failure prior to the burn-in sequence shall be rejected and not counted when determining lot rejection.

7.2.3 Other Failures

A component shall be counted as a failure in any of the following cases:

- Mechanical failure.
- Handling failure.
- Lost component.

7.3 FAILED COMPONENTS

A component shall be considered as a failed component if it exhibits one or more of the failure modes described in Para. 7.2 of this specification.

7.4 LOT FAILURE

In the case of lot failure, the Manufacturer shall act in accordance with the requirements of Para. 4.3.1 of this specification.

7.4.1 Lot Failure during 100% Testing

If the number of components failed on the basis of the failure criteria described in Para. 7.2 exceeds 5% (rounded upwards to the nearest whole number) of the number of components submitted to burn-in and electrical measurements, the lot shall be considered as failed.

If a lot is composed of groups of components of one family defined in one ESCC Detail Specification, but separately identifiable for any reason, then the lot failure criteria shall apply separately to each identifiable group.

7.4.2 Lot Failure during Sample Testing

A lot shall be considered as failed if the number of allowable failures during sample testing in accordance with General Inspection Level II of IEC Publication No. 410 and the applicable AQL as specified in the Detail Specification, is exceeded.

If a lot failure occurs, a 100% testing may be performed with the lot failure criteria given in Para. 7.4.1.

7.5 DOCUMENTATION

Data documentation of burn-in and electrical measurements shall be in accordance with Para. 10.9 of this specification.

8 QUALIFICATION APPROVAL, CAPABILITY APPROVAL AND LOT ACCEPTANCE TESTS

8.1 COMPONENT TYPE QUALIFICATION TESTING

8.1.1 General

Qualification testing shall be in accordance with the requirements of Chart IV of this specification. The tests of Chart IV shall be performed on the specified sample, chosen at random from components which have successfully passed the tests in Charts II(b) and III(b) for testing level 'B'. This sample constitutes the qualification test lot.

The qualification test lot is divided into subgroups of tests and all components assigned to a subgroup shall be subjected to all of the tests in that subgroup, in the sequence shown.

The applicable test requirements are detailed in the paragraphs referenced in Chart IV.

The conditions governing qualification testing are given in ESCC Basic Specification No. 20100, Para. 5.3 and, for the extension or renewal of qualification approval, in Paras. 6.3 and 6.4.

8.1.2 Distribution within the Qualification Test Lot

The qualification test lot shall be comprised in accordance with the following provisions, depending on whether it is required to obtain qualification approval for a single MMIC component type or for a "family" of MMIC component types.

8.1.2.1 Single MMIC Component Type

When it is proposed to submit a single MMIC component type for qualification testing, the sample quantity shall be as specified in Chart IV, Note 1. However, when such a single MMIC component type is to be qualified in more than one type of package, each package variation must be equally represented in the environmental/mechanical subgroup (Subgroup I) and in the assembly/capability subgroup (Subgroup II). For this purpose, the applicable sample distribution shall be the same as for the qualification approval of a family of MMIC component types as specified in Chart IV, Note 2 or Note 3.

8.1.2.2 Family of MMIC Component Types

A family of MMIC component types is a series of integrated circuits produced by the same manufacturing techniques, up to and including final sealing in their encapsulations, using the same types of machines and apparatus and using the same MMIC design rules. Such MMICs will be designed for the same supply, bias and signal voltages and for an input/output compatibility with each other under an established set of loading rules. They shall be produced using the same technology (e.g. the same diffusion schedules, method of metallisation, etc.) and identical design rules. They may only differ in logic or analogue function.

Qualification approval may be granted to a family of monolithic microwave integrated circuits subject to the successful outcome of the qualification testing of certain specified MMIC component types to represent the family.

Structurally similar monolithic microwave integrated circuits from such a family may be grouped together for the purpose of selecting samples for qualification testing. The component types selected must adequately represent all of the various mechanical, structural and electrical elements encountered within the family.

The component types chosen must be those that employ the extremes of design rules and tolerances and contain the maximum of internal sub-circuitry complexity, i.e. usually those that give the greatest risk of rejection.

When qualification approval is required for component types in more than one type of package, each package variation must be adequately represented in the environmental/mechanical subgroup (Subgroup I) and in the assembly/capability subgroup (Subgroup II).

The component types may be specified by, but in any case shall be agreed with, the ESCC Executive, prior to the commencement of qualification testing and the justification for the selection shall be declared in the qualification test report.

The number of MMIC types selected as representative of the family will therefore determine the total number of components comprising the qualification test lot. Depending on the number of types selected, the sample sizes shall be determined as follows:

(a) Two types selected
The sample quantity for each type shall be as specified in Chart IV, Note 2.
(b) Three or more types selected
The sample quantity for each type shall be as specified in Chart IV, Note 3.

NOTES
1. In the case of four or more component types selected, different pass/fail criteria from those shown in Chart IV may be applicable. When appropriate, these shall be agreed with the ESCC Executive prior to the commencement of qualification testing.

8.2 CAPABILITY APPROVAL

Capability approval of a technology domain, and the qualification of a component within an approved domain, shall be in accordance with ESCC Basic Specification No. 24300.

8.3 LOT ACCEPTANCE TESTING

8.3.1 General

For component type qualification approval the sample sizes of the 3 lot acceptance levels are specified in Chart V. All components assigned to a subgroup shall be subjected to all of the tests of that subgroup in the sequence shown.

The tests to Chart V shall be performed on the specified sample which shall have been chosen, whenever possible, at random from the proposed delivery lot (but see Para. 8.3.3(b)).

For capability approval, the requirements for lot acceptance levels 3, 2 and 1 are defined in Paras. 8.3.3, 8.3.4 and 8.3.5 respectively.

For a qualified Manufacturer, the failure of 1 component shall be permitted when this is completely attributable to a handling or other human error and can be demonstrated to have no bearing on the inherent quality or reliability of the lot. The Manufacturer shall prepare a report justifying this assessment for inclusion in the lot data documentation. The Manufacturer shall also ensure that appropriate measures are taken to prevent a reoccurrence of the error and make objective evidence of these preventative measures available to the ESCC Executive, when requested.

As a minimum for procurement of non-qualified components, lot acceptance level 3 shall apply. For procurement of qualified components, lot acceptance testing shall be performed if specified in a purchase order. Procurement lots ordered with a lot acceptance test level shall be delivered only after successful completion of lot acceptance testing.

8.3.2 Distribution within the Sample for Lot Acceptance Testing

When components from the ordered lot are used, the sample for lot acceptance testing shall be comprised in accordance with the following provisions, depending on whether a single MMIC component type or a family of MMIC component types is considered.

8.3.2.1 Single MMIC component type

When a single MMIC component type is submitted to lot acceptance testing, the sample quantity shall be as specified in Chart V, Note 1. However, when such a single MMIC component type is being procured in more than one type of package, each package variation must be equally represented in the environmental/mechanical subgroup (LA1) and the assembly/capability subgroup (LA3).

For this purpose, the applicable sample distribution shall be the same as for the lot acceptance of types from a family of MMIC components as specified in Chart V, Note 2 or 3.

8.3.2.2 Family of MMIC component types

When a purchase order involves a range or series of component types, drawn from an MMIC family, the distribution of the component types for lot acceptance testing will normally vary from procurement to procurement.

The selection of component types for lot acceptance testing shall be agreed between the Manufacturer and the Orderer and specified by the Orderer.

Subject to the limitations of the range or series being procured, the component types selected should adequately represent all of the various mechanical, structural and electrical elements encountered within the family (see also Para. 8.1.2.2). The component types for submission to lot acceptance level 1 and/or 2 shall be selected such as to adequately represent all types comprising the total procurement.

Component types for submission to lot acceptance level 3 shall be drawn from each delivery lot.

When component types are being procured in more than one type of package, each package variation must be adequately represented in the environmental/mechanical subgroup (LA1) and the assembly/capability subgroup (LA3).

The number of MMIC types selected as representative of a particular procurement from a family will therefore determine the total number of components comprising the sample for lot acceptance testing.

Depending on the number of types selected, the sample sizes shall be determined as follows:

(a) Two types selected
The sample quantity for each type shall be as specified in Chart V, Note 2.
(b) Three or more types selected
The sample quantity for each type shall be as specified in Chart V, Note 3.

NOTES

1. In the case of 4 or more types selected, different pass/fail criteria from those shown in Chart V may be applicable.
   When appropriate, these shall be agreed between the Manufacturer and the Orderer prior to the commencement of lot acceptance testing.

8.3.3 Lot Acceptance Level 3 Testing (LA3)

For component type qualified components and for components qualified within an approved capability domain, when ordered, lot acceptance level 3 testing shall be performed on components from the ordered lot.

Lot acceptance level 3 tests are designated as the electrical subgroup and comprise electrical measurement of characteristics and tests to prove the assembly capability of the component. For LA3 testing the following requirements and conditions shall apply:

(a) LA3 testing shall be performed by the Manufacturer's quality assurance personnel using dedicated quality assurance equipment whenever possible. LA3 testing shall not be a repetition of routine measurements made by production personnel during final production tests and burn-in and electrical measurements.
(b) When tests to Tables 2 and 3 of the Detail Specification have been performed on a sample basis, the components for LA3 testing shall be selected from this sample.
(c) The electrical measurements for LA3 are considered to be non-destructive and therefore components so tested may form part of the delivery lot.
(d) The solderability test is considered to be destructive and therefore components so tested shall not form part of the delivery lot. Post-burn-in electrical rejects may be used for this test.
(e) When required in the purchase order, the Manufacturer shall notify the Orderer at least 2 working weeks before the commencement of LA3 testing. The Orderer shall indicate immediately whether or not he intends to witness the tests.

8.3.4 Lot Acceptance Level 2 Testing (LA2)

For component type qualified components, lot acceptance level 2 testing shall be performed on components from the ordered lot.

For components qualified within an approved capability domain, the lot acceptance level 2 testing shall be performed on test structures (as defined in Para. 6.3 of ESCC Basic Specification No. 24300) or on components from the ordered lot. If test structures are used, the test sequence, sample size and accept/reject criteria in the endurance subgroup of the capability approval test programme shall apply. In addition, the electrical subgroup of Chart V shall be performed on components from the ordered lot.

When components from the ordered lot are used, the lot acceptance level 2 testing shall comprise the tests for LA3 (electrical subgroup) plus tests on an endurance subgroup.

For the electrical subgroup, the requirements and conditions as for LA3 (see Para. 8.3.3) shall apply.

For the endurance subgroup, the following shall apply:

Components of testing level 'C', selected for the endurance subgroup, shall be serialised prior to the tests.

The tests in this subgroup are considered to be destructive and therefore components (of testing level 'B' or 'C') so tested shall not form part of the delivery lot.

8.3.5 Lot Acceptance Level 1 Testing (LA1)

For component type qualified components, lot acceptance level 1 testing shall be performed on components from the ordered lot.

For components qualified within an approved capability domain, the lot acceptance level 1 testing shall be performed on test structures or on components from the ordered lot. If test structures are used, the requirements of the capability approval test programme shall apply. In addition, the electrical subgroup of Chart V shall be performed on components from the ordered lot.

When components from the ordered lot are used the lot acceptance level 1 testing shall comprise the tests for LA3 (electrical subgroup) and LA2 (endurance subgroup) plus tests on an environmental and mechanical subgroup.

For the electrical and endurance subgroups, the requirements and conditions for LA3 (see Para. 8.3.3) and LA2 (see Para. 8.3.4) respectively shall apply.

For the environmental subgroup, the following shall apply:

(a) Components of testing level 'C', selected for the environmental subgroup, shall be serialised prior to the tests.
(b) The tests in this subgroup are considered to be destructive and therefore components (of testing level 'B' or 'C') so tested shall not form part of the delivery lot.

8.4 FAILURE CRITERIA

The following criteria shall apply to qualification testing and to lot acceptance testing.

8.4.1 Environmental and Mechanical Test Failures

The following shall be counted as component failures:

Components which fail during tests for which the pass/fail criteria are inherent in the test method, e.g. seal, solderability, terminal strength, etc.

8.4.2 Electrical Failures

The following shall be counted as component failures:

(a) Components which, when subjected to electrical measurements on completion of environmental tests, in accordance with either Table 2 or Table 6, as specified in the Detail Specification, fail one or more of the applicable limits.
(b) Components which, when subjected to electrical measurements at intermediate and end-points during endurance testing, in accordance with Table 6 of the Detail Specification, fail one or more of the applicable limits.
(c) Components which, when subjected to measurement of electrical characteristics, in accordance with Tables 2 and 3 of the Detail Specification, fail one or more of the applicable limits.

8.4.3 Other Failures

The following additional failures may also occur during qualification testing or lot acceptance testing:

(a) Components failing to comply with the requirements of ESCC Basic Specification No. 20500.
(b) Lost components.

8.5 FAILED COMPONENTS

A component shall be considered as failed if it exhibits one or more of the failure modes detailed in Para. 8.4 of this specification.

The allowable number of failed components per subgroup, the aggregate failure constraints and the permitted distribution of such failures are shown at the foot of Charts IV and V of this specification or in the capability approval test programme defined in ESCC Basic Specification No. 24300.

When requested by the Qualifying Space Agency or, the Orderer, failure analysis of failed components shall be performed by the Manufacturer and the results provided.

Failed components from successful lots shall be marked as such and be stored at the Manufacturer's plant for 24 months.

8.6 LOT FAILURE

A lot shall be considered as failed if the allowable number of failures according to Chart IV or V of this specification or the capability approval test programme defined in ESCC Basic Specification No. 24300, as relevant, has been exceeded.

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.1 of this specification.

8.7 DOCUMENTATION

8.7.1 Qualification Approval

For qualification testing, the qualification test data shall be documented in accordance with the requirements of Para. 10.10 of this specification.

In the case of lot acceptance testing, the data shall be documented in accordance with the requirements of Para. 10.12 of this specification.

8.7.2 Capability Approval

Data documentation for capability approval test programmes and lot acceptance testing of components qualified within an approved capability domain shall be in accordance with the requirements of Paras. 10.11 and 10.12 of this specification.

CHART II(a) - WAFER SCREENING

	Manufacture
Para. 9.5.3.1	Electrical Measurements at Room Temperature
Para. 9.5.2.1	Electrical Measurements at High and Low Temperatures
Para. 9.1	Wafer Dicing
Para. 9.2	Dice Visual Inspection

CHART III(a) - WAFER ACCEPTANCE TESTING

Para. 9.3	TCV and DEC Assembly (1)
Para. 9.4	Internal (pre-encapsulation) Visual Inspection
Para. 9.8	Encapsulation
Para. 9.13	Seal tests
Para. 9.5.1.1	Parameter Drift Value (Initial Measurements for Burn-in)
Para. 9.6	Burn-in
Para. 9.5.1.1	Parameter Drift Value (Final Measurements for Burn-in)
Para. 9.7.1	Bond Strength Test
Para. 9.7.2	Die Shear Test
Para. 5.4.5	Check for Wafer Rejection and Wafer Release

NOTES

1. The quantities required are specified in Para. 5.4.2 of this specification.

CHART II(b) - FINAL PRODUCTION TESTS

Production and Controls in accordance with Section 5 of this Specification		
Production up to encapsulation stage		
Para. 9.4	Internal (Pre-encapsulation) Visual Inspection	
Para. 9.7.1	Bond Strength Test	(1)
Para. 9.7.2	Die Shear Test	(1)
Para. 9.8	Encapsulation	
Para. 9.9	High Temperature Stabilisation Bake (Optional)	(2)
Para. 9.5.3.3	Electrical Measurements at Room Temperature (Optional)	(2)
Para. 9.10	Temperature Cycling	
Para. 9.12	Particle Impact Noise Detection (PIND) Test	(3) (4)
Para. 9.13	Seal Test, Fine and Gross Leak (Optional)	(2)
Para. 9.5.3.3	Electrical Measurements at Room Temperature	
Para. 9.16	Pre-burn-in (240 hours max.) (Optional)	(2)
Para. 9.5.3.3	Electrical Measurements at Room Temperature	(5)
Para. 4.4	Marking (plus Serialisation for Level ‘B’)	(6)
Para. 9.14	External Visual Inspection	
Para. 9.26	Dimension Check	(3)
TO CHART III(b)		

NOTES

1. If read and record data is available for the same wafer (lot) from production, this may replace the test.
2. The performance of this test is left to the Manufacturer's discretion.
3. This test shall not be performed during naked dice procurement.
4. Testing level 'B' only.
5. This test shall not be performed if pre-burn-in is omitted.
6. Marking may be performed at any time during Chart II(b) or III(b). Traceability requirements shall be met.

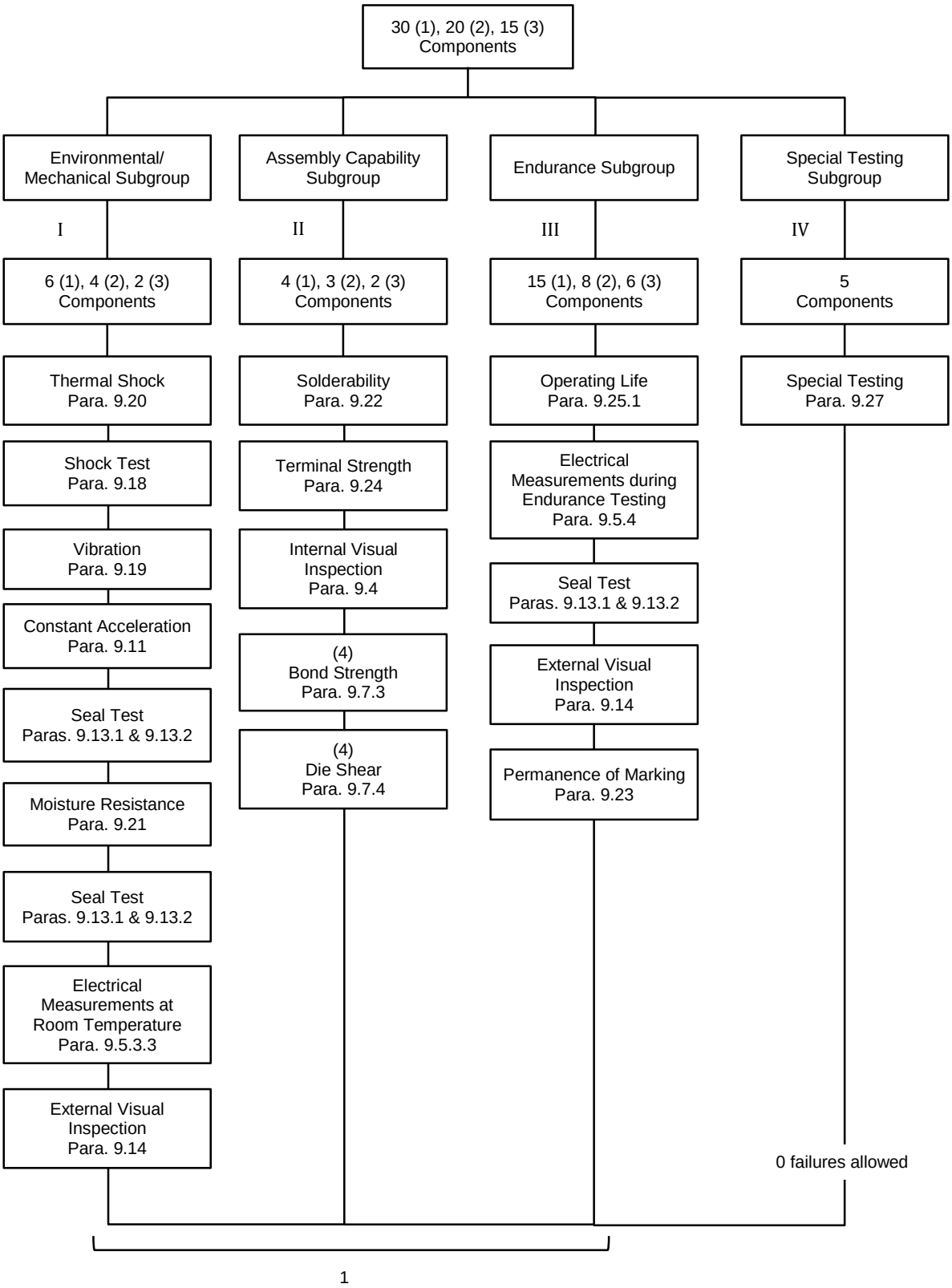
CHART III(b) - BURN-IN AND ELECTRICAL MEASUREMENTS

Components from Final Production Tests		Testing Levels	
		B	C
Para. 9.5.1.2	Parameter Drift Value (Initial Measurements for H.T.R.B) (1)	X	-
Para. 9.15	High Temperature Reverse Bias Burn-in	X	X
Para. 9.5.1.2	Parameter Drift Value (Final Measurements for H.T.R.B.; Initial Measurements for Power Burn-in)	X	-
Para. 9.16	Power Burn-in	X	X
Para. 9.5.1.2	Parameter Drift Value (Final Measurements for Power Burn-in)	X	-
Para. 9.5.3.3	Electrical Measurements at Room Temperature (2)	X	X
-	Hot Solder Dip (if applicable) (3)	X	X
Para. 9.5.2.2	Electrical Measurements at High and Low Temperatures (4)	X	X
Para. 9.17	Radiographic Inspection (4) (5)	X	-
Para. 9.13	Seal Test, Fine and Gross Leak (4) (5)	X	X
Para. 9.14	External Visual Inspection (4) (5)	X	X
Para. 9.5.3.3	Electrical Measurements at Room Temperature (Optional)	X	X
Para. 7.4	Check for Lot Failure	X	X
TO CHART IV or V			

NOTES

1. Measurements of parameters need not be repeated if data is available from last Electrical Measurements at Room Temperature.
2. The measurement of parameters for the calculation of drift value need not to be repeated tor electrical measurements at room temperature.
3. For components with hot solder dip final lead finish, the hot solder dip processing shall be performed at any time prior to High and Low Temperatures Electrical Measurements during Screening Tests. The requirements for hot solder dip are specified in ESCC Basic Specification No. 23500.
4. Rejects shall not be counted for lot failure.
5. This test shall not be performed during naked dice procurement.

CHART IV - QUALIFICATION TESTS

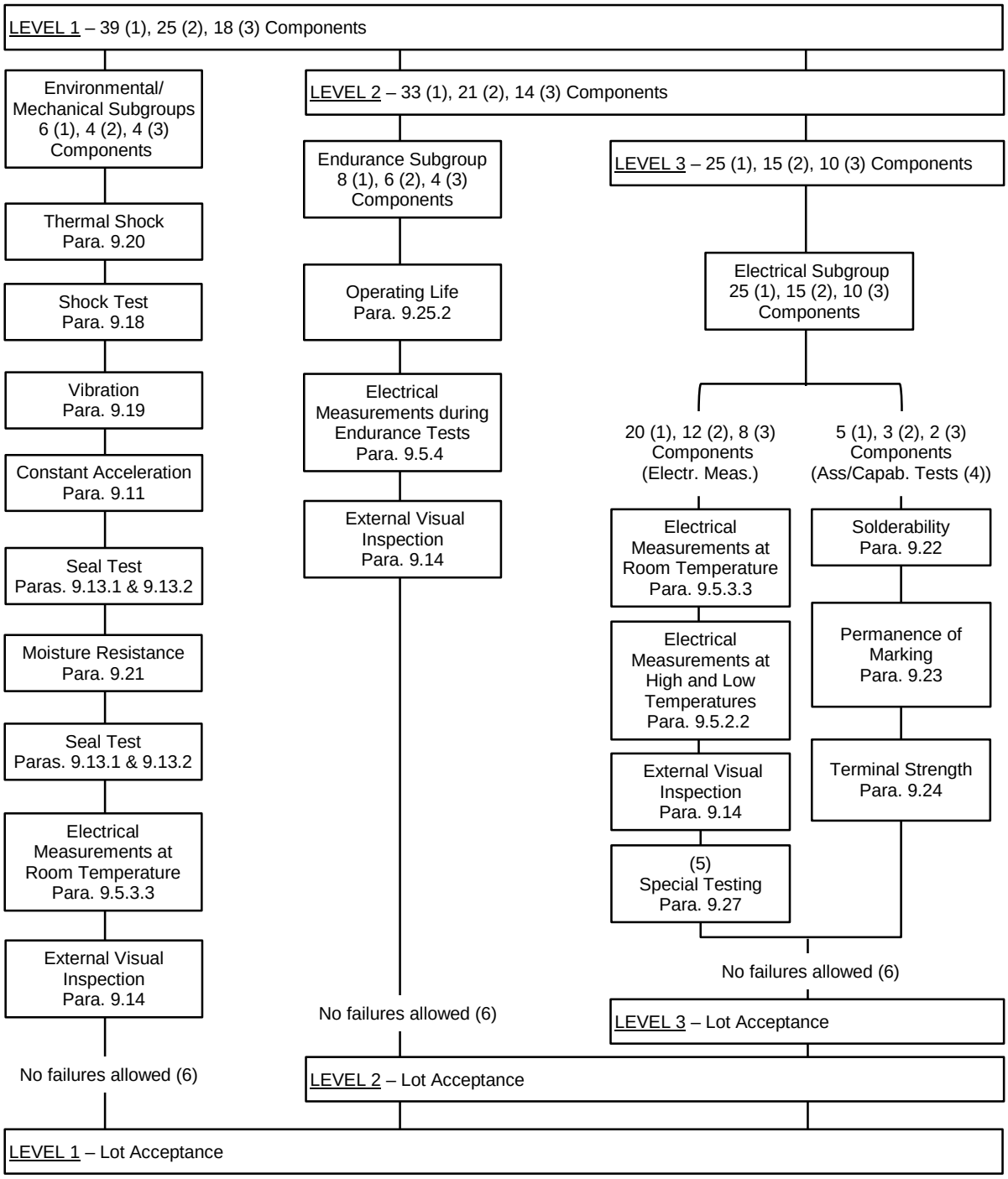


Total allowable number of failed components: 1

NOTES

1. Single MMIC type (see Para. 8.1.2.1)
2. Two types selected (see Para. 8.1.2.2).
3. Three or more types selected (see Para. 8.1.2.2).
4. No failures allowed for these tests.

CHART V - LOT ACCEPTANCE TESTS



NOTES

1. Single MMIC type (see Para. 8.3.2.1).
2. Two types selected (see Para. 8.3.2.2).
3. Three or more types selected (see Para. 8.3.2.2).
4. Post burn-in electrical rejects may be used for these tests.
5. If no special testing is specified in the Detail Specification, these parts are deliverable.
6. See Para. 8.3.1.

9 TEST METHODS AND PROCEDURES

If a Manufacturer elects to eliminate or modify a test method or procedure, the Manufacturer is still responsible for delivering components and naked dice that meet all of the performance, quality and reliability requirements defined in this specification and the Detail Specification.

Documentation supporting the change shall be approved by the ESCC Executive and retained by the Manufacturer. It shall be copied, when requested, to the ESCC Executive.

The change shall be specified in the Detail Specification and in the Process Identification Document (PID).

9.1 WAFER DICING

In accordance with the Process Identification Document (PID).

9.2 DICE VISUAL INSPECTION

In accordance with ESCC Basic Specification No. 20400 and the relevant paragraphs of the appropriate ancillary specification.

9.3 TCV AND DEC ASSEMBLY

Dice shall be assembled into their appropriate packages in accordance with the Process Identification Document (PID).

9.4 INTERNAL VISUAL INSPECTION

In accordance with ESCC Basic Specification No. 20400.

9.5 ELECTRICAL MEASUREMENTS

9.5.1 Parameter Drift Value Measurements

9.5.1.1 TCV and DEC

At each of the relevant data points, for TCV and DEC, measurements shall be made of all parameters listed in Table 4 of the TCV and DEC Test Document. All values obtained shall be recorded against serial numbers and the parameter drift calculated.

9.5.1.2 Components

At each of the relevant data points, for components of testing level 'B', measurements shall be made of all parameters listed in Table 4 of the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated.

9.5.2 Electrical Measurements at High and Low Temperatures

9.5.2.1 Wafers

DC and RF probe measurements, with traceability and wafer mapping, shall be performed on all processed wafers at high and low temperatures in accordance with Table 3 of the Detail Specification. The measurements shall be performed on 5 sample dice from each wafer chosen at random and all failed dice shall be identified.

If a failure occurs, further measurements shall be performed as specified in Para. 5.3.3 of this specification.

9.5.2.2 Components

For components of testing levels 'B' or 'C', the electrical measurements at high and low temperatures shall be made in accordance with Table 3 of the Detail Specification. For testing level 'B', all values obtained shall be recorded against serial numbers. The measurements shall be performed on 5 samples at random from the complete lot. If a failure occurs, the measurements shall be performed on the complete lot.

9.5.3 Electrical Measurements at Room Temperature

9.5.3.1 Wafers

DC and RF probe measurements, with traceability and wafer mapping, shall be performed on all processed wafers at room temperature in accordance with Table 2 of the Detail Specification. All values obtained shall be recorded by location and all failed dice shall be clearly identified.

As an alternative for procurement of components, the measurements may be performed go-no-go.

9.5.3.2 TCV and DEC

For TCV and DEC, electrical measurements at room temperature shall be performed in accordance with Table 2 of the TCV and DEC Test Document. All values obtained shall be recorded against serial numbers.

9.5.3.3 Components

For components of testing levels 'B' or 'C', the electrical measurements at room temperature shall be made in accordance with Table 2 of the Detail Specification. Where sample testing is applied, note the requirements of Para. 8.3.3(b). For testing level 'B', all values obtained shall be recorded against serial numbers, except during Final Production Tests (Chart II(b)).

9.5.4 Parameter Measurements during Environmental, Mechanical and Endurance Testing

At each of the relevant data points specified for environmental, mechanical and endurance testing, measurements shall be made of all parameters listed in Table 6 of the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated, if required.

9.6 TCV AND DEC BURN-IN

Burn-in on TCV and DEC shall be performed in accordance with the Table 5 of the TCV and DEC Test Document.

9.7 BOND STRENGTH AND DIE SHEAR TESTS

N.B.
These tests are destructive.

9.7.1 Bond Strength Test during Wafer Acceptance Test and Final Production Test

(a) Test Conditions

MIL-STD-883, Test Method 2011.

- Test Condition 'C' or 'D' for thermo-compression, ultrasonic or wedge-bonding.
- Test Condition 'F' for flip-chip bonding.
- Test Condition 'G' or 'H' for beam lead bonding.

(b) Test Procedures

- For device types having internal bonding wires numbering 8 or less, select 3 components at random from the lot accepted after internal (pre-encapsulation) visual inspection.
  Test all bonds.
- For device types having internal bonding wires numbering between 9 and 24, select 2 components at random from the lot accepted after internal (pre-encapsulation) visual inspection.
  Test all bonds.
- For device types having internal bonding wires numbering 25 or more, select 2 components at random from the lot accepted after internal (pre-encapsulation) visual inspection.
  Test 50% of the bonds on each component.

If agreed by the ESCC Executive (for qualification approval) or the Orderer (for a procurement), the components used for this test may have passed the low magnification phase only of the Internal Visual Inspection (Para. 9.4).

N.B.
The low magnification phase of the Internal Visual Inspection is that part of the inspection (at a magnification of < 100) that addresses the bonds, bond wires and die mount.

(c) Accept/Reject Criteria
Individual separation forces and categories shall be recorded. A single failure shall be cause for rejection of the lot.

9.7.2 Die-Shear Test during Wafer Acceptance Test and Final Production Tests

(a) Test Conditions
MIL-STD-883, Test Method 2019.

(b) Test Procedures
Perform the test on the components previously submitted to the bond strength test.

(c) Accept/Reject Criteria
Individual separation forces and categories shall be recorded. A single failure shall be cause for rejection of the lot.

9.7.3 Bond Strength Test during Qualification Testing

(a) Test Conditions
As per Para. 9.7.1(a).

(b) Test Procedures
As per Para. 9.7.1(b), but components to be selected from those in subgroup II of Chart IV or as derived from Para. 8.1 of ESCC Basic Specification No. 24300, as relevant.

(c) Accept/Reject Criteria:
As per Para. 9.7.1(c).

9.7.4 Die-Shear Test during Qualification Testing

(a) Test Conditions
As per Para. 9.7.2(a).

(b) Test Procedures
Perform the test on the components in subgroup II of Chart IV, or Para. 8.1 of ESCC Basic Specification No. 24300 previously submitted to the bond strength test.

(c) Accept/Reject Criteria
As per Para. 9.7.2(c).

9.8 ENCAPSULATION

In accordance with the Process Identification Document (PID).

9.9 HIGH TEMPERATURE STABILISATION BAKE

MIL-STD-883, Test Method 1008, Duration: 48 hours at maximum storage temperature rating specified in Table 1(b) of the Detail Specification.

9.10 TEMPERATURE CYCLING

MIL-STD-883, Test Method 1010. Test Condition: 'C'.

9.11 CONSTANT ACCELERATION

MIL-STD-883, Test Method 2001, Test Condition: 'E'; to be performed in plane Y_1 only. For MMICs which have a package weight of 5 grammes or more, Condition 'D' will be used.

9.12 PARTICLE IMPACT NOISE DETECTION (PIND)

MIL-STD-883, Test Method 2020, Test Condition 'A'. The use of the same attachment medium for the Sensitivity Test Unit (STU) and for the components under test (DUT) is not mandatory.

PIND prescreening shall not be performed.

The devices shall be submitted to PIND testing a maximum of 5 times and after each test run, defective devices shall be removed from the lot.

The lot may be accepted on any of the 5 runs if the percentage of defective devices is less than 1% (or 1, whichever is greater) of the devices tested.

Lots, which on the 5th run do not meet 1% PDA or which at any time exceed 25% cumulative, shall be rejected.

9.13 SEAL TEST

9.13.1 Seal Test, Fine Leak

MIL-STD-883, Test Method 1014, Condition 'A' or 'B'.

For Condition 'A1', leak rate: $5x10^{-8}atm.cm^3/sec$.

9.13.2 Seal Test, Gross Leak

MIL-STD-883, Test Method 1014, Condition 'C'.

9.14 EXTERNAL VISUAL INSPECTION

In accordance with ESCC Basic Specification No. 20500 or MIL-STD-883 Method 2009.

9.15 HIGH TEMPERATURE REVERSE BIAS BURN-IN

MIL-STD-883, Test Method 1015, Test Condition 'A'.

Duration and Test Conditions:

As specified, where applicable, in Table 5(a) of the Detail Specification.

Data Points:

For components of testing level 'B', undergoing the high temperature reverse bias test, the data points for parameter drift measurements shall be 0 hours (initial) and the test end point as specified in Table 5(a) of the Detail Specification.

9.16 POWER BURN-IN

MIL-STD-883, Test Method 1015, Test Condition 'B', 'D' or 'E'.

Duration:

Unless otherwise specified in the Detail Specification, components of level 'B' shall be subjected to a total power burn-in period of 240 hours and components of level 'C' to a total period of 168 hours.

Test Conditions: As specified in Table 5(b) of the Detail Specification.

Data Points:

For components of testing level 'B', undergoing a total burn-in period of 240 hours, the data points for parameter drift measurements shall be 0 hours (initial) and 240 (+ 24- 0) hours (final). For components of testing level 'C', undergoing a total power burn-in of 168 hours, the data point for post power burn-in electrical measurements shall be 168 (+ 24- 0) hours.

9.17 RADIOGRAPHIC INSPECTION

In accordance with ESCC Basic Specification No. 20900 or MIL-STD-883 Method 2012.

9.18 SHOCK TEST

MIL-STD-883, Test Method 2002, Test Condition: 'B'.

9.19 VIBRATION

MIL-STD-883, Test Method 2007, Test Condition: 'A'.

9.20 THERMAL SHOCK

MIL-STD-883, Test Method 1011, Test Condition: 'C'.

9.21 MOISTURE RESISTANCE

MIL-STD-883, Test Method 1004.

9.22 SOLDERABILITY

MIL-STD-883, Test Method 2003, to be performed on all terminals.

The use of activated fluxes (RMA and RA or OA) shall be allowed on leadless devices with gold finished terminals. All activated fluxes must be immediately cleaned off after dipping using an acceptable solvent in accordance with Para. 4.3 of ESCC Basic Specification No. 23500.

9.23 PERMANENCE OF MARKING

In accordance with ESCC Basic Specification No. 24800.

9.24 TERMINAL STRENGTH

MIL-STD-883, Test Method 2004, Test Condition 'A' for strip-line packages, Test Condition 'D' for chip carrier packages or Test Condition 'B2' for all other packages. For Condition 'B2', 3 leads (excluding corner leads) or 10% of the leads (whichever is greater) are to be randomly selected on each component of the sample.

9.25 OPERATING LIFE

9.25.1 Operating Life during Qualification Testing

MIL-STD-883, Test Method 1005.

Duration: 2000 hours.

Test conditions: As specified in the Detail Specification.

Data Points

Measurements at intermediate and end points according to Table 6 of the Detail Specification at 0, 1000 ± 48 hours and 2000 ± 48 hours. In the case where Table 6 specifies "changes", the drift shall always be related to the 0-hour measurement.

9.25.2 Operating Life during Lot Acceptance Testing

MIL-STD-883, Test Method 1005.

Duration: 1000 hours.

Test conditions: As specified in the Detail Specification.

Data Points

Measurements at 0 hours and at 1000 ± 48 hours according to Table 6 of the Detail Specification.

9.26 DIMENSION CHECK

In accordance with ESCC Basic Specification No. 20500 and the Detail Specification. To be performed on 3 samples only.

If a failure occurs, the complete lot shall be checked.

9.27 SPECIAL TESTING

The requirements for special testing shall be defined in the Detail Specification. The Detail Specification shall also state whether the test is destructive or not.

10 DATA DOCUMENTATION

10.1 GENERAL

For the qualification or capability approval records and with each component or naked chip delivery, a data documentation package is required. Depending on the testing level and lot acceptance level specified for the component, this package shall be compiled from:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Wafer lot acceptance data (if specified in the Purchase Order).
(e) Wafer screening data (Chart II(a)) (when applicable).
(f) Wafer acceptance testing data (Chart III(a)) (when applicable).
(g) Final production test data (Chart II(b)) (but see Para. 10.8).
(h) Burn-in and electrical measurement data (Chart III(b)).
(i) Qualification test data (Chart IV).
(j) Capability approval test data.
(k) Lot acceptance test data (Chart V) (when applicable).
(l) Failed components list (see Paras. 7.3 and 8.5) and failure analysis report (see Para. 8.5).
(m) Certificate of Conformity.
(n) Radiographic inspection photographs.
(o) SEM photographs.

Items (a) to (o) inclusive shall be grouped, preferably as subpackages and, for identification purposes, each page shall include the following information:

– ESCC Component Number.
– Manufacturer's name.
– Lot identification.
– Date of establishment of the document.
– Page number.

10.1.1 Qualification Approval

In the case of qualification approval, the items listed in Para. 10.1 (a) to (o) less items (e), (f), (j) and (k) are required.

10.1.2 Capability Approval

In case of capability approval, the items listed in Para. 10.1(a) to (o) less items (e), (f), (i) and (k) are required.

10.1.3 Component Delivery to Testing Level 'B'

10.1.3.1 Qualified Components

For deliveries of qualified components, the following documents shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity).
(b) Certificate of Conformity (including range of delivered serial numbers).
(c) Attributes record of measurements, tests and inspections performed in Chart II(b), Chart III(b) (including PDA figure) and Chart V (where applicable).
(d) Failed components list.
(e) Read and record data from Chart III(b) (if specified in the purchase order).

10.1.3.2 Unqualified Components

For deliveries of unqualified components, the documentation to be supplied shall be in accordance with Para. 10.1.3.1 plus the following:

(a) Wafer lot acceptance data (if specified in the Purchase Order).
(b) Read and record data from Chart III(b).
(c) Failure analysis report on failed components.

10.1.4 Component Delivery to Testing Level 'C'

10.1.4.1 Qualified Components

For deliveries of qualified components, the following documentation shall be supplied:

(a) Certificate of Conformity.

10.1.4.2 Unqualified Components

For deliveries of unqualified components, the documentation to be supplied shall be in accordance with Para. 10.1.4.1 plus the following:

(a) Cover sheet {if all of the information is not included in the Certificate of Conformity).
(b) Wafer lot acceptance data (if specified in the Purchase Order).
(c) Attributes record of all measurements, tests and inspections performed in Charts II(b), III(b) and V (when applicable).
(d) Failed components list (including Failure Analysis Report).

For components submitted to LA1 and LA2 testing, item (c) of Para. 10.1 shall also be provided (see Paras. 8.3.4(a) and 8.3.5(a)).

10.1.5 Dice Delivery

10.1.5.1 Type Qualified

For deliveries of type qualified naked dice, the following documentation shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity).
(b) Wafer lot acceptance data (if specified in the Purchase Order).
(c) Attributes record of all measurements, tests and inspections performed in Chart II(a).
(d) Wafer screening read and record test data from Chart II(a), including data mapping, (if specified in the Purchase Order).
(e) Attributes record of all measurements, tests and inspections performed in Chart II(b), Chart III(b) (including PDA figure) and Chart V for the test vehicles.
(f) Certificate of Conformity.

10.1.5.2 Type Approved

For deliveries of type approved naked dice, the following documentation shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity).
(b) Wafer lot acceptance data (if specified in the Purchase Order).
(c) Attributes record of all measurements, tests and inspections performed in Chart II(a).
(d) Wafer screening read and record test data from Chart II(a), including data mapping, (if specified in the Purchase Order).
(e) Attributes record of all measurements, tests and inspections performed in Chart III(a) (including PDA figure).
(f) Certificate of Conformity.

10.1.6 Data Retention/Data Access

If not delivered, all data shall be retained by the Manufacturer for a minimum of 5 years during which time it shall be available to the ESCC Executive and the Orderer, if requested, for review. The Manufacturer shall deliver variables Data/Reports to the Orderer if specified above or if required by the Purchase Order.

10.2 COVER SHEET(S)

The cover sheet(s) of the data documentation package shall include as a minimum:

(a) Reference to the Detail Specification, including issue and date.
(b) Reference to the applicable ESCC Generic Specification, including issue and date.
(c) Component type and number.
(d) Lot identification.
(e) Range of delivered serial numbers (for components of testing level 'B').
(f) Number of purchase order.
(g) Radiation testing level.
(h) Information relative to any additions to this specification and/or the Detail Specification.
(i) Manufacturer's name and address.
(j) Location of the manufacturing plant (specify place of diffusion, assembly and test).
(k) Signature on behalf of Manufacturer.
(l) Total number of pages of the data package.

10.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be prepared, if not in accordance with the data given in the Process Identification Document (PID). Where applicable, this list shall contain inventory number, Manufacturer's type number, serial number, etc. This list shall indicate for which tests such equipment was used.

10.4 LIST OF TEST REFERENCES

This list shall include all Manufacturer's references or codes which are necessary to correlate the test data provided with the applicable tests specified in the tables of the Detail Specification.

10.5 WAFER LOT ACCEPTANCE TEST DATA

Statistical Process Control (SPC) data for each wafer lot shall be supplied if specified in the Purchase Order.

Data of SEM inspection shall be provided in accordance with the requirements of ESCC Basic Specification No. 21400.

Radiation test report shall be provided in accordance with the requirements of ESCC Basic Specification No. 22900 (if required).

10.6 WAFER SCREENING DATA (CHART II(A))

A test result summary shall be compiled showing the total number of wafers submitted to, and the total number of dice rejected after each of the following tests:

- Electrical measurements at room temperature (Para. 9.5.3.1).
- Electrical measurements at high and low temperatures (Para. 9.5.2.1).
- Wafer dicing (Para. 9.1).
- Dice visual inspection (Para. 9.2).

In the case of naked dice delivery, read and record data shall be supplied for the following (if specified in the Purchase Order):

- Electrical measurements at room temperature (Para. 9.5.3.1)
- Electrical measurements at high and low temperatures (Para. 9.5.2.1)

10.7 WAFER ACCEPTANCE TESTING DATA (CHART III(A))

A test results summary shall be compiled showing the total number of dice submitted to, and the total number of TCVs and DECs rejected after each of the following tests:

- TCV and DEC Assembly (Para. 9.3).
- Pre-encapsulation internal visual inspection (Para. 9.4).
- Seal test (fine and gross leak) (Para. 9.13).
- Parameter drift value (Initial Measurements) (Para. 9.5.1.1)
- Burn-in (Para. 9.6).
- Parameter drift value (Final Measurements) (Para. 9.5.1.1).
- Bond strength (Para. 9.7.1).
- Die shear (Para. 9.7.2).

For the bond strength and die-shear tests, the separation forces and categories shall be recorded. The deltas shall be calculated and recorded.

10.8 FINAL PRODUCTION TEST DATA (CHART II(B))

A test result summary shall be compiled showing the total number submitted to, and the total number rejected after each of the following tests:

- Pre-encapsulation internal visual inspection (Para. 9.4).
- Bond strength and die-shear test (Para. 9.7).
- Seal test (fine and gross leak) (Para. 9.13) (when applicable).
- Environmental tests (Paras. 9.9, 9.10 and 9.12)
- Electrical measurements at high and low temperatures (Para. 9.5.2.2) (when applicable)
- Electrical measurements at room temperature (Para. 9.5.3.3)
- External visual inspection (Para. 9.4)
- Dimension check (Para. 9.26).

For the bond strength and die-shear tests, the separation forces and categories shall be recorded.

The final production test data shall form an integral part of the data documentation package, but it is not a mandatory requirement that it be delivered with the qualification lot or delivery lot. However, the data package to be delivered shall contain the information as detailed in Para. 10.1.3 or 10.1.4 and at least shall contain a list of final production tests actually performed and a certification that the data is available for review.

10.9 BURN-IN AND ELECTRICAL MEASUREMENT DATA (CHART III(B))

10.9.1 Testing Level 'B'

For components of testing level 'B', all data shall refer to the relevant serial numbers. Against these serial numbers, data shall be recorded for the following:

(a) HTRB burn-in measurements and delta values
(b) 0-hour measurement for power burn-in.
(c) 240 hour measurement for power burn-in.
(d) Delta values after power burn-in.
(e) Values obtained during measurements at high and low temperatures (Table 3 of the Detail Specification).
(f) Values obtained during measurements of electrical characteristics (Table 2 of the Detail Specification).
(g) Failures during seal test.
(h) Failures during external visual inspection.
(i) Photographs from radiographic inspection, including those of reject components.

10.9.2 Testing Level 'C'

For components of testing level 'C', a test result summary (i.e. the total number of components subjected to, and the total number rejected from, each of the tests and inspections) shall be prepared.

10.10 QUALIFICATION TEST DATA (CHART IV)

All data shall be referenced to the relevant serial numbers. Detailed records shall be provided of the components submitted to each test in each of the subgroups and of those rejected. Detailed data shall be provided of all electrical measurements made in accordance with Tables 2 and 6 of the Detail Specification, as and where applicable.

10.11 CAPABILITY APPROVAL TEST DATA

Detailed records shall be provided of the components and test structures submitted to each test, and of those rejected. If applicable, all data shall be referenced to serial numbers.

Detailed data shall be provided of all electrical measurements made in accordance with Tables 2 and 6 of the Detail Specification, as and where applicable.

10.12 LOT ACCEPTANCE TEST DATA (CHART V)

10.12.1 Testing Level 'B'

All data shall be referenced to the relevant serial numbers. Detailed records shall be provided of the components and test structures submitted to each test in each of the subgroups (as relevant to the lot acceptance level) and of those rejected.

Detailed data shall be provided of all electrical measurements made in accordance with Tables 2, 3 and 6 of the Detail Specification, as and where applicable.

10.12.2 Testing Level 'C'

A test result summary (i.e. the total number of components and test structures submitted to, and the total number of those rejected from, each of the tests and inspections) as relevant to the lot acceptance level acceptance level shall be provided.

In the case of lot acceptance 2 testing, all data in respect of electrical measurements made in accordance with Table 6 of the Detail Specification shall be referenced to the relevant serial numbers (see Para. 8.3.4(a)).

In the case of lot acceptance 1 testing, all data in respect of electrical measurements made in accordance with Tables 2, 3 and 6 of the Detail Specification shall be referenced to the relevant serial numbers (see Para. 8.3.5(a)).

10.13 FAILED COMPONENTS LIST AND FAILURE ANALYSIS REPORT

The failed components list and failure analysis report shall provide full details of:

(a) The reference number and description of the test or measurement performed as defined in this specification and/or the Detail Specification.
(b) The serial number (if applicable) of the failed component.
(c) The failed parameter and the failure mode of the component.
(d) Detailed failure analysis, if requested.
(e) In the case of an allowed failure during Chart V (see Para. 8.3.1), a report shall always be supplied.

10.14 CERTIFICATE OF CONFORMITY

A Certificate of Conformity shall be established as defined in ESCC Basic Specification No. 20100 or ESCC Basic Specification No. 24300.

11 DELIVERY

For qualification or capability approval, the disposition of the approval test lot and its related documentation shall be as specified in ESCC Basic Specification Nos. 20100 or 24300 and the relevant paragraphs of Section 10 of this specification.

For procurement, for each order, the items forming the delivery are:

(a) The delivery lot.
(b) The components used for lot acceptance testing, (when applicable), but not forming part of the delivery lot (see Paras. 8.3.3(d), 8.3.4(b) and 8.3.5(b)).
(c) The relevant documentation in accordance with the requirement of Section 10 of this specification.

In the case of a component for which a valid qualification or capability approval is in force, all data of all components submitted to LA1 and LA2 testing shall also be copied, when requested, to the ESCC Executive.

12 PACKAGING AND DESPATCH

The packaging and despatch of components to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 20600.