REQUIREMENTS FOR CAPABILITY APPROVAL OF DISCRETE MICROWAVE SEMICONDUCTOR COMPONENTS

ESCC Basic Specification No. 2435010

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1 PURPOSE

This specification defines the requirements for the Capability Approval of Discrete Microwave Semiconductor Components. It outlines the requirements for the definition of the Capability Domain and its boundaries, the evaluation of a Capability Domain, Capability Approval testing and Component Type Approval testing. ESCC Basic Specification No. 24300 gives the general requirements for Capability Approval of electronic component technologies.

2 APPLICABLE DOCUMENTS

The following ESCC specifications are applicable to the extent specified herein. The relevant issues shall be those in effect on the date the Capability Approval is granted by the ESCC Executive.

2.1 ESCC SPECIFICATIONS

- No. 5010, Discrete Microwave Semiconductor Components, Hermetically sealed and Naked Die
- No. 22600, Requirements for the Evaluation of standard electronic Components for Space Applications
- No. 22700, Requirements and Guidelines for the Process Identification Document (PID).
- No. 24300, Requirements for the Capability Approval of Electronic Component Technologies for Space Application.

3 INTRODUCTION

Capability Approval is a status given to a Manufacturer for a specified Discrete Microwave Semiconductor Component domain after successful completion of an ESCC evaluation, in accordance with ESCC 2265010, and completion of a Capability Approval Programme as described in ESCC Basic Specification No. 24300, the relevant section of ESCC No. 5010 and this document.

Capability Approval as defined in this specification applies to both Packaged Components and Naked Die Components as specified in ESCC No. 5010.

4 DEFINITION OF CAPABILITY DOMAIN AND BOUNDARIES

4.1 GENERAL

The Manufacturer shall define the Capability Domain for which Capability Approval is sought as required in ESCC Basic Specification No. 24300.

This definition shall result in the Process Identification Document (PID). The general requirements for this document are given in ESCC Basic Specification No. 22700.

This definition has to demonstrate that the Capability Domain represents a structured, and controllably restricted, fully documented design methodology and manufacturing process for Discrete Microwave Semiconductor Components.

The definition of the Capability Domain shall also comprise the areas listed in the following paragraphs at least to the extent detailed therein. Additional information shall be supplied whenever necessitated by the particular nature of the technology under approval. In case any one of the characteristics in the following paragraphs should not apply to the technology and/or methodology under approval, this shall be stated in the PID.

Within the definition of the Capability Domain, 6 areas are of particular concern:

- The physical design and procedures which are closely related to the manufacturing process.
- The design system and procedures used to implement the component design methodology.
- The interface between design and manufacturing.
- The manufacturing itself
- The inspection and test procedures.
- The traceability.

These areas are addressed in the following paragraphs.

4.2 PHYSICAL DESIGN

The physical design is governed by a set of technology specific rules and parameters. The construction and composition of components within the Capability Domain are defined, modelled, implemented, and tested using a fixed set of procedures as defined in the PID.

The description of the physical design requires the definition of at least the following characteristics:

(a) The physical characteristics, which specifies the topology of all types of physical structures, in terms of:
  - Physical function (e.g. substrate material, active layer, doping profile, recess, conductor, contact, dielectric, passivation, glassivation, pad composition and size, any passive element used for current ballasting, air-bridges, via-holes, backside metallisation and composition).
  - Substrate information (e.g. traceability, composition, characteristics, performances, visual criteria, specifications)
  - Epitaxy information (procurement specification, lot traceability, materials)
  - Shape (e.g. aspect ratios, polygons, angles).
  - Size (e.g. minimum/maximum width/length/depth, allowed range for number of gate/emitter fingers (2, 4, 6, 8, or higher), allowed range for unit gate width (e.g. 50µm to 200µm)).
  - Positioning (e.g. overlaps of compound structures, spacing between structures of equal or different nature, field plate spacings and geometries).

- The dimensions of all layers (e.g. epitaxy, mesa, recess, implantation, bridge, trenches, metallisation, passivation….)
- Pre-matched or unmatched variants

(b) The electrical rule and parameter set in terms of:
- The DC and RF current carrying capability of all metal and active layers.
- The specific capacitance between layers (e.g.poly/substrate,metal/substrate, metal/dielectric/metal) distinguishing sheet and edge capacitances.
- Equivalent circuit element values (e.g. capacitances, resistance, inductance, transconductance etc.).
- Sheet resistivity of metal layers.
- Dielectric breakdown voltages (DC and RF, if applicable).
- Transistor and diode parameters including DC and RF limits of application.
- Critical distance between individual cells
- Junction temperature operating guarantees for nominal application per type of structure (structure size, bias and temperature).
- Thermal resistance model vs structure size
- Maximum limits of operation (e.g. biasing, junction temperature, RF drive level, DC power dissipation and gate current, gate width per unit of area)

4.3 DESIGN SYSTEM

The component design methodology is defined by the design system and all other procedures applied in the design of a Discrete Microwave Semiconductor Component. The design system comprises simulation models, basic design data and software.

The Capability Approval of a design system requires as a minimum:

- The implementation of a configuration control system guaranteeing the traceability of all software and data forming part of the system and
- The application of a quality assurance system addressing at least documentation procedures, acceptance testing prior to system release and the organisation of error reporting and corrective action procedures.

Both systems shall be fully documented and their application has to be evident. At least the following items shall be covered in the PID:

(a) A general description of the design system including block diagrams representing:
- The software structure of the system.
- The design flow, distinguishing between interactive and automatic actions.

(b) The library of fixed cells, including pad cells, shall be described at least in terms of the following relevant details:
- The layout of all the discrete cells characterised by its name, connections and dimensions including the parameter limits of these cells.
- The detailed circuit schematic including effective element size.
- The final layout after completion of all post processing steps such as compaction or shrinking. It shall be presented in the form of a physical plot using a scale allowing clear recognition of all structures.

(c) The component model library, including as a minimum the following relevant details:
- DC, small signal and large signal models of all discrete cells, as applicable, with their scaling rules and limits of validity.
- Typical and maximum variations of all the electrical parameters of the discrete cells within a wafer, from wafer to wafer and from batch lot to batch lot.
- A thermal resistance model (e.g. case to junction or naked die back face to junction where relevant) allowing the junction temperature of all discrete cells to be determined. The PID shall define or reference the test procedure used for determining thermal resistance.
- The derated DC bias condition and limits of validity.
- The verification procedure of all the models shall be described.

(d) Software and associated data shall be described in terms of:
- The origin and version of commercial software allowed for electrical design, verification and layout.
- The version and programming language for in-house developed software.
- Verification of the in-house software shall be described.
- Definition of data formats.
- Definition of programme interfaces.

(e) A description of the configuration control system

(f) A description of the quality assurance system

4.4 INTERFACE BETWEEN COMPONENT DESIGN AND MANUFACTURING

For components intended to be qualified by means of component type approval on the basis of Capability Approval, a statement of compliance (Design Compliance Matrix) is required. This statement confirms the compliance of a particular component within the Capability Domain(s) to which it is attributed. This statement of compliance shall be issued during design review in the form of a Design Compliance Matrix.

During the design review the following items shall be addressed, as a minimum, in the following order:

- Die size (max and min, allowed width to length ratio W/L),
- Assembly capability (die backside and bond pad materials and thicknesses, recommended assembly process for die with via holes)
- Discrete component architecture
- Discrete component schematics
- Simulation results
- Sensitivity and stability analysis
- Layout (alignment check for all masks, design rule check)
- Maximum rating (DC only)
- RF maximum input drive
- Derating analysis
- Package details
- Prediction of parasitic and thermal effects (including bonding wires) introduced by the package
- Compliance of packaged components to the technical requirements
- Completion of design compliance matrix

The Design Compliance Matrix (checklist) shall be agreed by the Manufacturer and the Designer. Evidence that the design is completely within, and limited to, the approved Capability Domain shall be submitted to the ESCC Executive. The Design Compliance Matrix shall address as a minimum the following items:

- The component has been designed based on cells, models, layout, assembly details, package, etc... as stated in the PID.
- Any discrepancies, modifications of models, layout, assembly details, packages etc. shall be clearly described and assessed.

The Designer shall provide full information regarding documentation control and traceability of:

- The hardware, software, data safe-keeping and traceability used for this design.
- The description of the function and expected characteristic.
- Stability and sensitivity analysis of the component.
- De-rating analysis.

The ESCC Executive shall have free access to this information at the Designer's premises.

This compliance matrix form shall be referenced in the PID.

4.5 MANUFACTURE

4.5.1 Materials

The Manufacturer shall describe the procedures for selection, procurement and control of materials used for the production of components within the Capability Domain. The PID shall, as a minimum, cover the following items:

- The selection and qualification (approval methodology) of the materials used. A list of procurement specifications for the selected materials.
- A list of incoming inspection procedures and other documents used to ensure the consistent quality of materials.
- Procedures for traceability and control of limited shelf life items.

4.5.2 Technologies

The Manufacturer's description of the basic technologies for the manufacture of Discrete Microwave Semiconductor Components shall include as a minimum, but not be limited to, the following:

- Type of technology i.e. MESFET, HFET, P-HEMT, HBT, BJT, DIODE, etc...
- Type of substrate (GaAs, Si, SiGe, InP, SiC, GaN, Diamond, etc), orientation, epitaxy, backside etc...
- Metal material system used (e.g. for ohmic contacts, gate metals, lines, pads, Via-holes and back side metal layers including barriers).
- Die size range.
- Method of pattern formation.
- Method for die attach.
- Material and method for wire bonding.
- Encapsulation method, materials and material combinations used.
- Range of packages (if applicable).

4.5.3 Processes

The Manufacturer shall describe the processes for procuring raw materials (e.g. wafers, epitaxy), packages and the manufacture /assembly of components within the Capability Domain. He shall also give references to the documents specifying the processes. At least the following areas shall be covered including a statement of the equipment used:

- Clean room conditions.
- Wafer preparation.
- Mask manufacture and methods for identification of masks.
- Photolithographic methods (application and drying of photoresist, exposure, development, etching, photoresist removal, cleaning etc.).
- Active layer formation including etching methods.
- Dielectric and passivation deposition processes.
- Wafer storage conditions before, during and after processing.
- Probing, dicing.
- Assembly line
- Assembly processes (materials used, die attach, wire bonding, encapsulation).

The PID shall contain a list of all package types, manufacturers and pin counts to be included in the Capability Domain.

The largest package (size and/or pin count) of each type represents a boundary of the Capability Domain.

The largest device periphery (gate width and/or output power) represents a boundary of the Capability Domain

4.6 INSPECTION AND TEST

The Manufacturer shall describe the inspection and test methods and include references to the documents specifying the methods. As a minimum the following areas shall be covered:

- Incoming inspection testing.
- In-process inspection and testing (including SPC data and trend charts, with typical limits).
- Test equipment.
- Wafer Lot Acceptance testing (including Wafer Screening) (per ESCC No. 5010).
- Special In-Process Controls testing (per ESCC No. 5010).
- Pre-Encapsulation and Final Customer Source Inspections
- Screening Tests (per ESCC No. 5010).
- Component Type Approval testing.
- Qualification and Periodic Testing (including Lot Validation Testing) (per ESCC No. 5010).

4.7 TRACEABILITY

The Manufacturer shall describe the method for assuring traceability of materials, test structures, packages and components. At least the following points shall be covered:

- The use of purchase orders and specifications
- The use of route sheet and travellers
- The traceability of test structures

If the Manufacturer intends to deliver naked dice in the frame of the Capability Approval, the naked dice shall be traceable with respect to wafer, wafer lot and ESCC Detail Specification. When applicable, die traceability to the Component Type Approval testing report, Capability Approval certificate and related Capability Domain shall also be maintained.

5 TEST STRUCTURES AND MEASUREMENT METHODS

5.1 GENERAL

Representative Discrete Components (RDCs) are the preferred vehicle to be used for evaluation, Capability Approval testing and process control. These structures shall be described in the PID

Technology Characterisation Vehicles (TCVs) and Dynamic Evaluation Circuits (DECs), which shall also be described in the PID, can also be considered to be used as test structures in cases where they contribute to gathering information on process control and process stability (e.g. for determining process limits, current handling capability of metal lines, … etc) and to allow ease of testing (e.g. RFOW probing) in the case where it would be difficult to fully evaluate an RDC on wafer (e.g. for very large gate periphery power transistors).

The description of the RDC, TCV and DEC within the PID shall include Detail Specification and a Design Compliance Matrix.

5.2 REPRESENTATIVE DISCRETE COMPONENT (RDC)

The Representative Discrete Component (RDC) is one or a set of Discrete Microwave Semiconductor Components representative of the range of die layout/structure, assembly and packaging techniques within the Capability Domain. RDCs shall be designed and manufactured within the boundaries of the Capability Domain.

The purpose of the RDC is to:

- Validate the design domain (design models, thermal model, design system, layout rules, assembly rules, package suitability).
- Validate performance capability (e.g. max derated DC bias and junction temperature, frequency capability, RF output power capability)
- Confirm the reliability model and/or reliability figures of the process, obtained during the evaluation phase (random and/or wearout FIT figures, allowed temperature range, MTTF) under multiple stress environments.

Discrete Microwave Semiconductor Components that have already been developed, or are under development, may be proposed as RDCs provided they are in accordance with the Capability Domain and as far as they are representative and useful to verify the design and manufacturing capability.

Preferably the RDC should be designed to allow RF-on-Wafer (RFOW) measurements, however in some instances this may not be possible (e.g. due to thermal limitations imposed by large periphery transistors). When this is the case, alternative on wafer test screening approaches shall be proposed by the manufacturer and agreed with the ESCC Executive.

5.3 TECHNOLOGY CHARACTERISATION VEHICLE (TCV)

A TCV shall consist of basic elements from the cell library including specific elements relevant of the technology. The TCV could be a set of different test vehicles. Process Control Monitor (PCM) elements could be included in the TCV. The TCV must be designed with the most constrained design rules.

5.4 DYNAMIC EVALUATION CIRCUIT (DEC)

A Dynamic Evaluation Circuit shall be one or a set of discrete active elements. It shall be able to be bonded into a discrete package.

5.5 DESIGN AND LAYOUT RULES

RDCs, TCVs and DECs shall be included as test structures to verify the geometrical layout rule set, to consolidate thermal model for maximum junction temperature determination and to allow electrical, thermal and optical evaluation of the layer to layer misalignment which might occur during manufacturing and due to any processing anomalies.

In order to magnify problems and to enhance the diagnostic capabilities, test structures with design layout rules beyond worst case may be added where these would help to define process and device limits and help to assess reliability.

5.6 TECHNOLOGY

Additional appropriate test structures shall be provided for the evaluation of other known failure modes or parametric sensitivity or degradation affecting the technology under approval when subjected to radiation or other specific applications.

6 EVALUATION OF A CAPABILITY DOMAIN

The evaluation of a Capability Domain shall be performed first in accordance with the requirements of ESCC Basic Specification No. 22600 and then in accordance with ESCC Basic Specification No. 2265010 and related ancillary specifications.

On completion of evaluation testing, the final definition of the Capability Domain and its boundaries shall be agreed between the Manufacturer and the ESCC Executive, and the Capability Abstract shall be issued.

7 CAPABILITY APPROVAL TESTING

7.1 GENERAL

The general requirements for the preparation of a Capability Approval test programme are defined in ESCC Basic Specification No. 24300. This programme shall be reviewed and approved by the ESCC Executive prior to the start of Capability Approval testing.

The Capability Approval test programme for technologies covered by this specification shall generally consist of the tests and subgroups given in Chart IA or IB of this specification, as applicable. The requirements specified therein may be reduced by the ESCC Executive if it is demonstrated that particular requirements have already been covered in a different but equivalent qualification, evaluation or Capability Approval programme. The test vehicles submitted to Chart IA or IB testing shall be the RDC as defined in the PID. All packaging related tests shall be performed on the package with the highest pin count for each type of package and/or with the largest size transistor (gate periphery/output power within the Capability Domain) as stated in the PID.

Prior to RDCs being subjected to Capability Approval testing (Chart IA or IB of this specification), they shall first be subjected to the tests and inspections in accordance with the following:

(a) Production Control (including Wafer Lot Acceptance and Special In-Process Controls) (Para. 5/Chart F2 of ESCC No. 5010).

(b) Screening Tests (Para. 6/Chart F3 of ESCC No. 5010).

7.2 CAPABILITY APPROVAL TEST REPORT

On completion of the Capability Approval testing, the Manufacturer shall assemble all relevant test data and documentation in the form of a test report. This report shall be sent to the ESCC Executive for review.

8 COMPONENT TYPE APPROVAL TEST

8.1 GENERAL

For a component type manufactured within a Discrete Microwave Semiconductor Component Capability Domain, the qualification procedure of ESCC Basic Specification No. 24300 shall apply.

Component Type Approval testing is only applicable to those components that have been designed and manufactured within the boundaries of an approved Capability Domain and for which a statement of compliance has been issued.

The Component Type Approval testing shall be performed on the specified sample, chosen at random from components assembled in hermetic microwave packages which have successfully passed the tests and inspections in Production Control (Chart F2) and Screening Tests (Chart F3) in accordance with ESCC No. 5010. For Component Type Approval testing of Naked Die Components, the samples shall be chosen at random from the components in the Packaged Test Sublot, which have successfully passed the tests and inspections in Production Control (Chart F2) and Screening Tests (Chart F3) in accordance with ESCC No. 5010.

Component Type Approval testing shall consist of the tests specified in Chart II of this specification both for Packaged Components and Naked Die Components.

Sample size shall be 17 pieces minimum. The sample size shall be approved by the ESCC Executive prior to commencing the tests. Acceptance criteria shall be zero failures.

8.2 TEST METHODS AND CONDITIONS

8.2.1 Thermal Analysis

Thermal analysis shall be performed using industry standard or well proven methods to identify "hot-spots" which shall include, but not be limited to, infra-red cameras, liquid crystal or Raman measurements. Regions of abnormally elevated temperature shall be identified and characterised.

8.2.2 DC and RF Characterisation

Characterisation shall be carried out under "worst-case" operating conditions which shall include, when applicable, but not be restricted to:

- RF overdrive
- Input/ Output mismatching
- Source and load pulling
- Pushing and pulling (oscillators).
- Pulsed operation applications
- Continuous and transient operation stress limits recommended for the safe operating area.

8.2.3 Operating Life Test

DC and RF operating life test shall be performed in accordance with ESCC No. 5010, Para. 8.18 and Chart F4. No failures shall be allowed.

9 REDUCTION, EXTENSION AND CHANGE OF THE CAPABILITY DOMAIN

Any modification such as reduction, extension and change of the Capability Domain shall be in accordance with ESCC Basic Specification No. 24300.

In order to classify potential modifications, an evaluation matrix shall be included in the PID. This evaluation matrix features the parameters defining the Capability Domain and their interdependence. The relevance of a parameter in conjunction with the consequences for related parameters will support an efficient classification as minor or major changes.

For the distinction between minor and major changes the following shall be considered as a general guideline:

- Minor changes shall have no or only little impact on the Capability Domain and its boundaries, and must be downward compatible (previously designed components must still be manufacturable without redesign or changes to their specification). This may be the case for isolated parameter changes or the replacement of equipment and materials for the purpose of yield enhancement or to improve safety margins. The expansion of libraries can be considered a minor modification if similar prototypes are already existing but require documentation as per Para. 4.3 of this document.

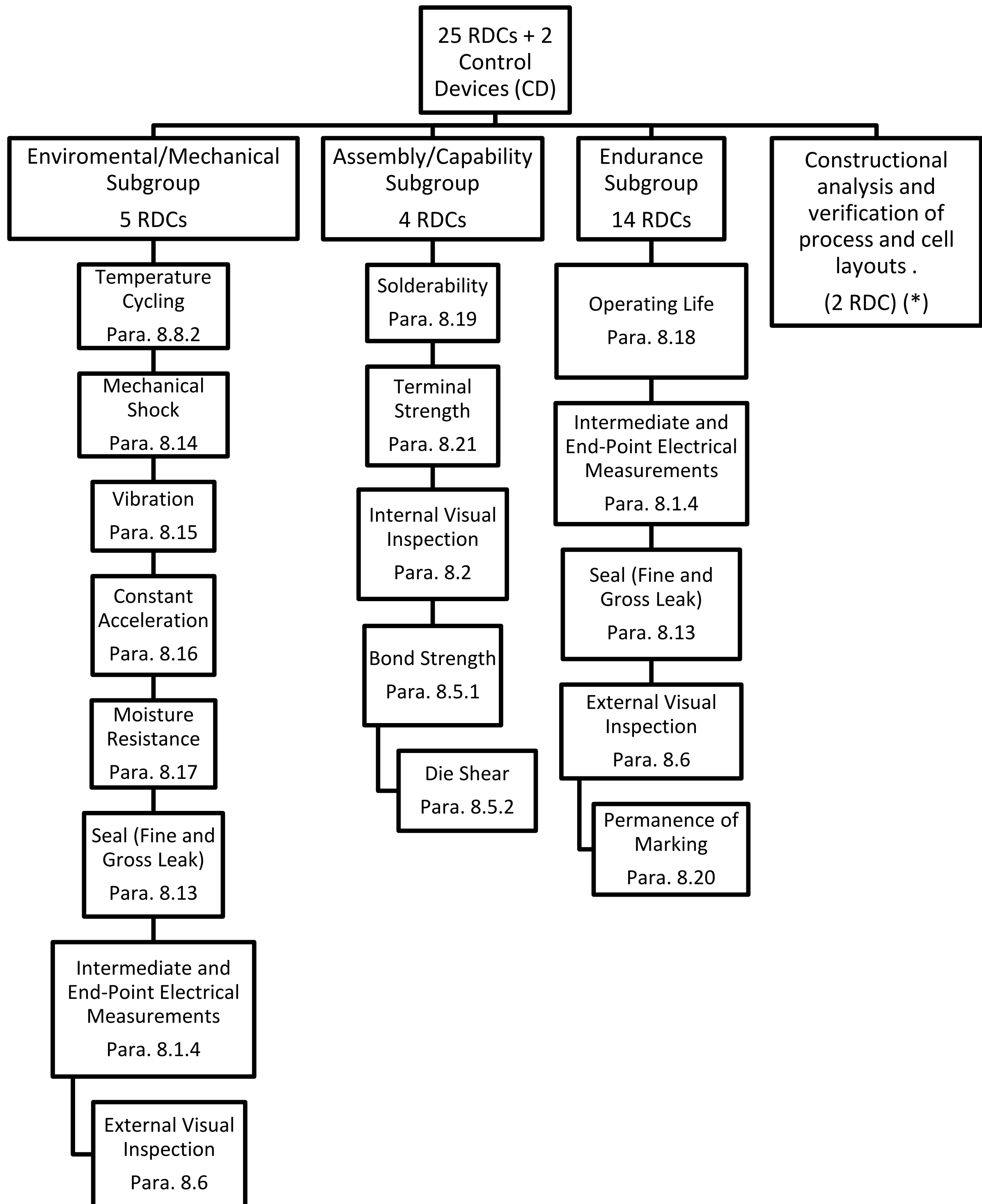
In case of doubt or if circuit performance or radiation tolerance is adversely affected, changes must be classified as major.

10 PROCUREMENT

Procurement of components manufactured within the Capability Domain and qualified in accordance with ESCC No. 24300, shall be in accordance with the requirements ESCC No. 5010 (ref. Chart F1A or Chart F1B).

11 CHARTS

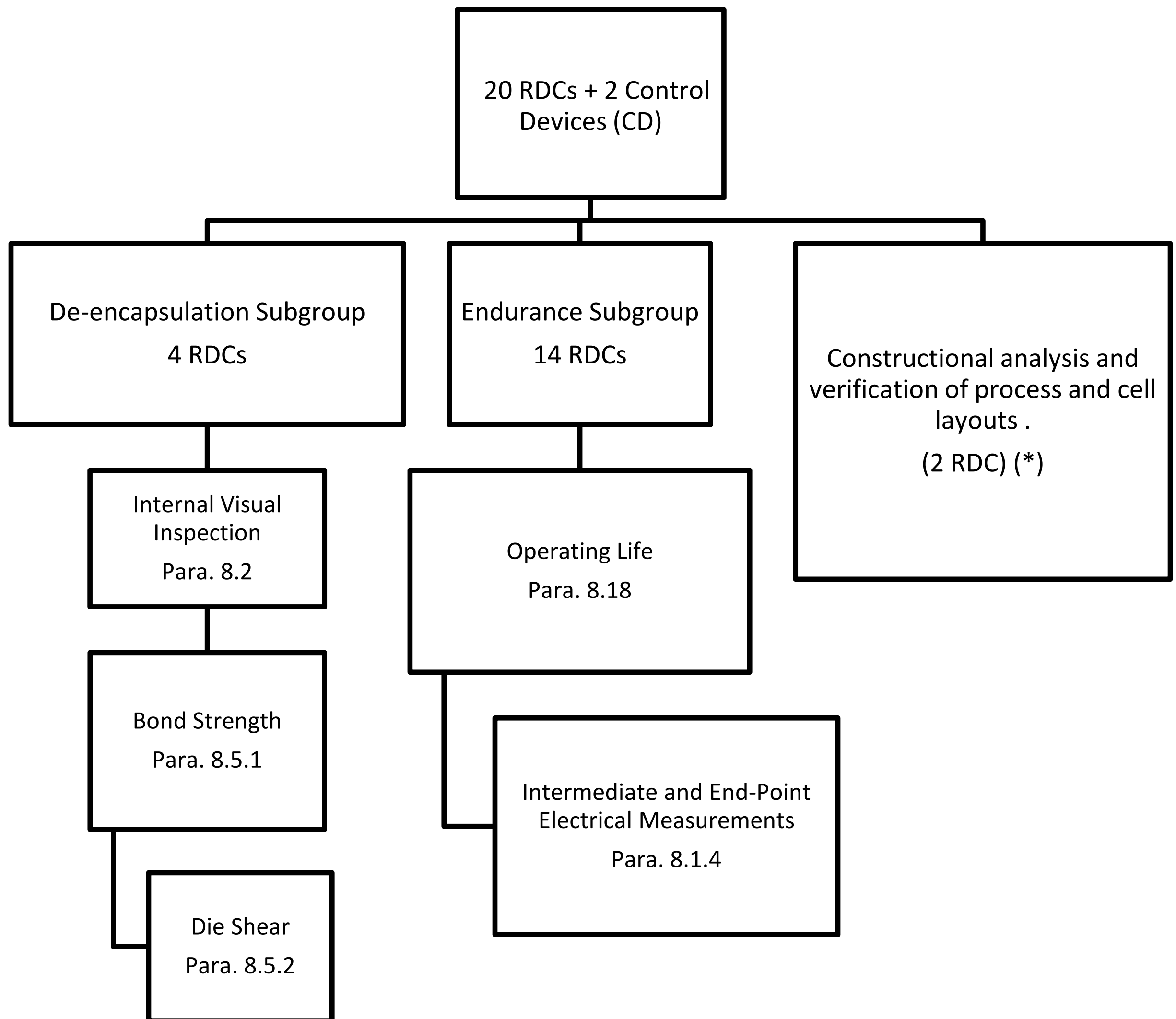
11.1 CHART IA – CAPABILITY APPROVAL TESTING FOR PACKAGED COMPONENTS



NOTES:

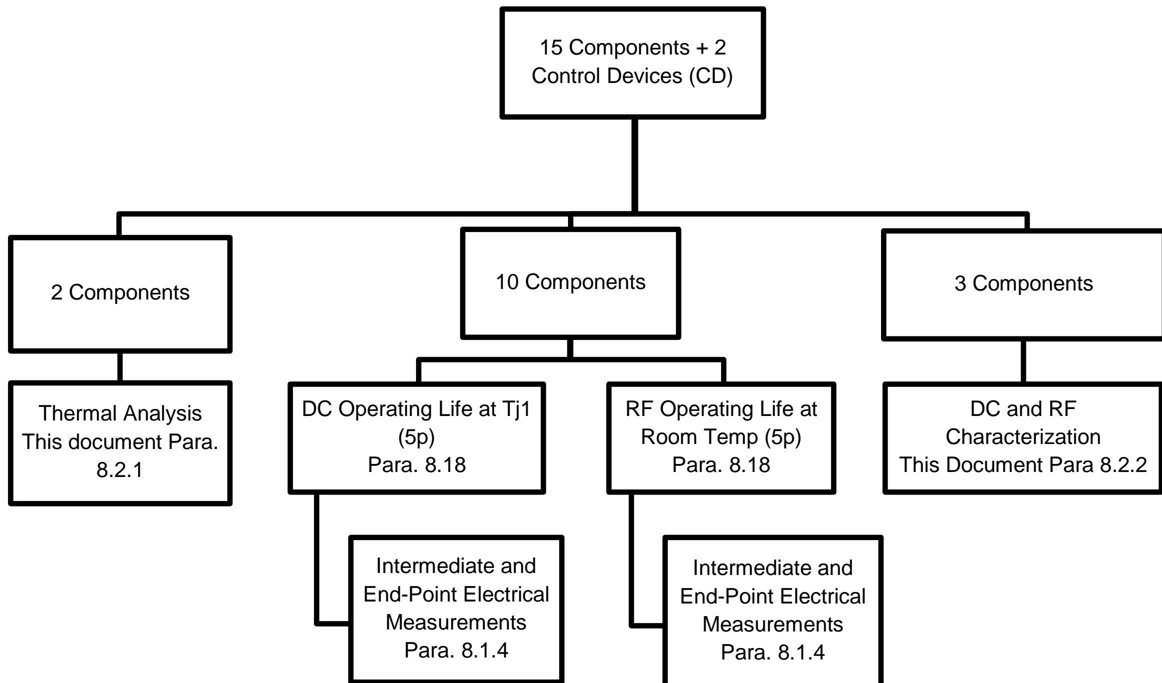
1. All referenced paragraphs in this Chart refer to ESCC No. 5010
2. No failures allowed for these tests.
3. (*) mechanical devices may be used

11.2 CHART IB – CAPABILITY APPROVAL TESTING FOR NAKED DIE COMPONENTS



NOTES:
1. To be performed on samples taken from the Packaged Test Sublot.
2. All referenced paragraphs in this Chart refer to ESCC No. 5010
3. No failures allowed for these tests.
4. (*) mechanical devices may be used

11.3 CHART II – COMPONENT TYPE APPROVAL TESTING



NOTES:

1. Applicable for Component Type Approval testing of both Packaged Components and Naked Die Components.
2. For Naked Die Components, to be performed on samples taken from the Packaged Test Sublot.
3. All referenced paragraphs in this Chart refer to ESCC No. 5010
4. No failures allowed for these tests.