



**INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS
STATIC 16K X 9BIT, PARALLEL FIRST IN FIRST OUT
MEMORY WITH THREE STATE OUTPUTS**

BASED ON TYPE 67206H, 672061H

ESCC Detail Specification No. 9301/048

Issue 2	August 2015
---------	-------------



Document Custodian: European Space Agency – see <https://escies.org>

LEGAL DISCLAIMER AND COPYRIGHT

European Space Agency, Copyright © 2015. All rights reserved.

The European Space Agency disclaims any liability or responsibility, to any person or entity, with respect to any loss or damage caused, or alleged to be caused, directly or indirectly by the use and application of this ESCC publication.

This publication, without the prior permission of the European Space Agency and provided that it is not used for a commercial purpose, may be:

- copied in whole, in any medium, without alteration or modification.
- copied in part, in any medium, provided that the ESCC document identification, comprising the ESCC symbol, document number and document issue, is removed.

DOCUMENTATION CHANGE NOTICE

(Refer to <https://escies.org> for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
936	Specification upissued to incorporate editorial changes per DCR.

TABLE OF CONTENTS

1	GENERAL	5
1.1	SCOPE	5
1.2	APPLICABLE DOCUMENTS	5
1.3	TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS	5
1.4	THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS	5
1.4.1	The ESCC Component Number	5
1.4.2	Component Type Variants	5
1.5	MAXIMUM RATINGS	6
1.6	HANDLING PRECAUTIONS	7
1.7	PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION	7
1.7.1	Multilayer Ceramic Dual-in-line Package (MDIL28) - 28 Pin	7
1.7.2	Flat Leaded Multilayer Flat Package (MFP-F28) - 28 Lead	8
1.7.3	Notes to Physical Dimensions and Terminal Identification	9
1.8	FUNCTIONAL DIAGRAM	10
1.9	PIN ASSIGNMENT	11
1.10	TRUTH TABLES AND TIMING DIAGRAMS	11
1.11	PROTECTION NETWORKS	18
2	REQUIREMENTS	19
2.1	GENERAL	19
2.1.1	Deviations from the Generic Specification	19
2.1.1.1	Deviations from Screening Tests-Chart F3	19
2.2	MARKING	19
2.3	ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES	19
2.3.1	Room Temperature Electrical Measurements	19
2.3.2	High and Low Temperatures Electrical Measurements	26
2.4	PARAMETER DRIFT VALUES	27
2.5	INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS	27
2.6	POWER BURN-IN CONDITIONS	28
2.7	OPERATING LIFE CONDITIONS	28
2.8	TOTAL DOSE RADIATION TESTING	29
2.8.1	Bias Conditions and Total Dose Level for Total Dose Radiation Testing	29
2.8.2	Electrical Measurements for Total Dose Radiation Testing	29

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930104801P

- Detail Specification Reference: 9301048
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: P (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Access Time (ns)	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	67206H-15	15	MDIL28	G2	3.5	P [30kRAD(Si)]
02	67206H-15	15	MFP-F28	G2	3	P [30kRAD(Si)]
03	67206H-30	30	MDIL28	G2	3.5	P [30kRAD(Si)]
04	67206H-30	30	MFP-F28	G2	3	P [30kRAD(Si)]
05	672061H-15 (Note 1)	15	MDIL28	G2	3.5	P [30kRAD(Si)]
06	672061H-15 (Note 1)	15	MFP-F28	G2	3	P [30kRAD(Si)]
07	672061H-30 (Note 1)	30	MDIL28	G2	3.5	P [30kRAD(Si)]

Variant Number	Based on Type	Access Time (ns)	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
08	672061H-30 (Note 1)	30	MFP-F28	G2	3	P [30kRAD(Si)]

NOTES:

1. With Programmable Half-full Flag (PHF).
2. The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
3. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 7	V	Note 1
Input Voltage Range	V_{IN}	-0.5 to $V_{DD}+0.3$	V	Notes 1, 2
Output Voltage Range	V_{OUT}	-0.5 to $V_{DD}+0.3$	V	Notes 1, 2
Output Current into Outputs	I_O	50	mA	Low condition Note 3
Maximum Device Power Dissipation	P_D	2	W	
Operating Temperature	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature	T_{stg}	-65 to +150	°C	
Soldering Temperature	T_{sol}	+ 265	°C	Note 4
Junction Temperature	T_j	+150	°C	Note 5
Thermal Resistance Junction to Case	$R_{th(j-c)}$	3	°C/W	

NOTES:

1. Device is functional for $4.5 \leq V_{DD} \leq 5.5$ with reference to $V_{SS} = 0V$.
2. $V_{DD}+0.3V$ shall not exceed 7V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
5. Maximum junction temperature may be increased to +175°C during Power Burn-in and Operating Life.

1.6 HANDLING PRECAUTIONS

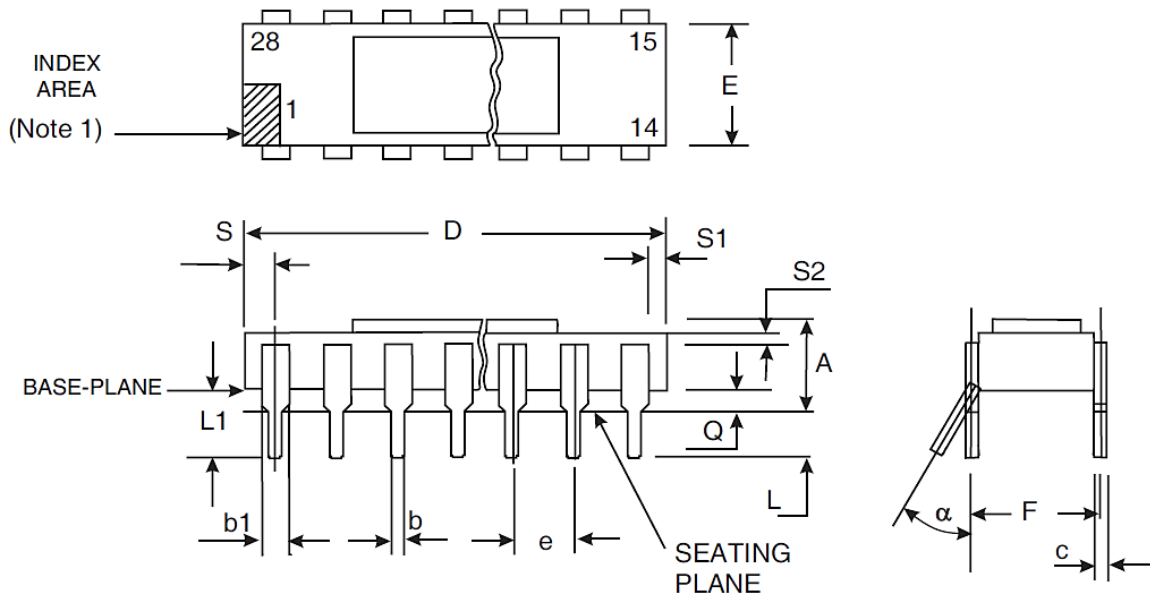
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Consolidated Notes are given following the case drawings and dimensions.

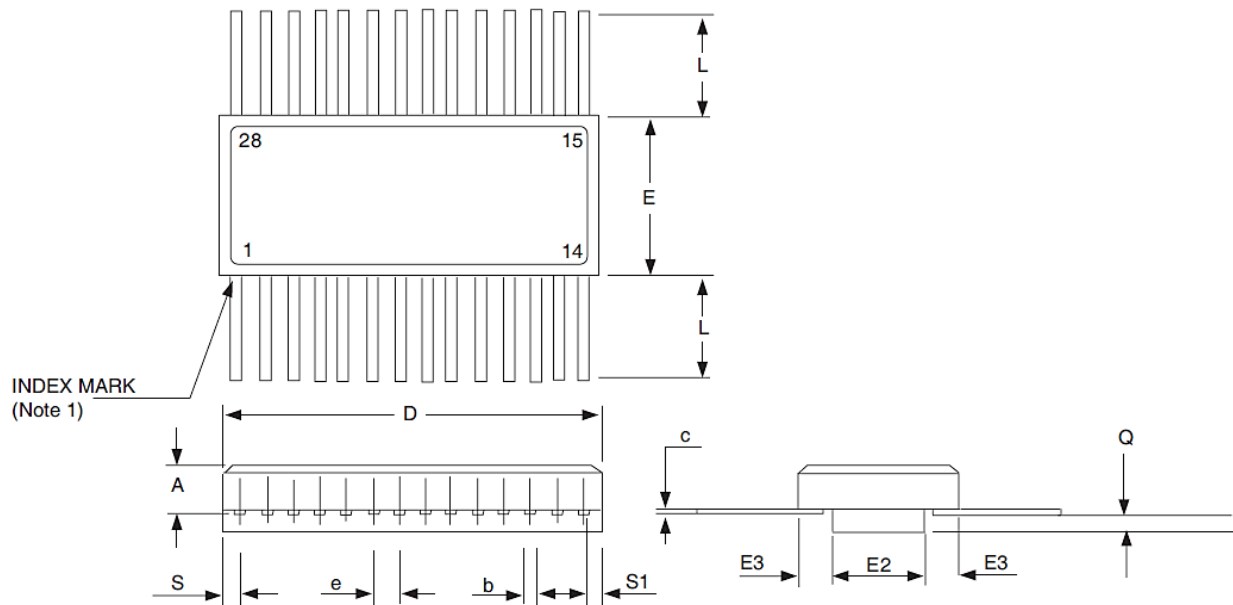
1.7.1 Multilayer Ceramic Dual-in-line Package (MDIL28) - 28 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	3.3	5.84	5
b	0.36	0.58	2
b1	0.96	1.65	2
c	0.2	0.38	2
D	-	37.72	
E	6.1	7.87	
F	7.37	8.13	6
e	2.54 BSC		2, 3
L	2.92	5.08	2, 5
L1	3.3	-	2

Symbols	Dimensions mm		Notes
	Min	Max	
Q	0.38	2.54	5
S	-	2.54	8
S1	0.13	-	8
S2	0.13	-	2
α	0°	15°	2

1.7.2 Flat Leaded Multilayer Flat Package (MFP-F28) - 28 Lead



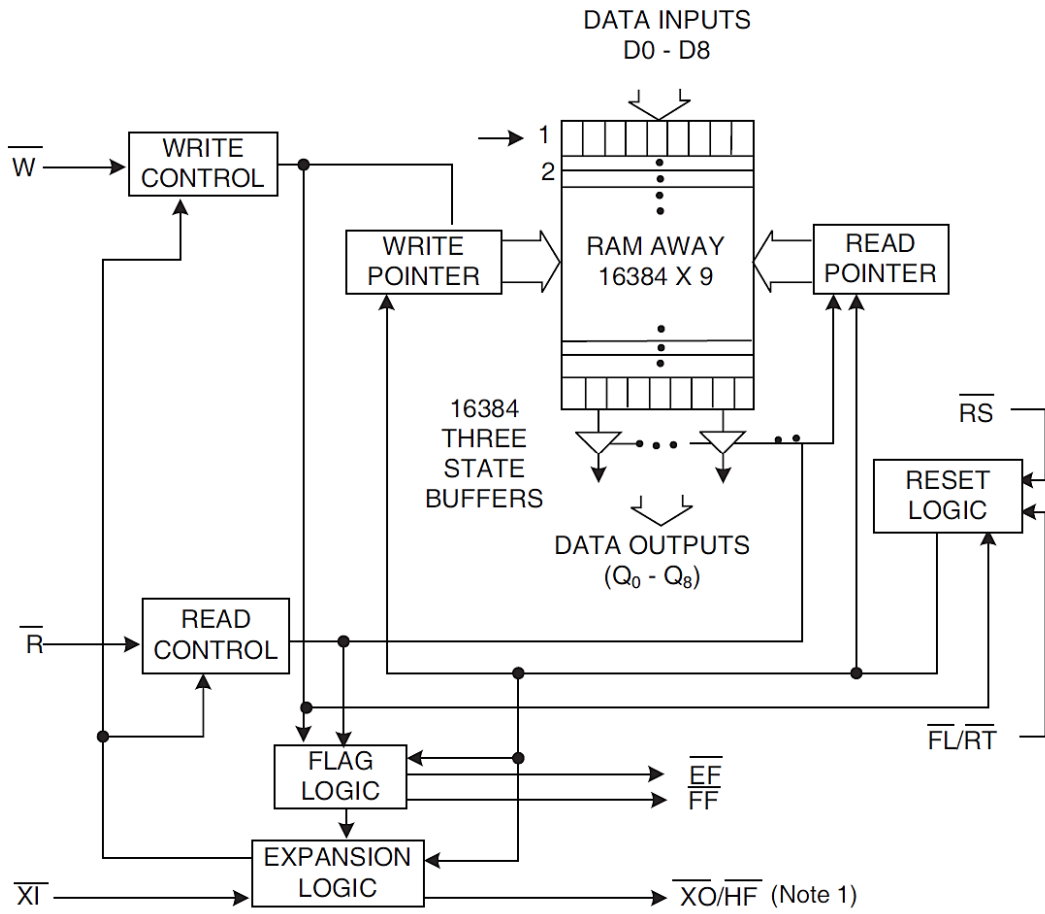
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.29	3.3	
b	0.38	0.48	2
c	0.08	0.15	2
D	-	18.8	7
E	9.65	10.67	7
E2	4.57	-	
E3	0.76	-	
e	1.27 BSC		2, 4
L	6.35	9.4	2

Symbols	Dimensions mm		Notes
	Min	Max	
Q	0.66	-	2, 9
S	-	1.3	8
S1	0	-	8

1.7.3 Notes to Physical Dimensions and Terminal Identification

1. Index mark: a notch or terminal 1 identification mark for MFP-F28 package shall be located adjacent to terminal 1 and for MDIL28 package shall be in the shaded area.
2. All terminals.
3. 26 places. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within $\pm 0.25\text{mm}$ of its true longitudinal position relative to Pin 1 and the highest pin number.
4. 26 places. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within $\pm 0.13\text{mm}$ of its true longitudinal position relative to Pin 1 and the highest pin number.
5. Dimensions are measured with the package seated in a seating plane gauge.
6. Dimensions are measured with the leads constrained to be perpendicular to the base plane.
7. This dimension allows for package edge anomalies caused by material protrusions, such as rough ceramic, misaligned ceramic layers and lids, meniscus, and glass overrun.
The corner shape (square, notch, radius etc.) may vary at the manufacturer's option from that shown on the drawing.
8. Two places.
9. Dimension shall be measured at the point of exit of the lead from the body.

1.8 FUNCTIONAL DIAGRAM



NOTES:

1. For Variants 05 to 08 the terminal symbol is $\overline{XO/PHF}$.

1.9 PIN ASSIGNMENT

Pin	Function	Pin	Function
1	\bar{W} Input (Write Enable)	15	\bar{R} Input (Read Enable)
2	D8 Input (Data)	16	Q4 Output
3	D3 Input (Data)	17	Q5 Output
4	D2 Input (Data)	18	Q6 Output
5	D1 Input (Data)	19	Q7 Output
6	D0 Input (Data)	20	\bar{XO}/\bar{HF} Output (Expansion Out/Half-full Flag) Note 1
7	\bar{XI} Input (Expansion In)	21	\bar{EF} Output (Empty Flag)
8	\bar{FF} Output (Full Flag)	22	\bar{RS} Input (Reset)
9	Q0 Output	23	\bar{FL}/\bar{RT} Input (First Load/Retransmit)
10	Q1 Output	24	D7 Input (Data)
11	Q2 Output	25	D6 Input (Data)
12	Q3 Output	26	D5 Input (Data)
13	Q8 Output	27	D4 Input (Data)
14	V_{SS}	28	V_{DD}

NOTES:

- For Variants 05 to 08 the function shall be \bar{XO}/\bar{PHF} Output (Expansion Out/Programmable Half-full Flag).

 1.10 TRUTH TABLES AND TIMING DIAGRAMS

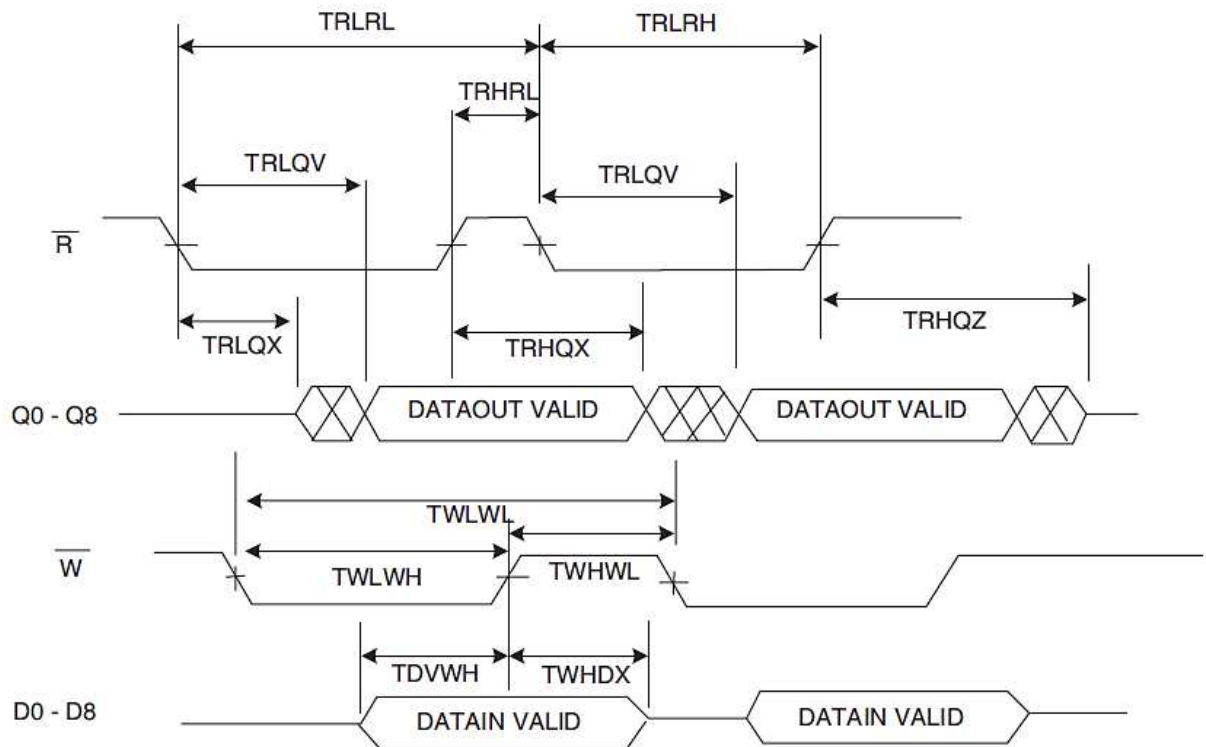
- The Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
- For Variants 05 to 08 the output symbol \bar{HF} shall be \bar{PHF} .
- Pointer will increment if flag is high.
- \bar{XI} is connected to \bar{XO} of previous device.

RESET AND RETRANSMIT TRUTH TABLE

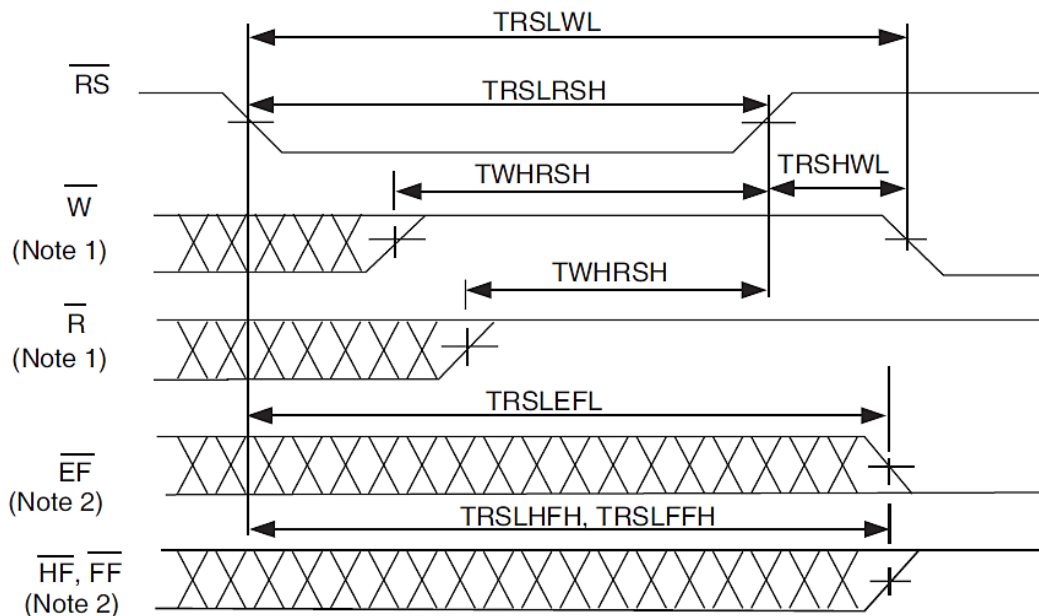
Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs (Note 2)		
	\bar{RS}	\bar{RT}	\bar{XI}	Read Pointer	Write Pointer	\bar{EF}	\bar{FF}	\bar{HF}
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	X	X	X
Read/Write	H	H	L	Increment (Note 3)	Increment (Note 3)	X	X	X

ASYNCHRONOUS WRITE AND READ OPERATION



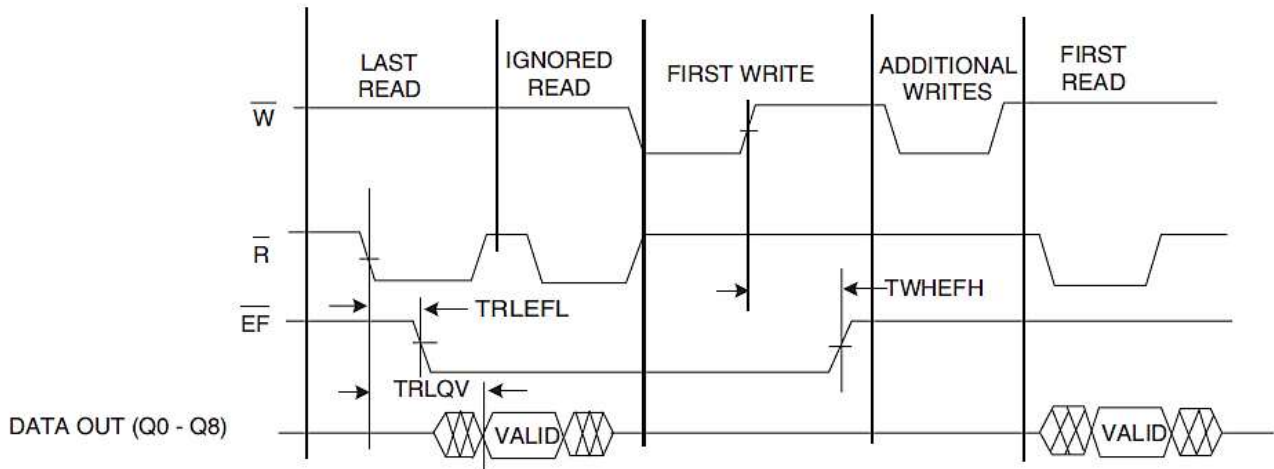
RESET TIMING



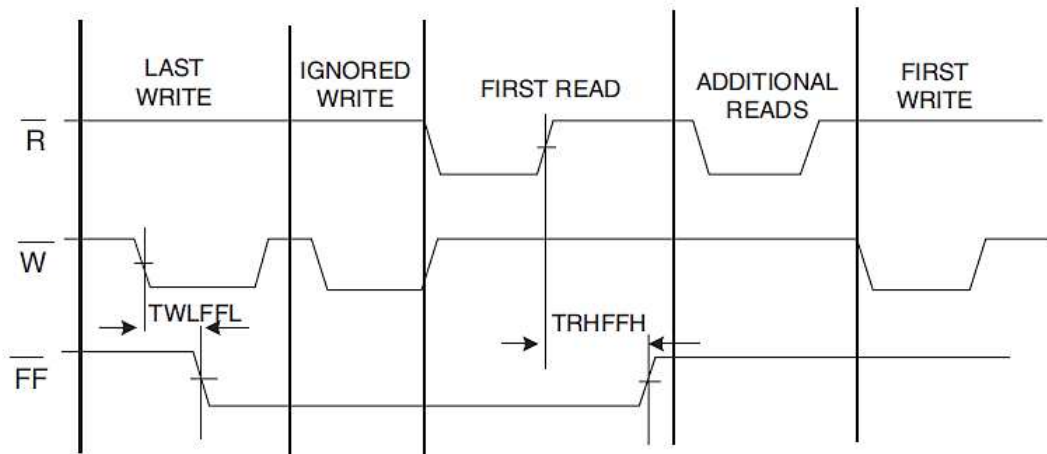
NOTES:

1. \bar{W} and $\bar{R} = V_{IH}$ around the rising edge of \bar{RS} .
2. \bar{EF} , \bar{HF} and \bar{FF} may change status during RESET, but flags will be valid at $TRSLWL$.

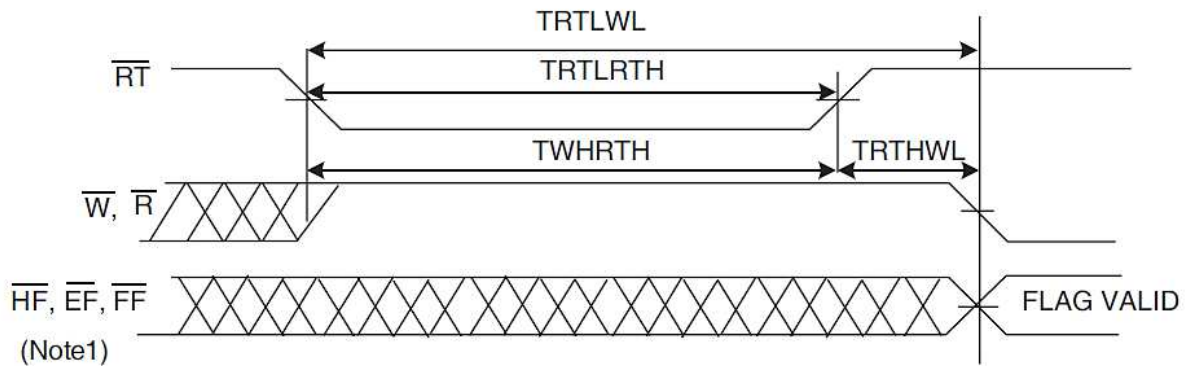
EMPTY FLAG FROM LAST READ TO FIRST WRITE



FULL FLAG FROM LAST WRITE TO FIRST READ



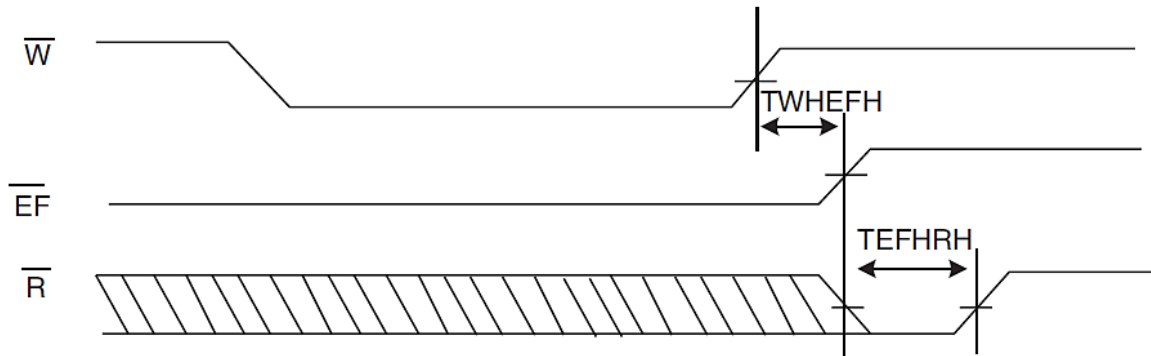
RETRANSMIT



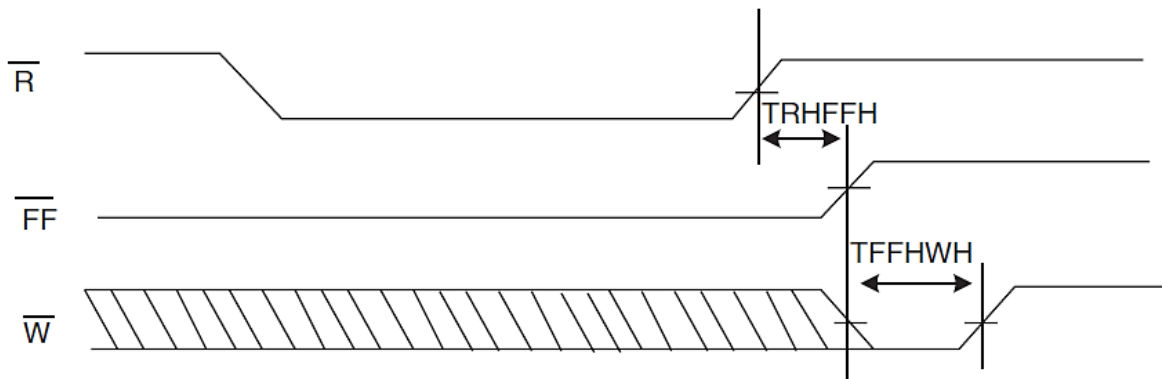
NOTES:

1. \overline{EF} , \overline{HF} and \overline{FF} may change status during Retransmit, but flags will be valid at TRTLWL. (\overline{HF} shall be \overline{PHF} for Variants 05 to 08).

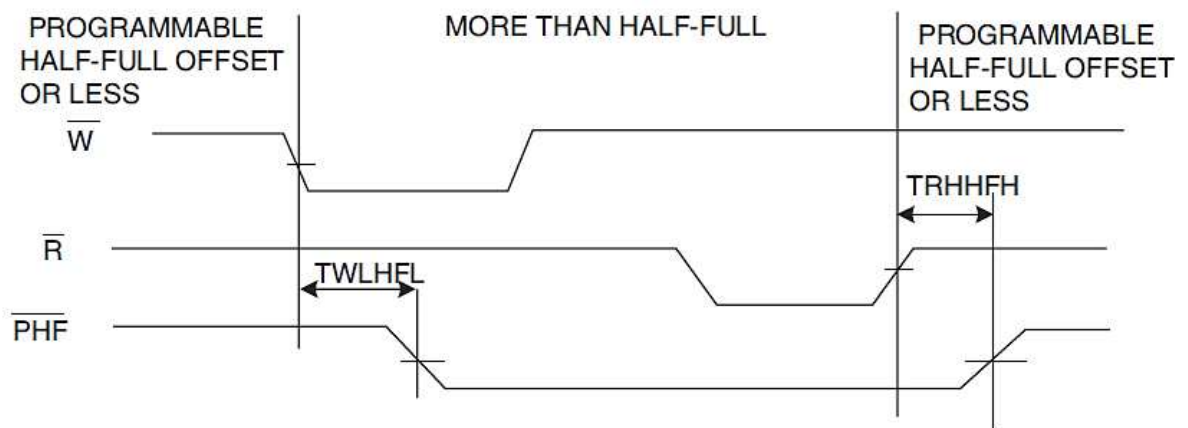
EMPTY FLAG TIMING



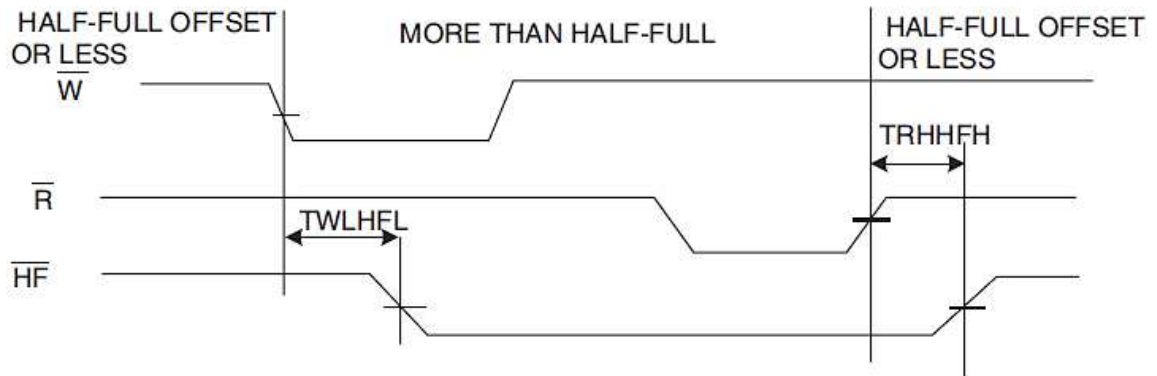
FULL FLAG TIMING



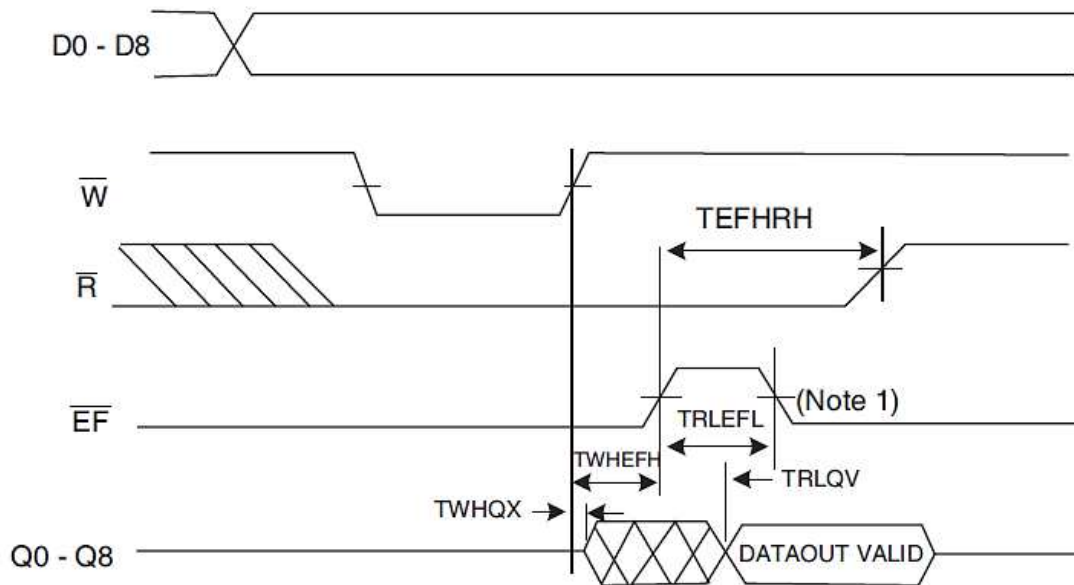
PROGRAMMABLE HALF-FULL FLAG TIMING (VARIANTS 05 TO 08)



HALF-FULL FLAG TIMING (VARIANTS 01 TO 04)



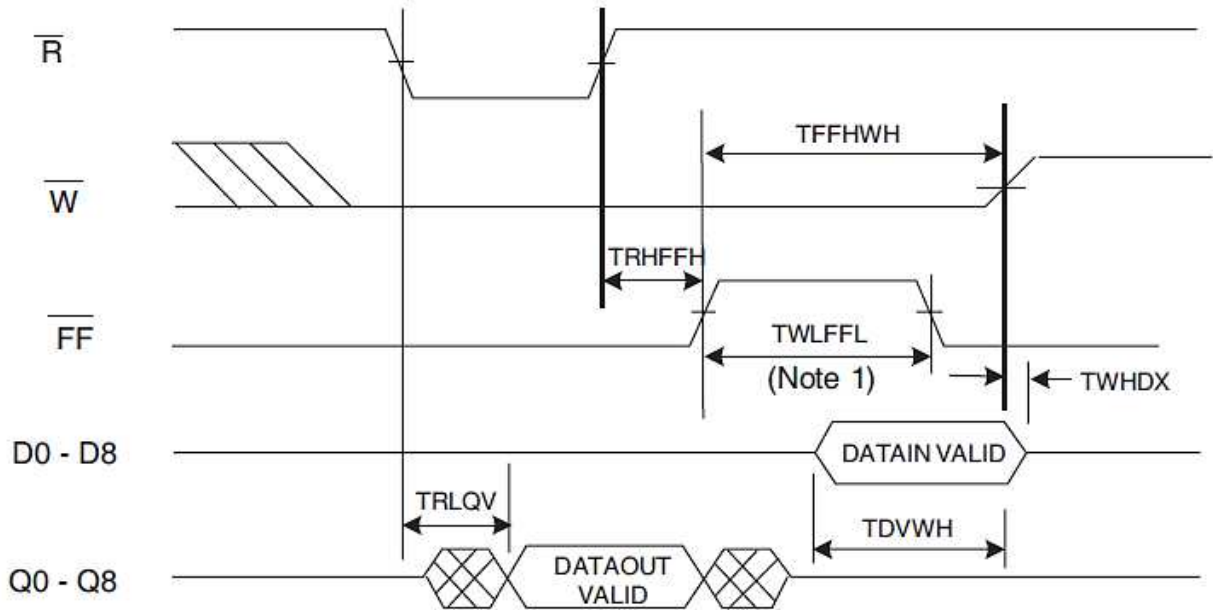
READ DATA FLOW - THROUGH MODE



NOTES:

1. For FIFO empty condition only, a read cannot begin until completion of a write. Therefore the TRLEFL reference is the rising edge of EF.

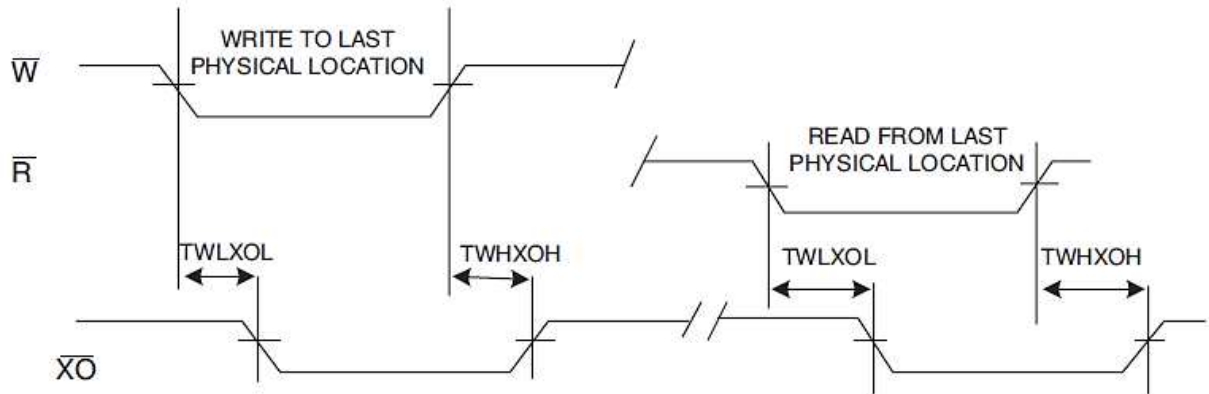
WRITE DATA FLOW - THROUGH MODE



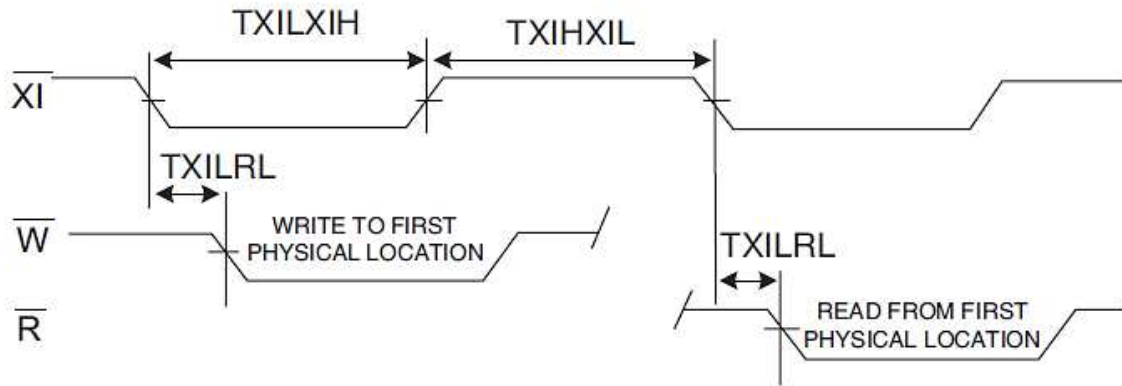
NOTES:

1. For FIFO empty condition only, a write cannot begin until completion of a read. Therefore the T_{WLFFL} reference is the rising edge of \bar{FF} .

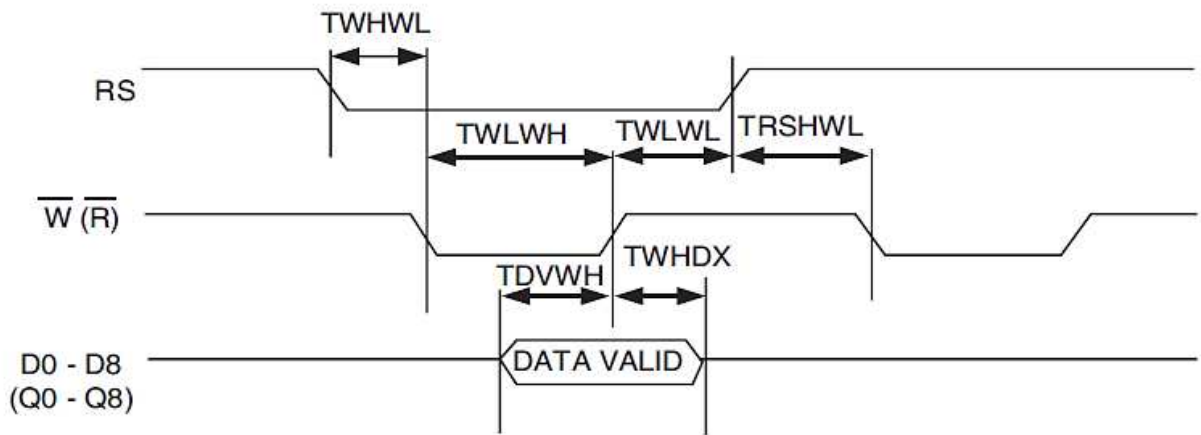
EXPANSION OUT



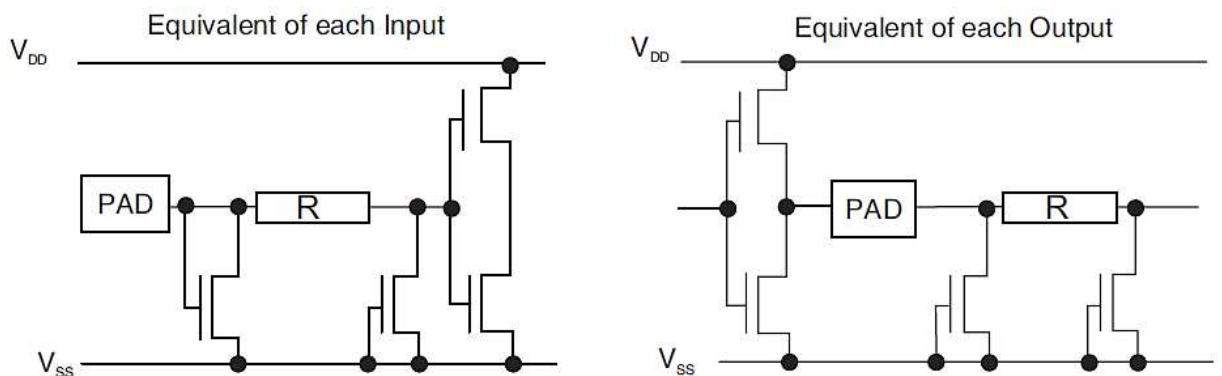
EXPANSION IN



RESET (WRITE (READ) TO PROGRAMMABLE HALF-FULL FLAG REGISTER) VARIANTS 05 TO 08 ONLY



1.11 PROTECTION NETWORKS



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}C$.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table Note 2	-	-	-
Input Clamp Voltage to V_{SS}	V_{IC}	3008	I_{IN} (Under Test) = $-200\mu A$ V_{IN} (Remaining Inputs) = 0V $V_{DD} = V_{SS} = 0V$	-0.1	-1.9	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V $V_{DD} = V_{SS} = 0V$	-	-1	μA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V $V_{DD} = 5.5V, V_{SS} = 0V$	-	1	μA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	$V_{IN}(\bar{R}) = 2.2V$ $V_{OUT} = 0V$ $V_{DD} = 5.5V, V_{SS} = 0V$	-	-1	μA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	$V_{IN}(\bar{R}) = 2.2V$ $V_{OUT} = 5.5V$ $V_{DD} = 5.5V, V_{SS} = 0V$	-	1	μA
Low Level Output Voltage	V_{OL}	3007	$V_{IL} = 0.8V, V_{IH} = 2.2V$ $I_{OL} = 8mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ Note 3	-	400	mV
High Level Output Voltage	V_{OH}	3006	$V_{IL} = 0.8V, V_{IH} = 2.2V$ $I_{OH} = -2mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ Note 3	2.4	-	V
Stand-by Supply Current	I_{DDSB}	3005	$V_{IN}(\bar{X}I) = 0V$ $V_{IN}(\bar{R}, \bar{W}, \bar{RS}, \bar{FL}/\bar{RT}) = 2.2V$ All Outputs Open $V_{DD} = 5.5V, V_{SS} = 0V$	-	5	mA
Power Down Supply Current	I_{DDPD}	3005	$V_{IN}(\bar{X}I) = 0V$ V_{IN} (Remaining Inputs) = 5.5V All Outputs Open $V_{DD} = 5.5V, V_{SS} = 0V$	-	400	μA
Dynamic Operating Supply Current	I_{DDOP}	3005	$V_{IL} = 0V, V_{IH} = 3V$ Write/Read cycle: $f_{write} = 25MHz$ (Variants 03, 04, 07, 08) and = 40MHz (Variants 01, 02, 05, 06) $f_{read} = 100MHz$ All Outputs Open $V_{DD} = 5.5V, V_{SS} = 0V$ Variants 01, 02, 05, 06 Variants 03, 04, 07, 08	-	120 110	mA
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test) = 0V $f = 1MHz$ $V_{DD} = V_{SS} = 0V$ Note 4	-	10	pF

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Capacitance	C _{OUT}	3012	V _{IN} (Not Under Test) = 0V f = 1MHz V _{DD} = V _{SS} = 0V Note 4	-	10	pF
Read Pulse Low to Data Bus, Low Impedance	t _{RLQX}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 4	0	-	ns
Write Pulse High to Data Bus, Low Impedance	t _{WHQX}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 4 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	5 3	- -	ns
Read Pulse High to Data Bus, High Impedance	t _{RHQZ}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 4 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	20 15	ns
Retransmit Set-up Time	t _{WHRTH}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 4 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns
Reset to Empty Flag Low	t _{RSLEFL}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 4 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 25	ns
Read/Write High to Expansion Out High	t _{WHXOH}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 4 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 15	ns
Read Cycle Time	t _{RLRL}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 5 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	40 25	- -	ns
Access Time	t _{RLQV}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 5 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 15	ns
Data Set-up Time	t _{DVWH}	3003	V _{DD} = 4.5V & 5.5V V _{SS} = 0V Note 5 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	18 9	- -	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Data Hold Time	t_{WHDX}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 5	0	-	ns
Read Low to Empty Flag Low	t_{RLEFL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 5 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 25	ns
Write High to Empty Flag High	t_{WHEFH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 5 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 15	ns
Read High to Full Flag High	t_{RHFFH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 5 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 25	ns
Write Low to Full Flag Low	t_{WLFFL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 5 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 20	ns
Write Low to Half- full Flag Low	t_{WLHFL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 5	-	30	ns
Read Recovery Time	t_{RHRL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	10	-	ns
Read Pulse Width	t_{RLRH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns
Data Valid from Read Pulse High	t_{RHQX}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	5	-	ns
Write Cycle Time	t_{WLWL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	40 25	- -	ns
Write Pulse Width	t_{WLWH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Write Recovery Time	t_{WHWL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	10	-	ns
Reset Cycle	t_{RSLWL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	40 25	- -	ns
Reset Pulse Width	t_{RSLRSH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns
Reset Set-up Time	t_{WHRSH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 20	- -	ns
Reset Recovery Time	t_{RSHWL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	10	-	ns
Retransmit Cycle Time	t_{RTLWL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	40 25	- -	ns
Retransmit Pulse Width	t_{RTLRTH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns
Retransmit Recovery Time	t_{RTHWL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	10	-	ns
Reset to Half-full Flag High	t_{RSLHFH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 25	ns
Reset to Full Flag High	t_{RSLFFH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 25	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Read Pulse Width after Empty Flag High	t_{EFHRH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns
Read High to Half- full Flag High	t_{RHFFH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	-	30	ns
Write Pulse Width after Full Flag High	t_{FFHWH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns
Read/Write Low to Expansion Out Low	t_{WLXOL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	- -	30 15	ns
Expansion In Pulse Width	t_{XILXIH}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6 Variants 03, 04, 07, 08 Variants 01, 02, 05, 06	30 15	- -	ns
Expansion In Recovery Time	t_{XIHXL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	10	-	ns
Expansion In Set-up Time	t_{XILRL}	3003	$V_{DD} = 4.5V \text{ \& } 5.5V$ $V_{SS} = 0V$ Note 6	10	-	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional go-no-go test with the following test sequences:

FUNCTIONAL TEST 1

Pattern	Timing (ns) Note (a)	V _{DD} (V)	V _{SS} (V)	V _{IL} (V)	V _{IH} (V)	I _{OL} (mA)	I _{OH} (mA)	V _{out comp} (V) Note (b)
WRT-RD000	175	4.5 & 5.5	0	0	3	8	-2	1.5
WRT-RD1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-000	175	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-155	175	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-000	175	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-155	175	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
ADDRESS	175	4.5 & 5.5	0	0	3	8	-2	1.5
CKBD-000	175	4.5 & 5.5	0	0	3	8	-2	1.5
CKBD-1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
FLAGS	175	4.5 & 5.5	0	0	3	8	-2	1.5
Xi	175	4.5 & 5.5	0	0	3	8	-2	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns) Note (a)	V _{DD} (V)	V _{SS} (V)	V _{IL} (mV)	V _{IH} (V)	I _{OL} (mA)	I _{OH} (mA)	V _{out comp} (V) Note (b)
WRITE/READ000	175	4.5	0	800	4.5	8	-2	1.5
WRITE/READ000	175	5.5	0	0	2.2	8	-2	1.5
FLAGS	175	4.5	0	800	4.5	8	-2	1.5
FLAGS	175	5.5	0	0	2.2	8	-2	1.5
Xi	175	4.5	0	800	4.5	8	-2	1.5
Xi	175	5.5	0	0	2.2	8	-2	1.5

FUNCTIONAL TEST 3

Pattern	Timing (ns) Note (a)		V _{DD} (V)	V _{SS} (V)	V _{IL} (V)	V _{IH} (V)	I _{OL} (mA)	I _{OH} (mA)	V _{out comp} (V) Note (b)
	Variants 01, 02, 05, 06	Variants 03, 04, 07, 08							
MARCH-000	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-155	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-1FF	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-000	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-155	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-1FF	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FLAGS	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
Xi	25	40	4.5 & 5.5	0	0	3	8	-2	1.5

- (a) $t_r = t_f \leq 5\text{ns}$
- (b) Output Load = 1 TTL gate equivalent + $C_L < 100\text{pF}$
- 3. Measurements shall be performed using MARCH-000 and MARCH-1FF test patterns.
- 4. Guaranteed but not tested. Characterised at initial design and after major process changes.
- 5. Measurements shall be performed during Functional Test 3 using the following test patterns:
 - For t_{RLRL} and t_{RLQV} MARCH-000
 - For t_{DVWH} and t_{WHDx} FIFO-1FF
 - For t_{RLEFL} , t_{WHEFH} , t_{RHFFH} ,
 t_{WLFFL} and t_{WLHFL} FLAGS
- 6. Measurements shall be performed, on a go-no-go basis, during Functional Test 3.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at $T_{amb} = +125 (+0 -5)^\circ\text{C}$ and $T_{amb} = -55 (+5 -0)^\circ\text{C}$.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}C$.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics (Note 1)	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	± 0.1	-	-1	μA
High Level Input Current	I_{IH}	± 0.1	-	1	μA
Output Leakage Current, Third State, Low Level Applied	I_{OZL}	± 0.1	-	-1	μA
Output Leakage Current, Third State, High Level Applied	I_{OZH}	± 0.1	-	1	μA
Low Level Output Voltage	V_{OL}	± 100	-	400	mV
High Level Output Voltage	V_{OH}	± 0.1	2.4	-	V
Stand-by Supply Current	I_{DDBS}	± 0.5	-	5	mA
Power Down Supply Current	I_{DDPD}	± 40	-	400	μA

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3^{\circ}C$.

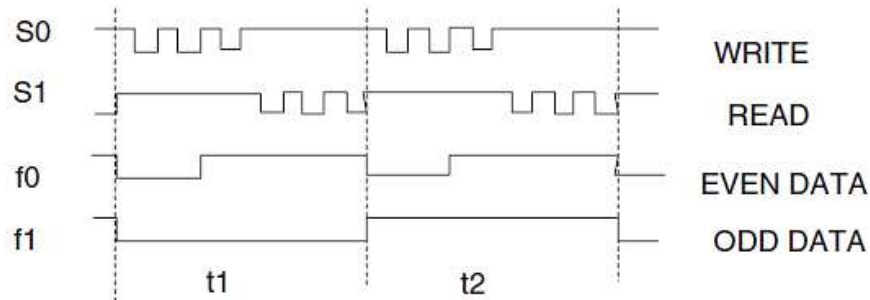
The test methods, test conditions and limits shall be as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs \overline{FF} , Q_n , $\overline{XO}/\overline{HF}$ (PHF), \overline{EF}	V_{OUT}	V_{SS}	V
Inputs \overline{RS} , $\overline{FL}/\overline{RT}$	V_{IN}	V_{DD}	V
Input \overline{XI}	V_{IN}	V_{SS}	V
Input \overline{W}	V_{IN}	S0 (Note 1)	V
Input \overline{R}	V_{IN}	S1 (Note 1)	V
Inputs D0, D2, D4, D6, D8	V_{IN}	V_{GEN0} (Note 1)	V
Inputs D1, D3, D5, D7	V_{IN}	V_{GEN1} (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN0} f_{GEN1}	275k \pm 20% 137.5k \pm 20% 50 \pm 15% Duty Cycle Note 1	Hz
Positive Supply Voltage	V_{DD}	5 (+0.5 -0)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

- Input waveforms to indicate required timing and phase relationships:



- $t1 = t2 = 3.6\mu s$.
- Input Protection Resistor = Output Load = 1k Ω .

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during radiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ±3	°C
Outputs \overline{FF} , Q_n , \overline{XO}/HF (PHF), \overline{EF}	V_{OUT}	Open	V
Inputs D_n , \overline{W} , \overline{XI} , \overline{FL}/RT , \overline{R}	V_{IN}	V_{DD}	V
Input \overline{RS}	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	5 ±0.1	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = 1kΩ.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of radiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at $T_{amb} = +22 \pm 3^\circ\text{C}$.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.