INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS STATIC 4K X 9BIT, PARALLEL FIRST IN FIRST OUT MEMORY WITH THREE STATE OUTPUTS

BASED ON TYPE 67204H

ESCC Detail Specification No. 9301/049

Issue 2	August 2015

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
936	Specification upissued to incorporate editorial changes per DCR.

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930104901P

- Detail Specification Reference: 9301049
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: P (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Access Time (ns)	Case	Lead/Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	67204H-15	15	MDIL28	G2	3.5	P [30kRAD(Si)]
02	67204H-15	15	MFP-F28	G2	3	P [30kRAD(Si)]
03	67204H-15	30	MDIL28	G2	3.5	P [30kRAD(Si)]
04	67204H-15	30	MFP-F28	G2	3	P [30kRAD(Si)]

The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 7	V	Note 1
Input Voltage Range	V_{IN}	-0.5 to V_{DD}+0.3	V	Notes 1, 2
Output Voltage Range	V_{OUT}	-0.5 to V_{DD}+0.3	V	Notes 1, 2
Output Current into Outputs (Low)	I_{OUT}	50	mA	Note 3
Maximum Device Power Dissipation	P_D	1	W	
Operating Temperature	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature	T_{stg}	-65 to +150	°C	
Soldering Temperature	T_{sol}	+265	°C	Note 4
Junction Temperature	T_j	+150	°C	Note 5
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	3	°C/W	

NOTES:

1. Device is functional for $4.5 \leq V_{DD} \leq 5.5$ with reference to V_{SS} = 0V.
2. V_{DD}+0.3V shall not exceed 7V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
5. Maximum junction temperature may be increased to +175°C during Power Burn-in and Operating Life.

1.6 HANDLING PRECAUTIONS

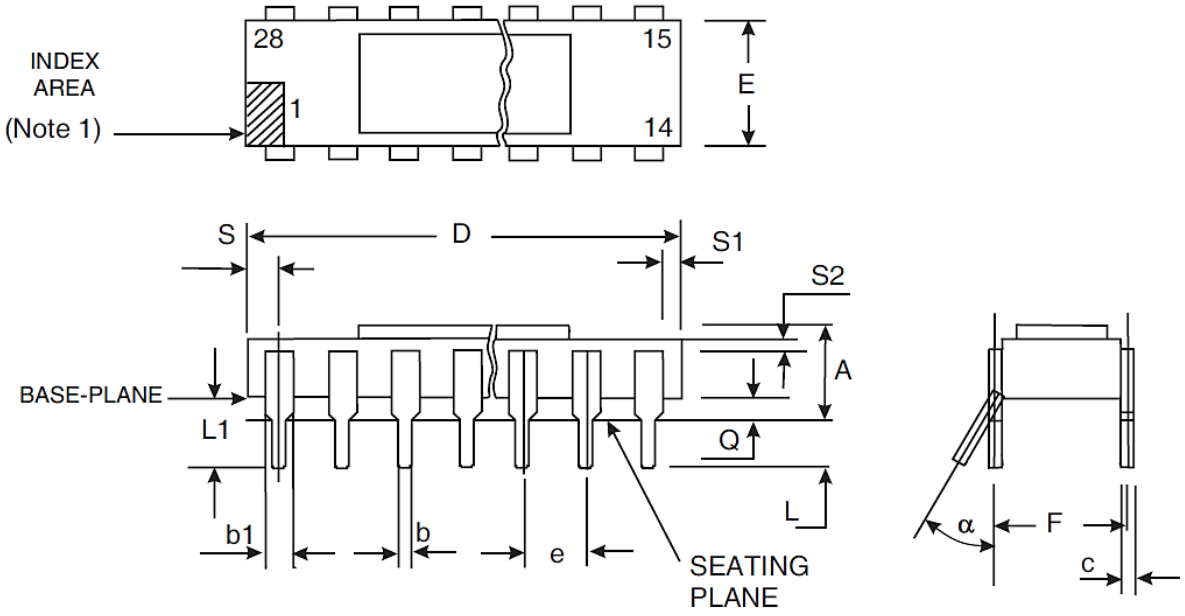
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

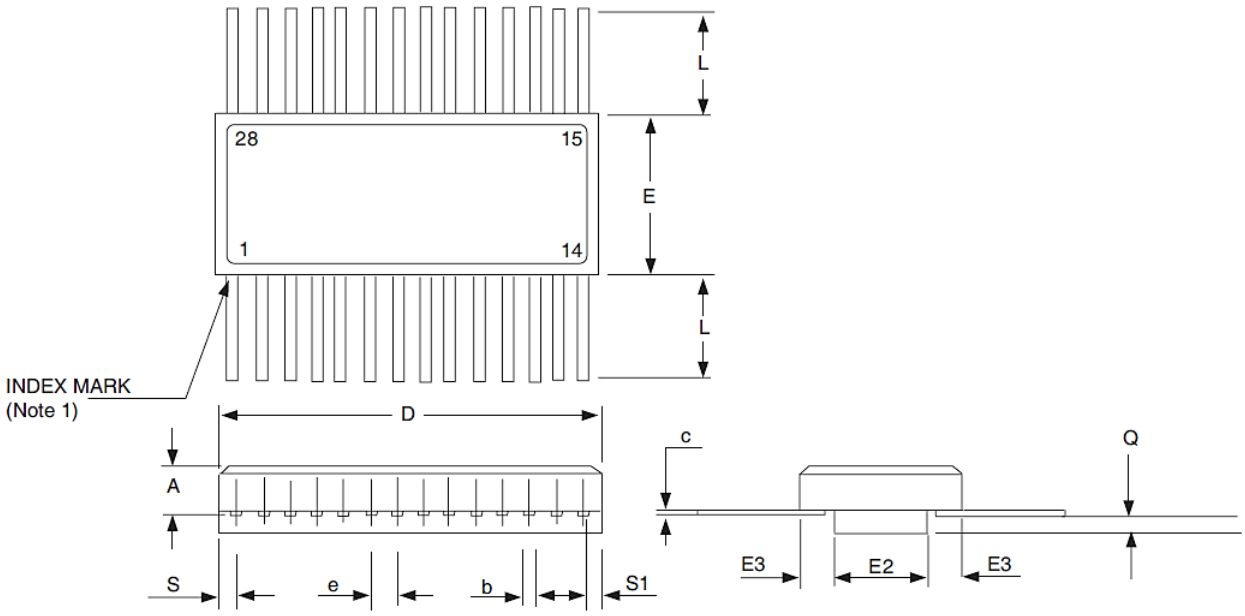
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Multilayer Ceramic Dual-in-Line Package (MDIL28) - 28 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	3.3	5.84	5
b	0.36	0.58	2
b1	0.96	1.65	2
c	0.2	0.38	2
D	-	37.72	
E	6.1	7.87	
F	7.37	8.13	6
e	2.54 BSC		2, 3
L	2.92	5.08	2, 5
L1	3.3	-	2
Q	0.38	2.54	5
S	-	2.54	8
S1	0.13	-	8
S2	0.13	-	2
α	0°	15°	2

1.7.2 Flat Leaded Multilayer Flat Package (MFP-F28) - 28 Lead



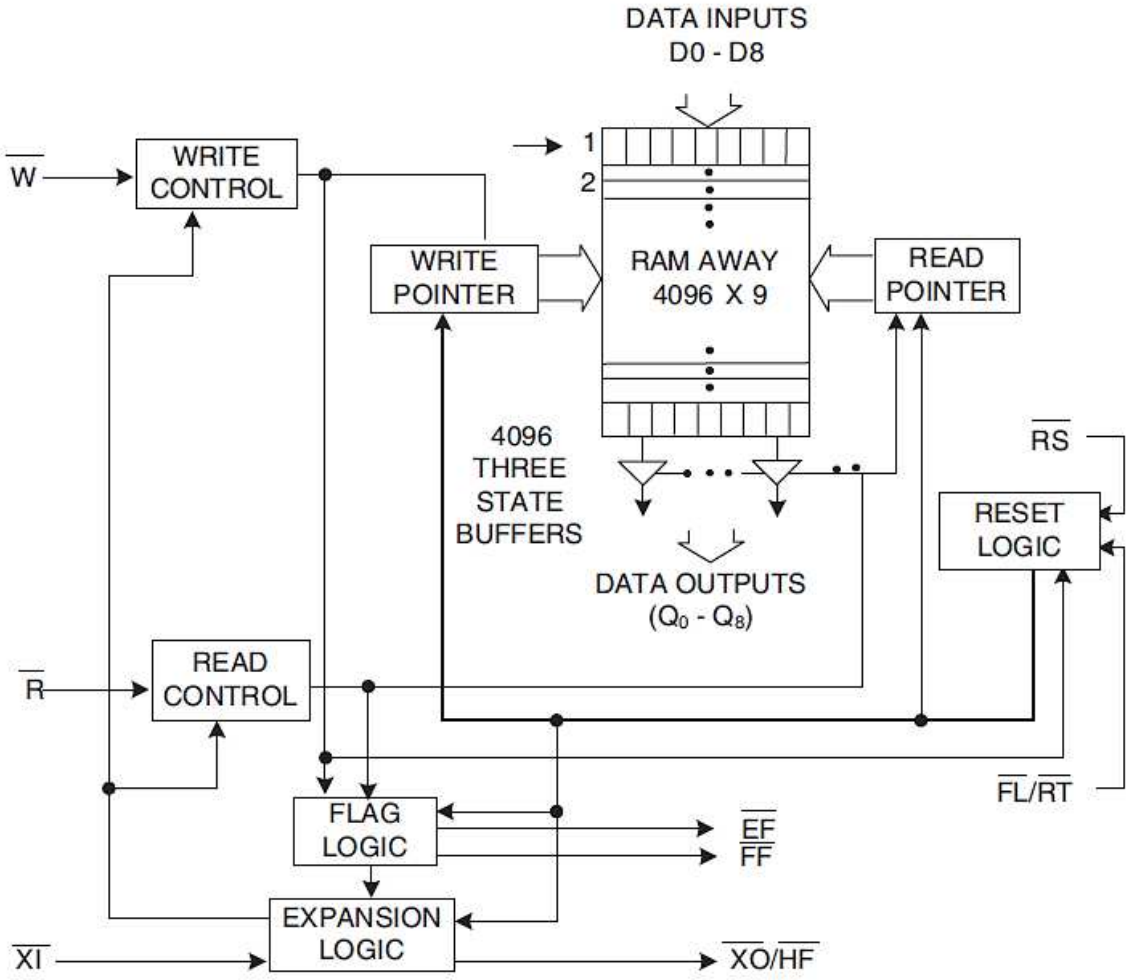
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.29	3.3	
b	0.38	0.48	2
c	0.08	0.15	2
D	-	18.8	7
E	9.65	10.67	7
E2	4.57	-	
E3	0.76	-	
e	1.27 BSC		2, 4
L	6.35	9.4	2
Q	0.66	-	2, 9
S	-	1.3	8
S1	0	-	8

1.7.3 Notes to Physical Dimensions and Terminal Identification

1. Index mark: a notch or terminal 1 identification mark for MFP-F28 package shall be located adjacent to terminal 1 and for MDIL28 package shall be in the shaded area.
2. All terminals.
3. 26 places. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.

4. 26 places. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. Dimensions are measured with the package seated in a seating plane gauge.
6. Dimensions are measured with the leads constrained to be perpendicular to the base plane.
7. This dimension allows for package edge anomalies caused by material protrusions such as rough ceramic, misaligned ceramic layers and lids, meniscus, and glass overrun.
   The corner shape (square, notch, radius etc.) may vary at the manufacturer's option from that shown on the drawing.
8. Two places.
9. Dimension shall be measured at the point of exit of the lead from the body.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Function	Pin	Function
1	$\overline{W}$ Input (Write Enable)	15	$\overline{R}$ Input (Read Enable)
2	D8 Input (Data)	16	Q4 Output
3	D3 Input (Data)	17	Q5 Output
4	D2 Input (Data)	18	Q6 Output
5	D1 Input (Data)	19	Q7 Output
6	D0 Input (Data)	20	$\overline{XO}/\overline{HF}$ Output (Expansion Out/Half-full Flag)
7	$\overline{XI}$ Input (Expansion In)	21	$\overline{EF}$ Output (Empty Flag)
8	$\overline{FF}$ Output (Full Flag)	22	$\overline{RS}$ Input (Reset)
9	Q0 Output	23	$\overline{FL}/\overline{RT}$ Input (First Load/Retransmit)
10	Q1 Output	24	D7 Input (Data)
11	Q2 Output	25	D6 Input (Data)
12	Q3 Output	26	D5 Input (Data)
13	Q8 Output	27	D4 Input (Data)
14	V_{SS}	28	V_{DD}

1.10 TRUTH TABLES AND TIMING DIAGRAMS

1. The Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
2. Pointer will increment if flag is high.
3. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

RESET AND RETRANSMIT TRUTH TABLE

Single Device Configuration/Width Expansion Mode

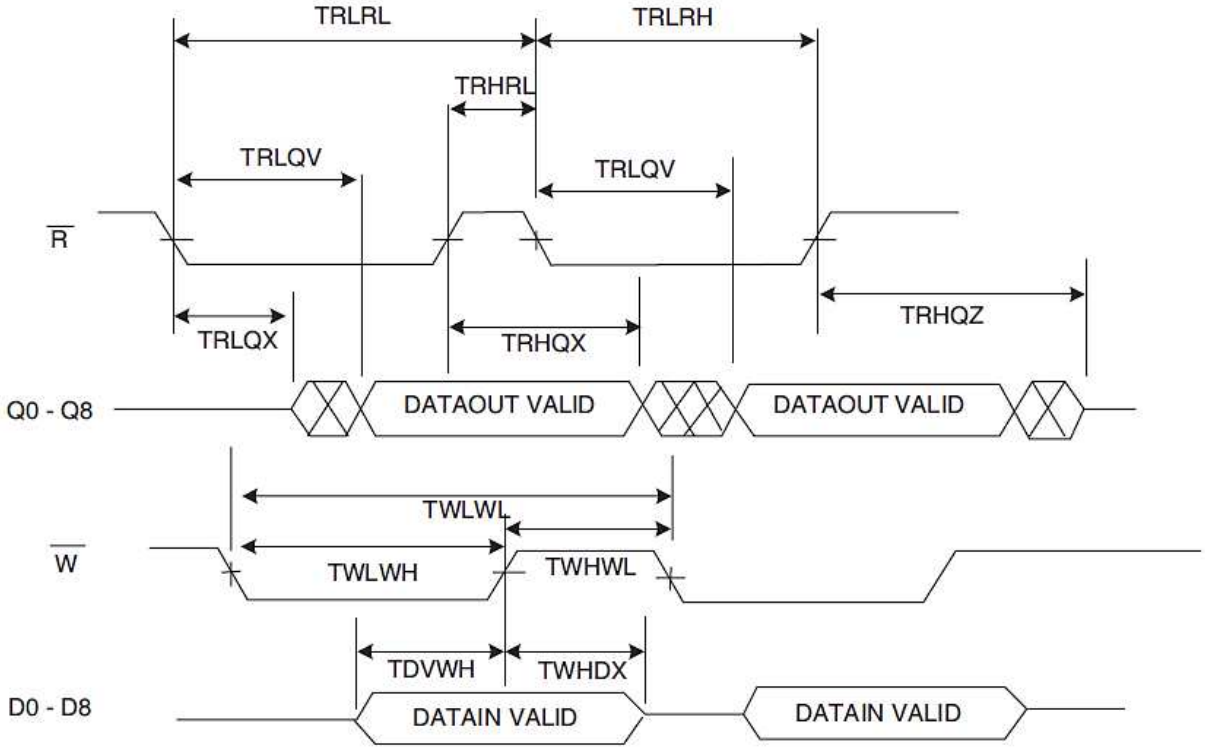
Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	X	X	X
Read/Write	H	H	L	Increment (Note 2)	Increment (Note 2)	X	X	X

RESET AND FIRST LOAD TRUTH TABLE

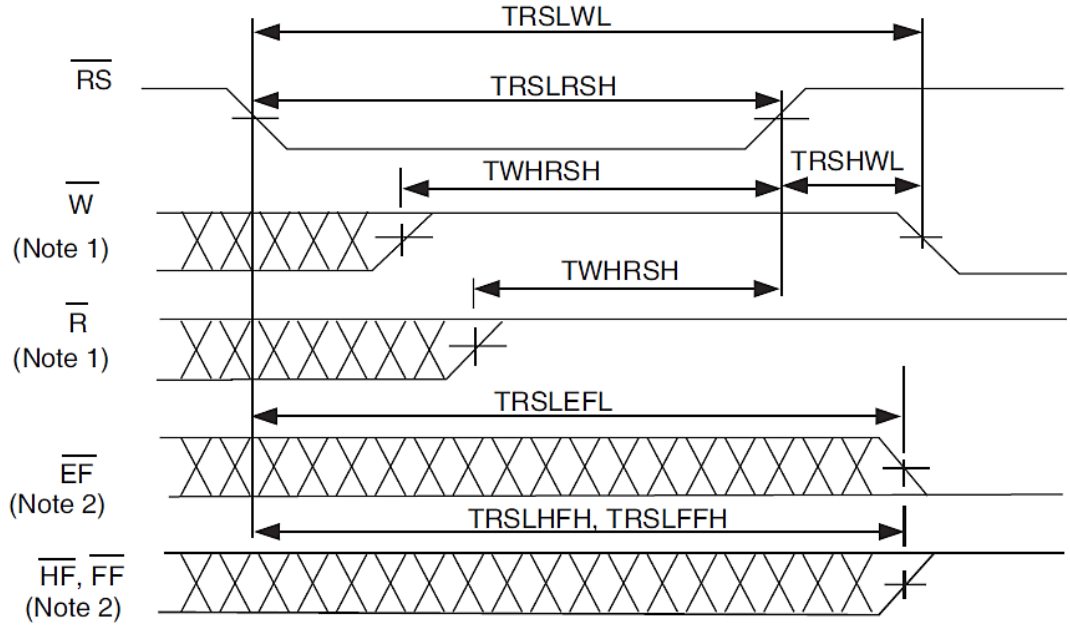
Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	L	L	Note 3	Location Zero	Location Zero	L	H
Reset All Other Devices	L	H	Note 3	Location Zero	Location Zero	L	H
Read/Write	H	X	Note 3	X	X	X	X

ASYNCHRONOUS WRITE AND READ OPERATION



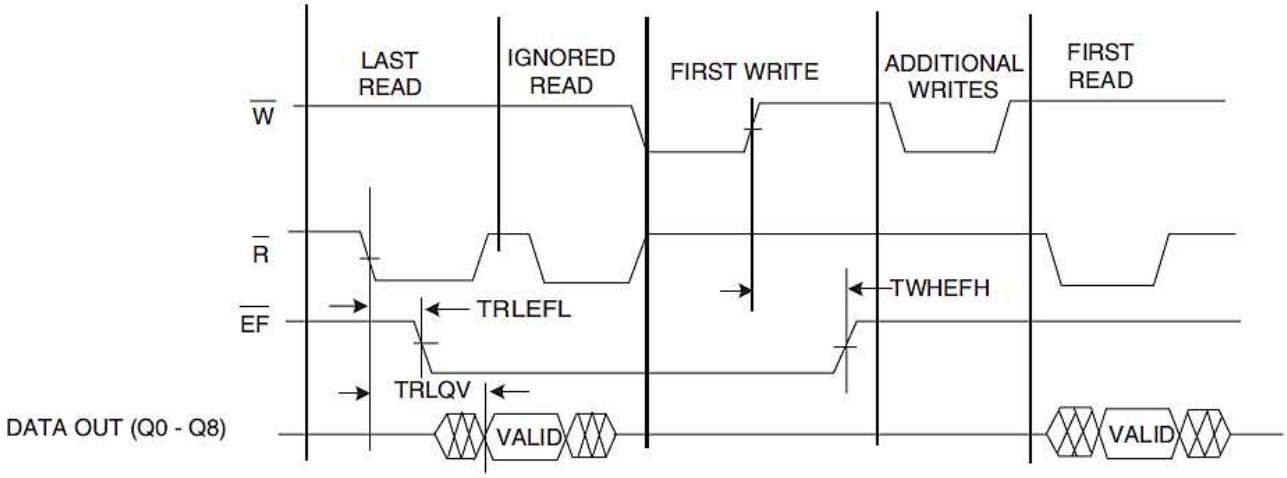
RESET TIMING



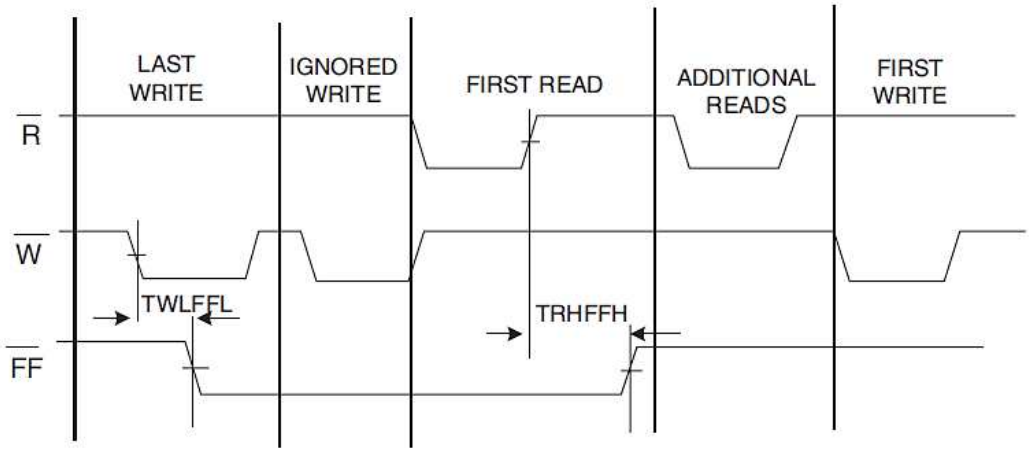
NOTES:

1. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change status during RESET, but flags will be valid at TRSLWL.

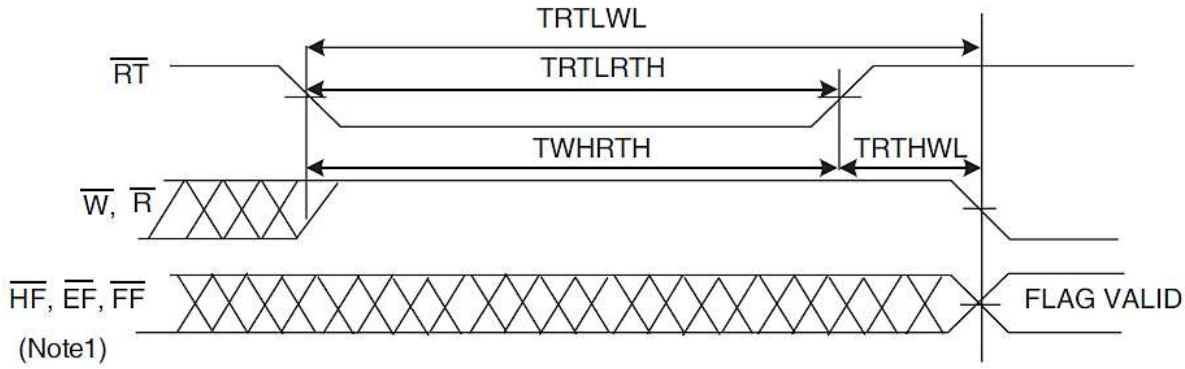
EMPTY FLAG FROM LAST READ TO FIRST WRITE



FULL FLAG FROM LAST WRITE TO FIRST READ



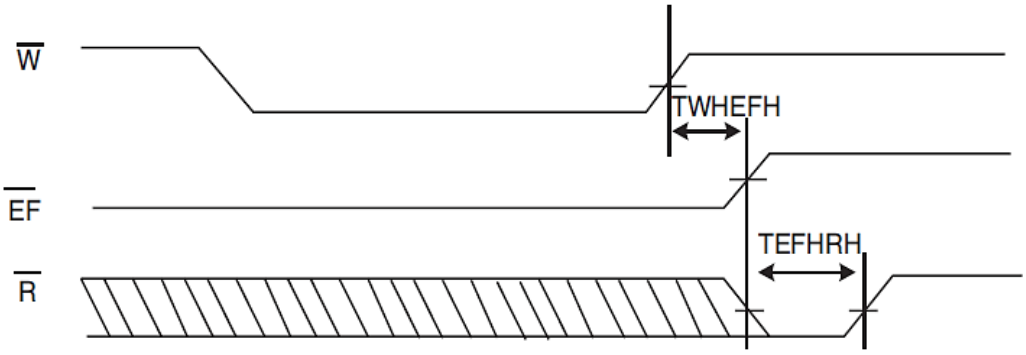
RETRANSMIT



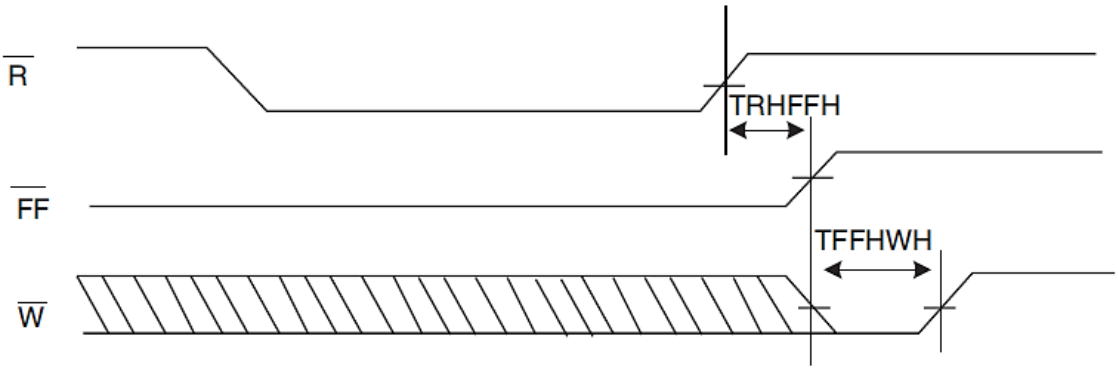
NOTES:

1. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at TRTLWL.

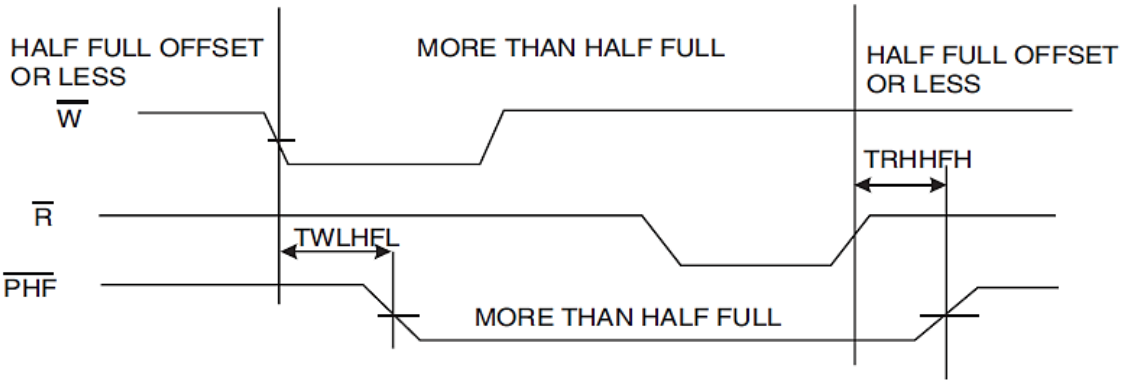
EMPTY FLAG TIMING



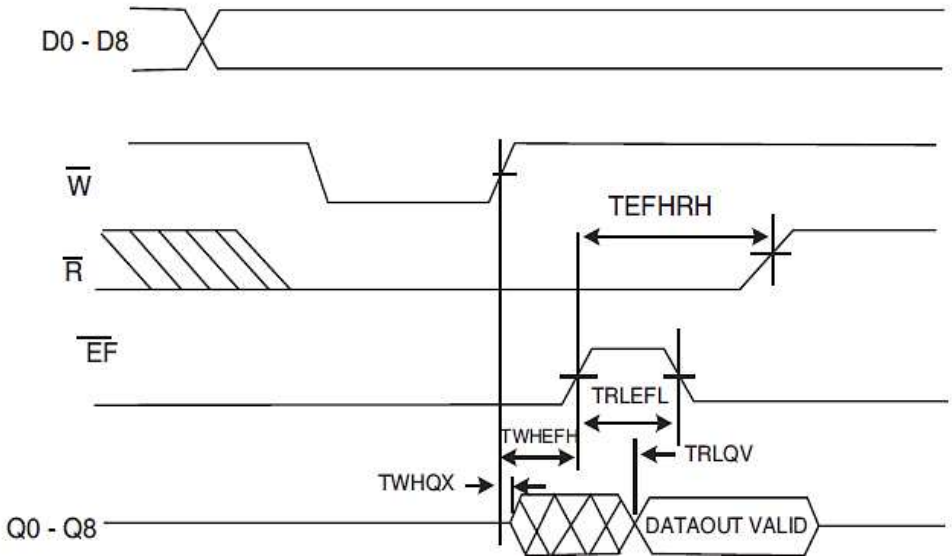
FULL FLAG TIMING



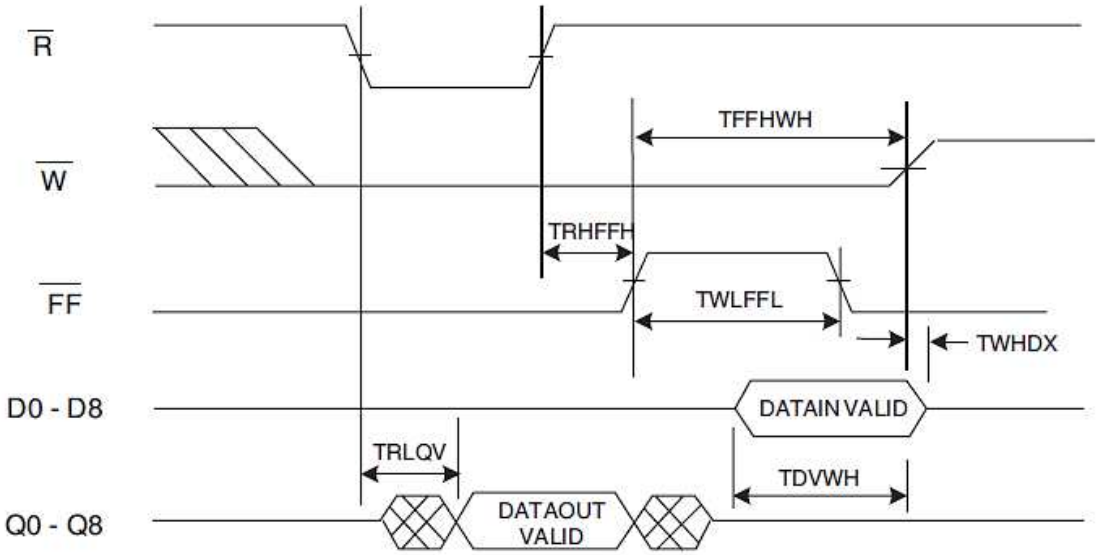
HALF-FULL FLAG TIMING



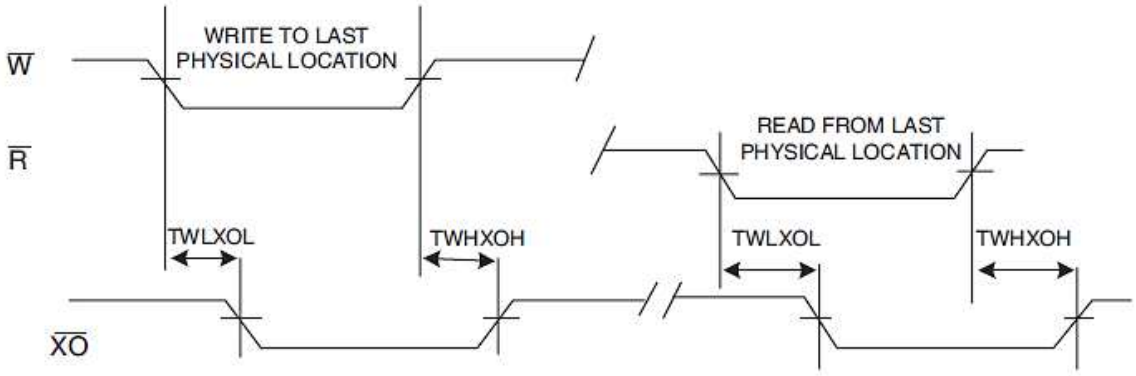
READ DATA FLOW - THROUGH MODE



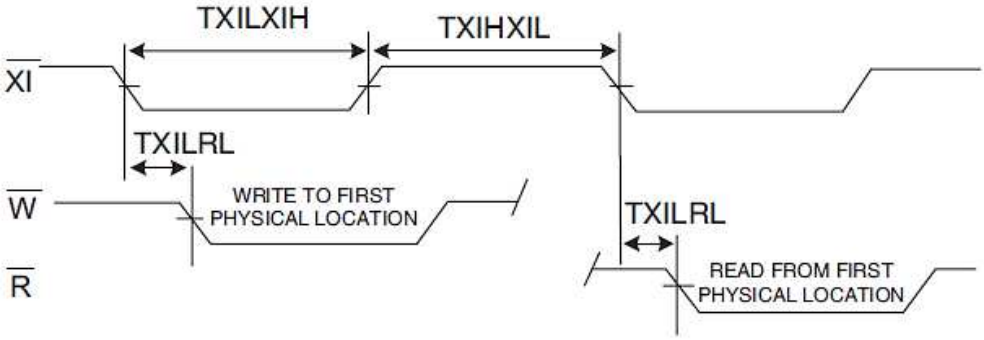
WRITE DATA FLOW - THROUGH MODE



EXPANSION OUT

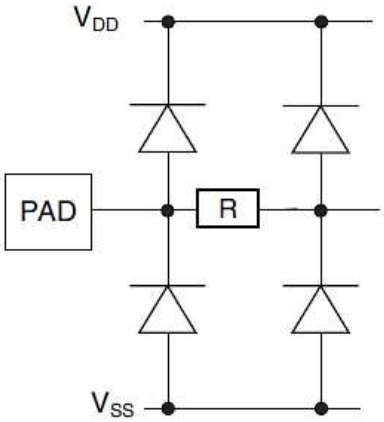


EXPANSION IN

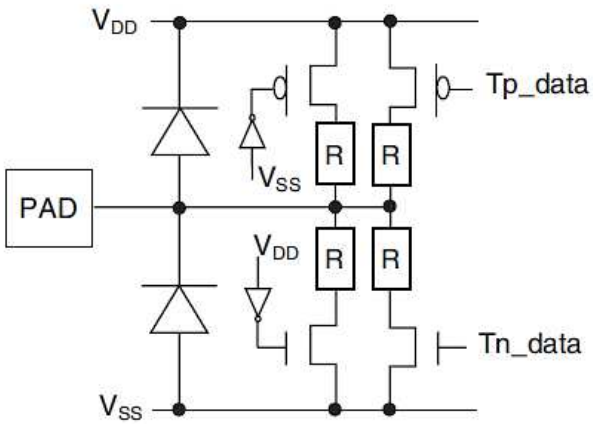


1.11 PROTECTION NETWORKS

Equivalent of Each Input



Equivalent of Each Output



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table Note 2	-	-	-
Input Clamp Voltage to V_{SS}	V_{IC}	3008	I_{IN} (Under Test) = -200µA V_{IN} (Remaining Inputs) = 0V $V_{DD} = V_{SS} = 0V$	-0.1	-1.9	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V	-	-1	µA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V	-	1	µA
Output Leakage Current, Third State, Low Level Applied	I_{OZL}	3020	V_{IN} ($\overline{R}$) = 2.2V V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V	-	-1	µA
Output Leakage Current, Third State, High Level Applied	I_{OZH}	3021	V_{IN} ($\overline{R}$) = 2.2V V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V	-	1	µA
Low Level Output Voltage	V_{OL}	3007	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = 8mA V_{DD} = 4.5V, V_{SS} = 0V Note 3	-	400	mV
High Level Output Voltage	V_{OH}	3006	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OH} = -2mA V_{DD} = 4.5V, V_{SS} = 0V Note 3	2.4	-	V
Stand-by Supply Current	I_{DDSB}	3005	V_{IN} ($\overline{XI}$) = 0V V_{IN} ($\overline{R}$, $\overline{W}$, $\overline{RS}$, $\overline{FL}$/$\overline{RT}$) = 2.2V All Outputs Open V_{DD} = 5.5V, V_{SS} = 0V	-	5	mA
Power Down Supply Current	I_{DDPD}	3005	V_{IN} ($\overline{XI}$) = 0V V_{IN} (Remaining Inputs) = 5.5V All Outputs Open V_{DD} = 5.5V, V_{SS} = 0V	-	400	µA
Dynamic Operating Supply Current	I_{DDOP}	3005	V_{IL} = 0V, V_{IH} = 3V Write/Read cycle: f_{read} = f_{write} = 40MHz (Variants 01, 02) and = 25MHz (Variants 03, 04) All Outputs Open V_{DD} = 5.5V, V_{SS} = 0V Variants 01, 02 Variants 03, 04	 - -	 120 110	mA
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test) = 0V f = 1MHz V_{DD} = V_{SS} = 0V Note 4	-	8	pF

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Capacitance	C_{OUT}	3012	V_{IN} (Not Under Test) = 0V f = 1MHz V_{DD} = V_{SS} = 0V Note 4	-	12	pF
Read Pulse Low to Data Bus Low Impedance	t_{RLQX}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 4 Variants 01, 02 Variants 03, 04	 0 5	 - -	ns
Write Pulse High to Data Bus Low Impedance	t_{WHQX}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 4 Variants 01, 02 Variants 03, 04	 3 5	 - -	ns
Read Pulse High to Data Bus High Impedance	t_{RHQZ}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 4 Variants 01, 02 Variants 03, 04	 - -	 15 20	ns
Retransmit Set-up Time	t_{WHRTH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 4 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Reset to Empty Flag Low	t_{RSLEFL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 4 Variants 01, 02 Variants 03, 04	 - -	 25 30	ns
Read/Write High to Expansion Out High	t_{WHXOH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 4 Variants 01, 02 Variants 03, 04	 - -	 15 30	ns
Read Cycle Time	t_{RLRL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5 Variants 01, 02 Variants 03, 04	 25 40	 - -	ns
Access Time	t_{RLQV}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5 Variants 01, 02 Variants 03, 04	 - -	 15 30	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Data Set-up Time	t_{DVWH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5 Variants 01, 02 Variants 03, 04	 9 18	 - -	ns
Data Hold Time	t_{WHDX}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5	0	-	ns
Read Low to Empty Flag Low	t_{RLEFL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5 Variants 01, 02 Variants 03, 04	 - -	 25 30	ns
Write High to Empty Flag High	t_{WHEFH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5 Variants 01, 02 Variants 03, 04	 - -	 15 30	ns
Read High to Full Flag High	t_{RHFFH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5 Variants 01, 02 Variants 03, 04	 - -	 25 30	ns
Write Low to Full Flag Low	t_{WLFFL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5 Variants 01, 02 Variants 03, 04	 - -	 20 30	ns
Write Low to Half-full Flag Low	t_{WLHFL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 5	-	30	ns
Read Recovery Time	t_{RHRL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	10	-	ns
Read Pulse Width	t_{RLRH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Data Valid from Read Pulse High	t_{RHQX}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	5	-	ns
Write Cycle Time	t_{WLWL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 25 40	 - -	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Write Pulse Width	t_{WLWH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Write Recovery Time	t_{WHWL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	10	-	ns
Reset Cycle	t_{RSLWL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 25 40	 - -	ns
Reset Pulse Width	t_{RSLRSH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Reset Set-up Time	t_{WHRSH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 20 30	 - -	ns
Reset Recovery Time	t_{RSHWL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	10	-	ns
Retransmit Cycle Time	t_{RTLWL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 25 40	 - -	ns
Retransmit Pulse Width	t_{RTLRTH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Retransmit Recovery Time	t_{RTHWL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	10	-	ns
Reset to Half-full Flag High	t_{RSLHFH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 25 30	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Reset to Full Flag High	t_{RSLFFH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 25 30	ns
Read Pulse Width After Empty Flag High	t_{EFHRH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Read High to Half-full Flag High	t_{RHHFH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	-	30	ns
Write Pulse Width after Full Flag High	t_{FFHWH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Read/Write Low to Expansion Out Low	t_{WLXOL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 15 30	ns
Expansion In Pulse Width	t_{XILXIH}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 15 30	 - -	ns
Expansion In Recovery Time	t_{XIHXIL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	10	-	ns
Expansion In Set-up Time	t_{XILRL}	3003	V_{DD} = 4.5V & 5.5V V_{SS} = 0V Note 6	10	-	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional go-no-go test with the following test sequences:

FUNCTIONAL TEST 1

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (b)
WRT-RD000	175	4.5 & 5.5	0	0	3	8	-2	1.5
WRT-RD1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-000	175	4.5 & 5.5	0	0	3	8	-2	1.5

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (b)
MARCH-155	175	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-000	175	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-155	175	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
ADDRESS	175	4.5 & 5.5	0	0	3	8	-2	1.5
CKBD-000	175	4.5 & 5.5	0	0	3	8	-2	1.5
CKBD-1FF	175	4.5 & 5.5	0	0	3	8	-2	1.5
FLAGS	175	4.5 & 5.5	0	0	3	8	-2	1.5
Xi	175	4.5 & 5.5	0	0	3	8	-2	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns) Note (a)	V_{DD} (V)	V_{SS} (V)	V_{IL} (mV)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (b)
WRITE/READ000	175	4.5	0	800	4.5	8	-2	1.5
WRITE/READ000	175	5.5	0	0	2.2	8	-2	1.5
FLAGS	175	4.5	0	800	4.5	8	-2	1.5
FLAGS	175	5.5	0	0	2.2	8	-2	1.5
Xi	175	4.5	0	800	4.5	8	-2	1.5
Xi	175	5.5	0	0	2.2	8	-2	1.5

FUNCTIONAL TEST 3

Pattern	Timing (ns) Note (a)		V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{out\ comp}$ (V) Note (b)
	Variants 01, 02	Variants 03, 04							
MARCH-000	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-155	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
MARCH-1FF	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-000	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-155	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FIFO-1FF	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
FLAGS	25	40	4.5 & 5.5	0	0	3	8	-2	1.5
Xi	25	40	4.5 & 5.5	0	0	3	8	-2	1.5

(a) $t_r = t_f \leq 5$ns.
(b) Output Load = 1 TTL gate equivalent + $C_L < 100$pF.

3. Measurement shall be performed using MARCH-000 and MARCH-1FF test patterns.
4. Guaranteed but not tested. Characterised at initial design and after major process changes.
5. Measurements shall be performed during Functional Test 3 using the following test patterns:

For t_{RLRL} and t_{RLQV}	MARCH-000
For t_{DVWH} and t_{WHDX}	FIFO-1FF
For t_{RLEFL}, t_{WHEFH}, t_{RHFFH}, t_{WLFFL} and t_{WLHFL}	FLAGS

6. Measurements shall be performed, on a go-no-go basis, during Functional Test 3.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics (Note 1)	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	±0.1	-	-1	µA
High Level Input Current	I_{IH}	±0.1	-	1	µA
Output Leakage Current, Third State, Low Level Applied	I_{OZL}	±0.1	-	-1	µA
Output Leakage Current, Third State, High Level Applied	I_{OZH}	±0.1	-	1	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V
Stand-by Supply Current	I_{DDSB}	±0.5	-	5	mA
Power Down Supply Current	I_{DDPD}	±40	-	400	µA

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

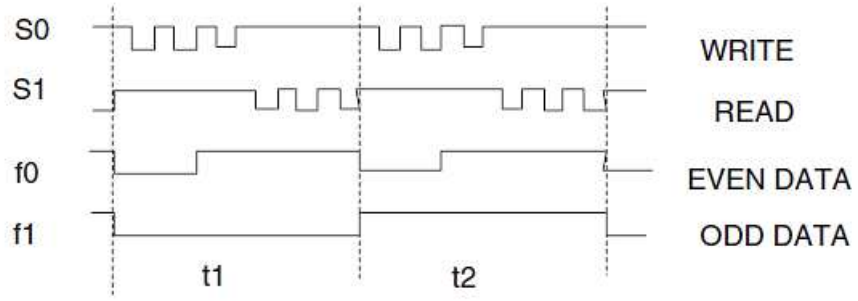
Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.The test methods, test conditions and limits shall be as specified for Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs $\overline{FF}$, Qn, $\overline{XO}/\overline{HF}$, $\overline{EF}$	V_{OUT}	V_{SS}	V
Inputs $\overline{RS}$, $\overline{FL}/\overline{RT}$	V_{IN}	V_{DD}	V
Input $\overline{XI}$	V_{IN}	V_{SS}	V
Input $\overline{W}$	V_{IN}	S0 (Note 1)	V
Input $\overline{R}$	V_{IN}	S1 (Note 1)	V
Inputs D0, D2, D4, D6, D8	V_{IN}	V_{GEN0} (Note 1)	V
Inputs D1, D3, D5, D7	V_{IN}	V_{GEN1} (Note 1)	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN0} f_{GEN1}	275k ±20% 137.5k ±20% 50 ±15% Duty Cycle Note 1	Hz
Positive Supply Voltage	V_{DD}	5 (+0.5 -0)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input waveforms to indicate required timing and phase relationships:



t1 = t2 = 3.6µs

2. Input Protection Resistor = Output Load = 1kΩ.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during radiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22 ±3	°C
Outputs $\overline{FF}$, Qn, $\overline{XO}/\overline{HF}$, $\overline{EF}$	V_{OUT}	Open	V
Inputs Dn, $\overline{W}$, $\overline{XI}$, $\overline{FL}/\overline{RT}$, $\overline{R}$	V_{IN}	V_{DD}	V
Input $\overline{RS}$	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	5 ±0.1	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input Protection Resistor = 1kΩ.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of radiation testing the devices shall successfully meet Room Temperature Electrical Measurements specified herein.

Unless otherwise specified the measurements shall be performed at T_{amb} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified for Room Temperature Electrical Measurements.