TRANSISTORS, POWER, MOSFET, N-CHANNEL, RAD-HARD

BASED ON TYPE STRH40N6

ESCC Detail Specification No. 5205/024

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION
941	Specification upissued to incorporate changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000
(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520502401F

- Detail Specification Reference: 5205024
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: F (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	STRH40N6	SMD.5	Q14	2	F [50kRAD(Si)]

The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Drain-Source Voltage	V_{DS}	60	V	Over T_{op}, V_{GS}=0V Note 2
Gate-Source Voltage	V_{GS}	±20	V	Over T_{op}
Drain Current	I_{DS}	30	A	Continuous At T_{case} ≤ +25 °C Note 1
		19	A	Continuous At T_{case} > +100 °C Note 1
Drain Current (Pulsed)	I_{DM}	120	A	Note 2
Power Dissipation	P_{tot}	66	W	At T_{case} ≤ +25 °C Note 1
Avalanche Energy (Single Pulse)	E_{AS}	 354 105	mJ	V_{DS}=40V, I_A=20A T_j = +25 ±3 °C T_j = +110 (+0 -5) °C
Avalanche Energy (Repetitive Pulse)	E_{AR}	 5.8 1.9	mJ	V_{DS}=40V, I_A=15A f=100kHz, Duty Cycle = 10% T_j = +25 ±3 °C T_j = +110 (+0 -5) °C
Operating Temperature Range	T_{op}	-55 to +150	°C	Note 3
Junction Temperature	T_j	+150	°C	
Storage Temperature Range	T_{stg}	-55 to +150	°C	Note 3
Soldering Temperature	T_{sol}	+260	°C	Note 4
Thermal Resistance, Junction-to-Heat Sink	$R_{th(j-s)}$	1.88	°C/W	Note 5
Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$	50	°C/W	Note 2

NOTES:

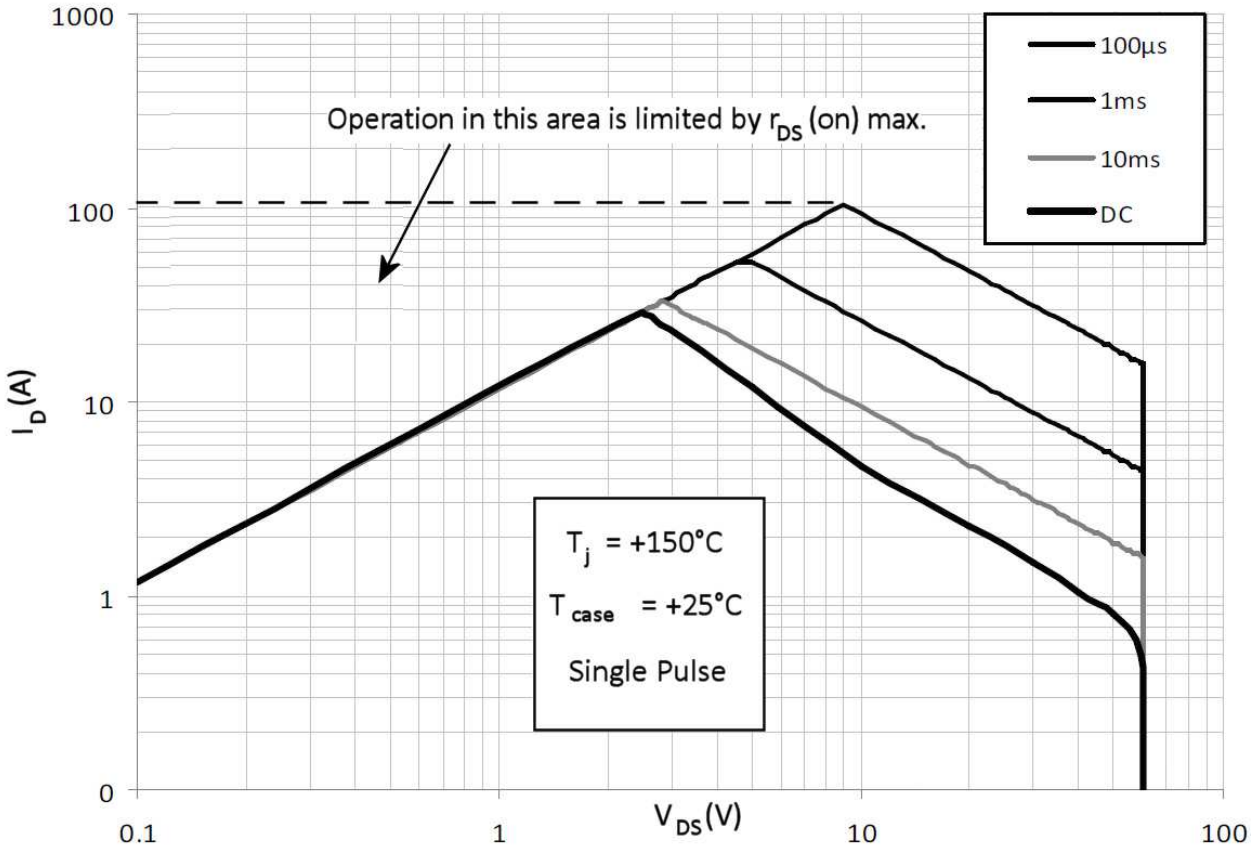
1. I_{DS} and P_{tot} ratings are in accordance with $R_{th(j-s)}$. The maximum theoretical I_D limit at T_{case} > +25°C can be obtained by using the following formula (I_D is limited by the package and device construction):

$$I_D = \sqrt{\frac{T_j(max) - T_{case}}{(R_{th(j-s)}) \times \left(r_{DS(on)} \text{ at } T_j(max)\right)}}$$

where ($r_{DS(on)}$ at T_j(max)) = 94.5mΩ.
For T_{case} > +25°C, the power dissipation derates linearly to 0W at T_{case} = +150°C.

2. Safe Operating Area applies as follows:

Maximum Safe Operating Area



3. For Variants with hot solder dip lead finish all testing and any handling performed at T_{amb} > +125°C shall be carried out in a 100% inert atmosphere.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
5. Package is mounted on an infinite heatsink.

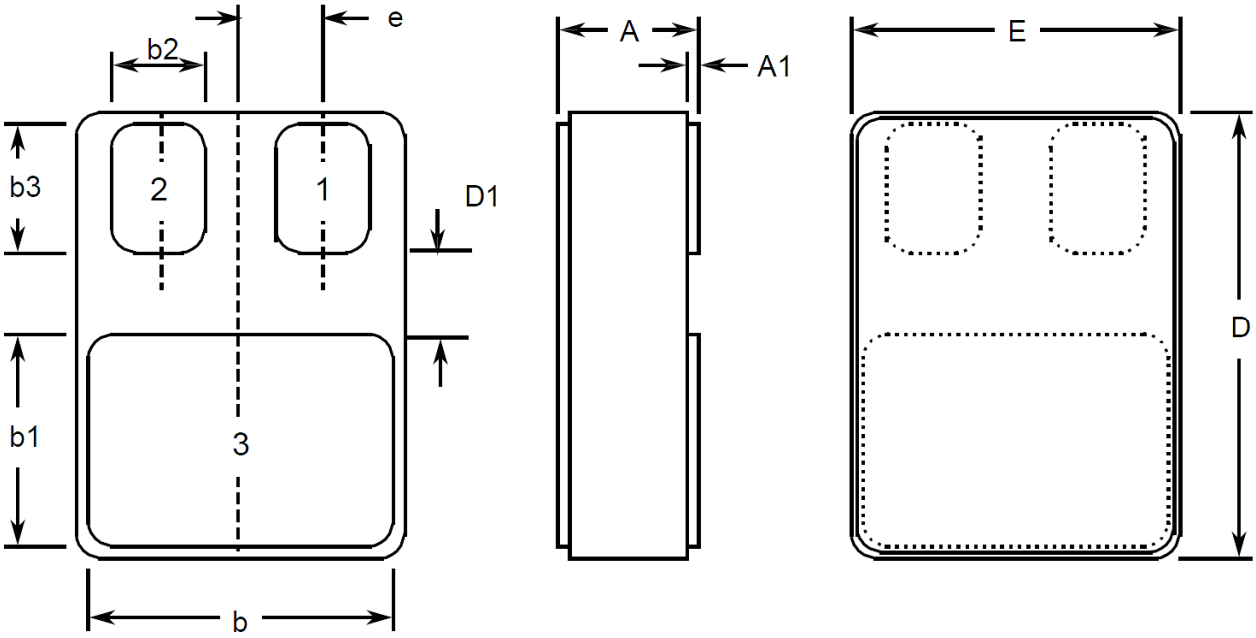
1.6 HANDLING PRECAUTIONS

These components are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 1700 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Surface Mount Package (SMD.5) – 3 terminal



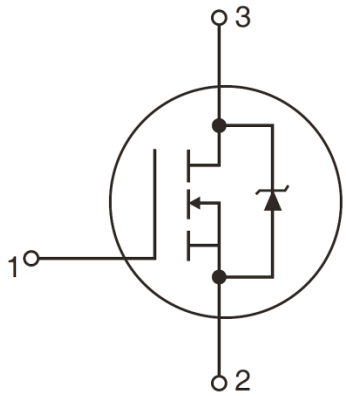
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.84	3.15	
A1	0.25	0.51	
b	7.13	7.39	
b1	5.58	5.84	
b2	2.28	2.54	2
b3	2.92	3.18	2
D	10.03	10.28	
D1	0.76	-	2
E	7.39	7.64	
e	1.91 BSC		2

NOTES:

1. The terminal identification is specified by the component's geometry. See Functional Diagram for the terminal connections.
2. 2 places.

1.8 FUNCTIONAL DIAGRAM

Terminal 1: Gate
Terminal 2: Source
Terminal 3: Drain



NOTES:
1. The lid is not connected to any terminal.

1.9 MATERIALS AND FINISHES
Materials and finishes shall be as follows:

(a) Case
The case shall be hermetically sealed and have a ceramic body with a kovar lid.
(b) Terminals
As specified in Component Type Variants.

2 REQUIREMENTS

2.1 GENERAL
The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

- Verification of Safe Operating Area
  The Safe Operating Area shall be verified by performing the ΔV_{SD} test specified in Room Temperature Electrical Measurements (Thermal Resistance, Junction-to-Case).
- A High Temperature Forward Bias test shall be performed instead of Power Burn-in.

2.1.1.2 Deviations from Qualification and Periodic Tests - Chart F4
Terminal Strength is not applicable.

2.2 WAFER LOT ACCEPTANCE
A SEM inspection shall be performed as specified in the ESCC Generic Specification.

2.3 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) The ESCC Qualified Component symbol (for ESCC qualified components only).
(b) The ESCC Component Number.
(c) Traceability information.

2.4 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables.

2.4.1 Room Temperature Electrical Measurements

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 °C.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	3407	V_{GS} = 0V, I_D = 1mA Bias condition C	60	-	V
Gate-to-Source Leakage Current 1	I_{GSS1}	3411	V_{GS} = 20V, V_{DS} = 0V Bias condition C	-	100	nA
Gate-to-Source Leakage Current 2	I_{GSS2}	3411	V_{GS} = -20V, V_{DS} = 0V Bias condition C	-100	-	nA
Drain Current	I_{DSS}	3413	V_{DS} = 48V, V_{GS} = 0V Bias condition C	-	10	µA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ I_D = 1mA	2	4.5	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	3421	V_{GS} = 12V, I_D = 15A Note 1	-	45	mΩ
Source-to-Drain Diode Forward Voltage	V_{SD}	4011	V_{GS} = 0V, I_{SD} = 30A Note 1	-	1.5	V
Thermal Resistance, Junction-to-Heat Sink	$R_{th(j-s)}$	3161	Note 2	-	1.88	°C/W
Input Capacitance	C_{iss}	3431	V_{GS} = 0V, V_{DS} = 25V f = 1MHz	1312	1968	pF
Output Capacitance	C_{oss}	3453		281	421	pF
Reverse Transfer Capacitance	C_{rss}	3433		111	167	pF
Total Gate Charge	Q_g	3471	V_{GS} = 12V, V_{DS} = 30V I_D = 40A	35	52	nC
Gate-to-Source Charge	Q_{gs}			9	13	nC
Gate-to-Drain Charge	Q_{gd}			12	18	nC

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Turn-on Delay Time	$t_{d(on)}$	3472	V_{GS} = 12V, V_{DS} = 30V I_D = 20A R_G = 4.7Ω	13	21	ns
Rise Time	t_r			26	92	ns
Turn-off Delay Time	$t_{d(off)}$			18	48	ns
Fall Time	t_f			7	16	ns
Reverse Recovery Time	t_{rr}	3473	V_{DS} = 48V, I_{SD} = 40A di/dt = 100A/µs T_j = +25 ±3 °C	288	432	ns

2.4.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 3	Limits		Units
				Min	Max	
Gate-to-Source Leakage Current 1	I_{GSS1}	3411	V_{GS} = 20V, V_{DS} = 0V Bias condition C T_{case} = +125 (+0 -5) °C	-	200	nA
Gate-to-Source Leakage Current 2	I_{GSS2}	3411	V_{GS} = -20V, V_{DS} = 0V Bias condition C T_{case} = +125 (+0 -5) °C	-200	-	nA
Drain Current	I_{DSS}	3413	V_{DS} = 48V, V_{GS} = 0V Bias condition C T_{case} = +125 (+0 -5) °C	-	100	µA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$, I_D = 1mA T_{case} = +125 (+0 -5) °C	1.5	3.7	V
			$V_{DS} \geq V_{GS}$, I_D = 1mA T_{case} = -55 (+5 -0) °C	2.1	5.5	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	3421	V_{GS} = 12V, I_D = 15A T_{case} = +125 (+0 -5) °C Note 1	-	76	mΩ
Source-to-Drain Diode Forward Voltage	V_{SD}	4011	V_{GS} = 0V, I_{SD} = 30A T_{case} = +125 (+0 -5) °C Note 1	-	1.275	V

2.4.3 Notes to Room, High and Low Electrical Measurements

1. Pulsed measurement: Pulse Width ≤ 680µs, Duty Cycle ≤ 2%.
2. The $R_{th(j-s)}$ limit is guaranteed by performing a ΔV_{SD} (go-no-go) test. The following test conditions and limits shall apply:
   - V_{DS} = 3V
   - I_D = 18.33A
   - I_{cal} = 10mA
   - t_{pulse} = 20ms
   - t_{cal} = 50µs
   - V_{SD} = 100mV minimum, 190mV maximum
3. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 °C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Gate-to-Source Leakage Current 1	I_{GSS1}	±50 or (1) ±100%	-	100	nA
Gate-to-Source Leakage Current 2	I_{GSS2}	±50 or (1) ±100%	-100	-	nA
Drain Current	I_{DSS}	±4 or (1) ±100%	-	10	µA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	±5%	2	4.5	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	±10%	-	45	mΩ

NOTES:

1. Whichever is the greater referred to the initial value.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3 °C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Drain Current	I_{DSS}	-	10	µA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	2	4.5	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	-	45	mΩ

2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

HTRB Burn-in shall be performed in accordance with MIL-STD-750, Test Method 1042, Test Condition A with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	48	V
Gate-to-Source Voltage	V_{GS}	0	V
Duration	t	240 minimum	Hours

2.8 HIGH TEMPERATURE FORWARD BIAS BURN-IN CONDITIONS

HTFB Burn-in shall be performed in accordance with MIL-STD-750, Test Method 1042, Test Condition B with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	0	V
Gate-to-Source Voltage	V_{GS}	16	V
Duration	t	48 minimum	Hours

2.9 OPERATING LIFE CONDITIONS

Operating Life shall consist of High Temperature Reverse Bias in accordance with MIL-STD-750, Test Method 1042, Test Condition A, followed by High Temperature Forward Bias in accordance with MIL-STD-750, Test Method 1042, Test Condition B. The test conditions are as follows:

High Temperature Reverse Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	48	V
Gate-to-Source Voltage	V_{GS}	0	V
Duration	t	1000 minimum	Hours

High Temperature Forward Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Drain-to-Source Voltage	V_{DS}	0	V
Gate-to-Source Voltage	V_{GS}	16	V
Duration	t	1000 minimum	Hours

2.10 TOTAL DOSE RADIATION TESTING

All lots shall be irradiated in accordance with ESCC Basic Specification No. 22900, standard dose rate (window 1: 3.6kRAD to 36kRAD per hour).

2.10.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

The following bias condition (worst-case) shall be used for Total Dose Radiation Testing at T_{amb} = 22 ±3 °C:

With V_{GS} bias = +15V and V_{DS} = 0V during irradiation.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

2.10.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ±3 °C.

Unless otherwise specified the test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during irradiation testing, on completion of irradiation testing, after 24 hours anneal at Room Temperature and after 168 hours anneal at +100 ±3 °C are shown below.

Characteristics	Symbols	Limits			Units
		Drift Values (Δ)	Absolute		
			Min	Max	
Drain-to-Source Voltage Note 1	V_{DSS}	-20% Note 2	N/A		V
Gate-to-Source Leakage Current 1	I_{GSS1}	+1.5	-	100	nA
Gate-to-Source Leakage Current 2	I_{GSS2}	-1.5	-100	-	nA
Drain Current	I_{DSS}	+20	-	10	µA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	-60% / +20%	2	4.5	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	±10%	-	45	mΩ
Source-to-Drain Diode Forward Voltage	V_{SD}	±5%	-	1.5	V
Total Gate Charge	Q_g	-5% / +50%	35	52	nC
Gate-to-Source Charge	Q_{gs}	±35%	9	13	nC
Gate-to-Drain Charge	Q_{gd}	-5% / +110%	12	18	nC

NOTES:

1. Drain-to-Source Voltage measurements shall be made in accordance with MIL-STD-750, Test Method 3405, with V_{GS} = 0V and I_D = 1mA.
2. Referred to an initial Drain-to-Source Voltage measurement made prior to the commencement of Total Dose Radiation Testing.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Room Temperature Electrical Measurements	The AC characteristics C_{iss}, C_{oss}, C_{rss}, Q_g, Q_{gs}, Q_{gd}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f and t_{rr} may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot in accordance with STMicroelectronics procedure 8212069, which includes AC (C_{iss}, C_{oss}, C_{rss}, Q_g, Q_{gs}, Q_{gd}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f and t_{rr}) characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Electrical Measurements for Total Dose Radiation Testing	The AC characteristics Q_g, Q_{gs} and Q_{gd} need not be measured because they are guaranteed by the results obtained by STMicroelectronics during the evaluation phase which proved these characteristics are directly correlated to the $V_{GS(th)}$ shift.
Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.

ADDITIONAL DATA - STMICROELECTRONICS (F)

N.B: Heavy ions characterisation has been carried out on STRH100N6 devices. The STRH40N6 is based on the same technology and the same epitaxy. The results obtained on the STRH100N6 are considered transposable to the STRH40N6.

(a) Derating for Space Application
These components are susceptible to Single Event Gate Rupture if operated in a space environment unless the following derating is applied. The derating for space applications was originally obtained on STRH100N6 devices under the following test conditions. The testing was performed in a vacuum at UCL (Louvain-la-Neuve, Belgium):

Ion used = Kr

LET = 32 (MeV / (mg/cm^2))

Energy = 768 MeV

Range = 94µm

$V_{DS} \leq 60V$ when $V_{GS} = 0V$,

$V_{DS} \leq 48V$ when $V_{GS} = -2V$,

$V_{DS} \leq 15V$ when $V_{GS} = -15V$.

Single Event Effect Safe Operating Area for STRH100N6