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INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS FIFO REGISTER WITH 3-STATE OUTPUTS

BASED ON TYPE 40105B

ESCC Detail Specification No. 9306/033

Issue 3	September 2009

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DCR No.	CHANGE DESCRIPTION
255, 447, 485	Specification up issued to incorporate editorial and technical changes per DCRs.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 930603301

- Detail Specification Reference: 9306033
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g
01	40105B	FP	G2	0.7
02	40105B	FP	G4	0.7
07	40105B	CCP	2	0.6
08	40105B	DIP	G2	2.2
09	40105B	DIP	G4	2.2
10	40105B	SO	G2	0.7
11	40105B	SO	G4	0.7

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 18	V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD} +0.5	V	Note 1 Power on
Input Current	I_{IN}	±10	mA	-
Device Power Dissipation (Continuous)	P_D	200	mW	-
Power Dissipation per Output	P_{DSO}	100	mW	-
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	-
Soldering Temperature For FP, DIP and SO For CCP	T_{sol}	 +265 +245	°C	 Note 2 Note 3

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 15V$.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

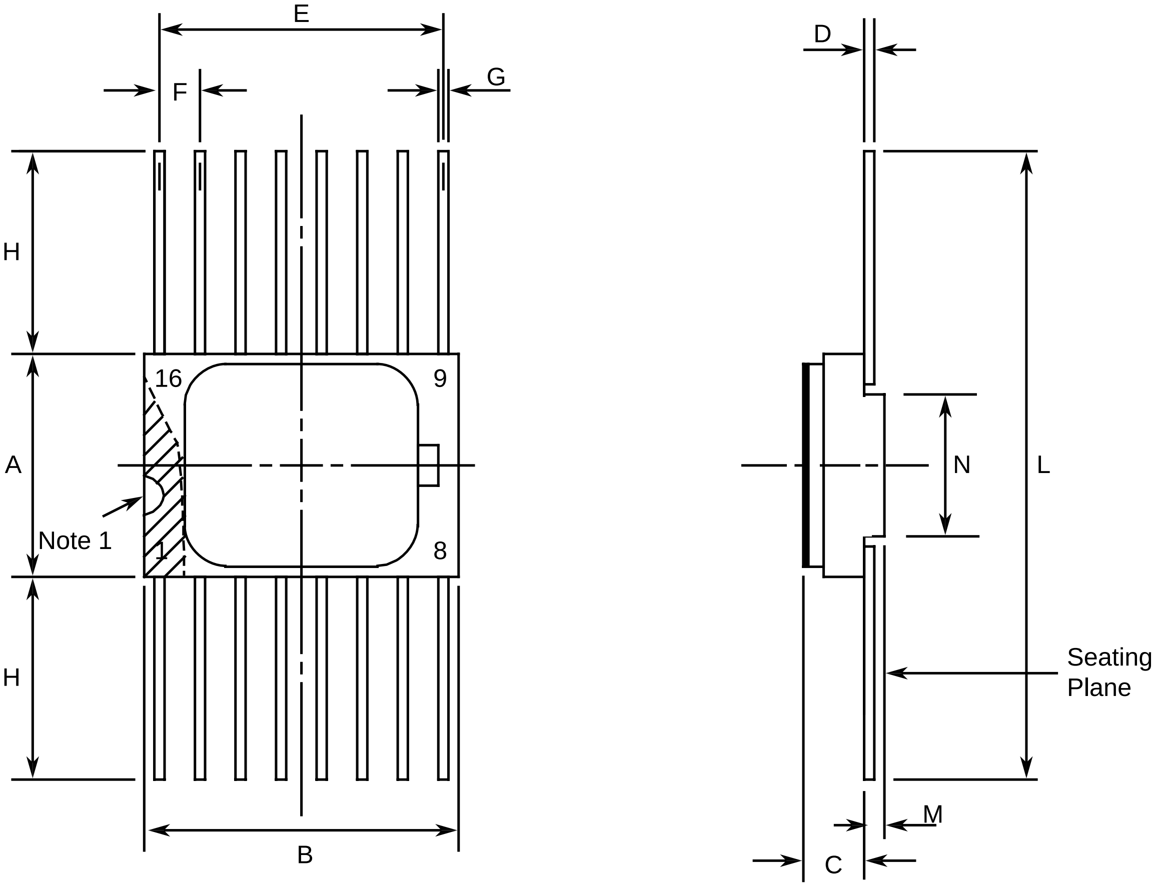
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

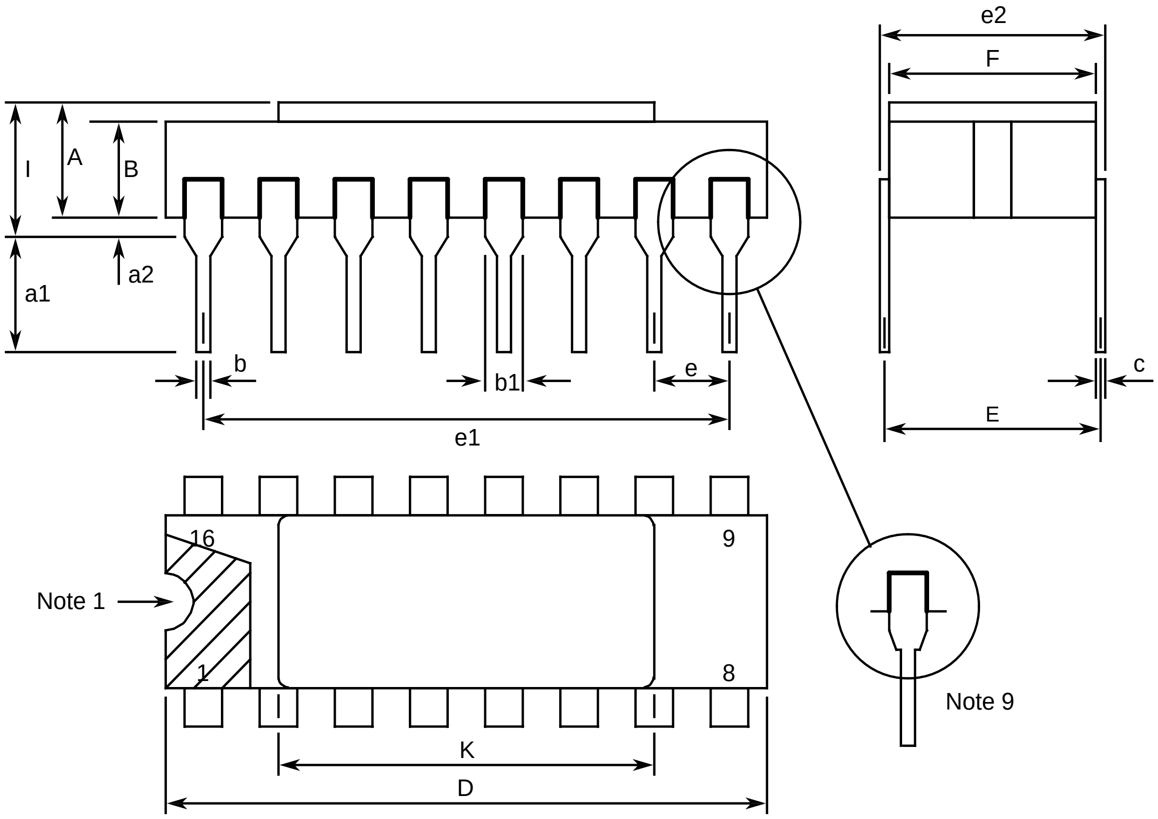
Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	6	-	5
L	18.75	22	
M	0.33	0.43	
N	4.32 TYPICAL		

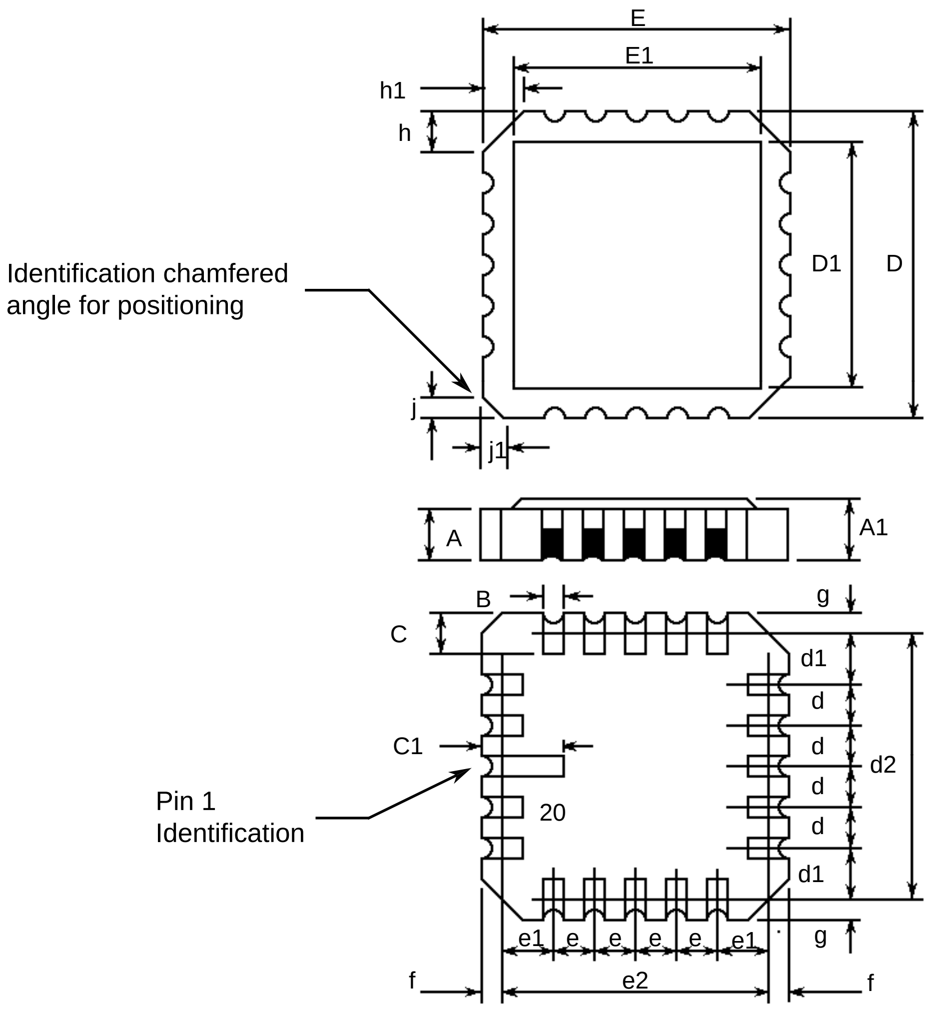
1.7.2 Dual-in-line Package (DIP) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	2.1	2.71	
a1	3	3.7	
a2	0.63	1.14	2
B	1.82	2.39	
b	0.4	0.5	5
b1	1.14	1.5	5
c	0.2	0.3	5
D	20.06	20.58	
E	7.36	7.87	
e	2.54 BSC		4, 6
e1	17.65	17.9	
e2	7.62	8.12	
F	7.29	7.7	
I	-	3.83	

Symbols	Dimensions mm		Notes
	Min	Max	
K	10.9	12.1	

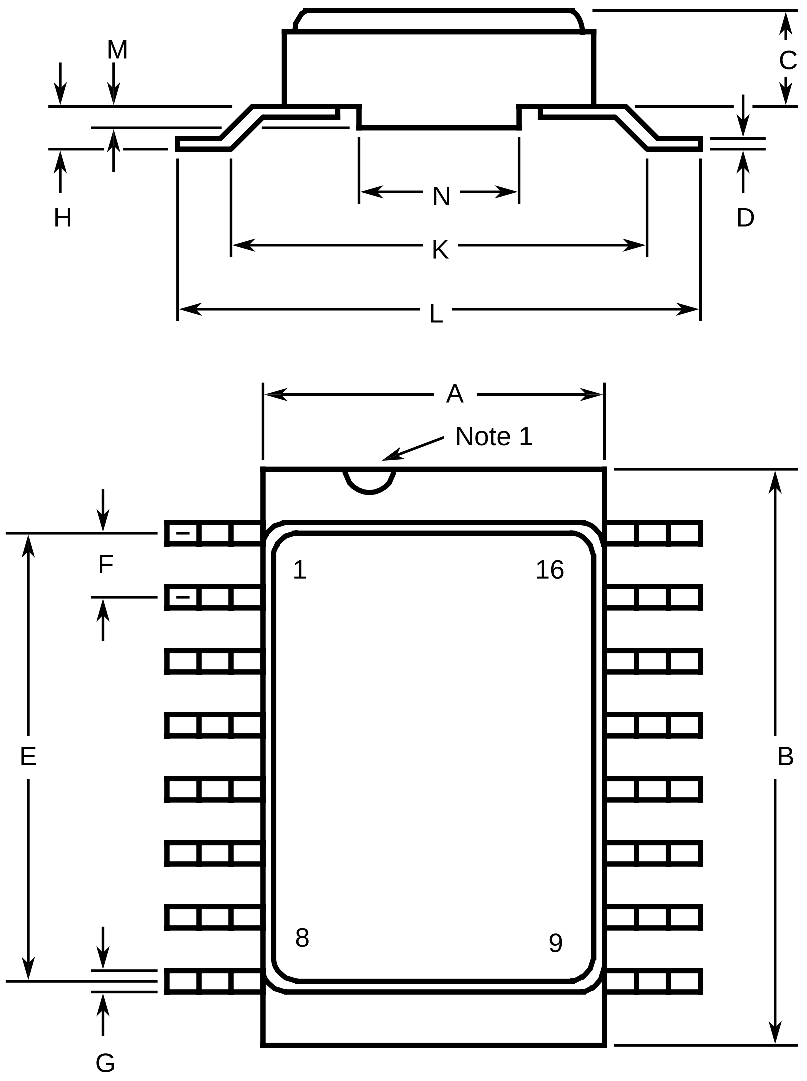
1.7.3 Chip Carrier Package (CCP) - 20 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5
C	1.06	1.47	5
C1	1.91	2.41	

Symbols	Dimensions mm		Notes
	Min	Max	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27 BSC		3
d2	7.62 BSC		
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27 BSC		3
e2	7.62 BSC		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	0.6	0.9	5

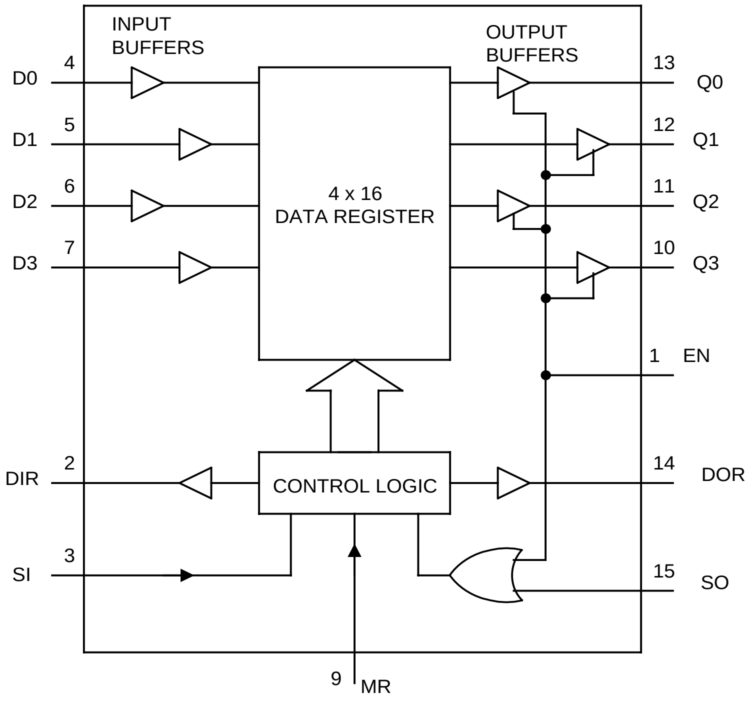
Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Notes to Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only



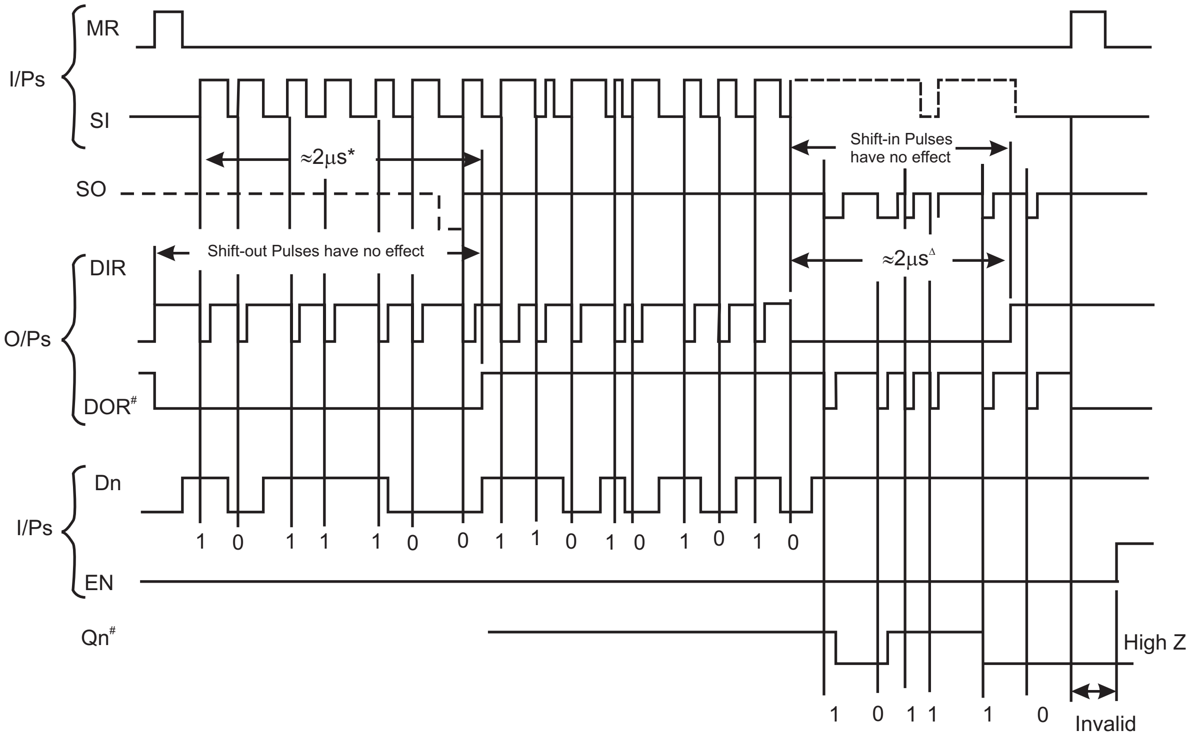
1.9 PIN ASSIGNMENT

Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	EN Input (3-State Enable)	EN Input (3-State Enable)	11	Q2 Output	MR Input (Master Reset)
2	DIR Output (Data In Ready)	DIR Output (Data In Ready)	12	Q1 Output	Q3 Output
3	SI Input (Shift-In)	-	13	Q0 Output	-
4	D0 Input	SI Input (Shift-In)	14	DOR Output (Data Out Ready)	Q2 Output
5	D1 Input	D0 Input	15	SO Input (Shift-Out)	Q1 Output
6	D2 Input	D1 Input	16	V_{DD}	Q0 Output
7	D3 Input	D2 Input	17	-	DOR Output (Data Out Ready)
8	V_{SS}	-	18	-	-
9	MR Input (Master Reset)	D3 Input	19	-	SO Input (Shift-Out)
10	Q3 Output	V_{SS}	20	-	V_{DD}

1.10 TRUTH TABLE AND TIMING CHART

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance.
2. ↑ = Transition, Low to High ; ↓ = Transition, High to Low.

INPUTS				OUTPUTS		FUNCTION
EN	MR	SI	SO	DIR	DOR	
-	-	-	-	H	L	FIFO is empty
-	-	-	-	H	X	FIFO contains space for data
-	-	-	-	X	H	FIFO contains data
-	-	-	-	L	H	FIFO is full
X	L	↑	X	H	X	Data loaded into FIFO
L	L	X	↓	X	H	Data unloaded from FIFO
X	H	L	X	H	L	Data in FIFO is invalid (No change)
H	X	X	X	X	X	Outputs Qn = Z



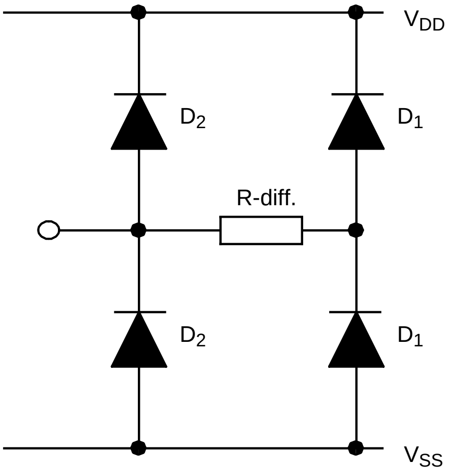
NOTES:

* Ripple time from position 1 to position 16 (V_{DD} = 5V).

Δ Ripple time from postion 16 to position 1 (V_{DD} = 5V).

Data Out Ready goes High in advance of the Data Outputs (Qn) by a maximum of 50ns at V_{DD} = 5V, 25ns at V_{DD} = 10V and 20ns at V_{DD} = 15V (C_L = 50pF and T_{amb} = +25^{o}C).

1.11 INPUT PROTECTION NETWORK



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{amb}=+22 \pm 3^oC$.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load $V_{IL}=0V, V_{IH}=3V$ $V_{DD}=3V, V_{SS}=0V$ Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load $V_{IL}=0V, V_{IH}=15V$ $V_{DD}=15V, V_{SS}=0V$ Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Quiescent Current	I_{DD}	3005	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 3	-	1	µA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test)=0V V_{DD}=15V,V_{SS}=0V	-	-50	nA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=15V V_{DD}=15V,V_{SS}=0V	-	50	nA
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL}=0V, V_{IH}=15V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	3007	V_{IL}=1.5V, V_{IH}=3.5V, I_{OL}=0A V_{DD}=5V, V_{SS}=0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	V_{OL3}	3007	V_{IL}=4V, V_{IH}=11V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	1.5	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL}=0V, V_{IH}=15V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	3006	V_{IL}=1.5V, V_{IH}=3.5V, I_{OH}=0A V_{DD}=5V, V_{SS}=0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	V_{OH3}	3006	V_{IL}=4V, V_{IH}=11V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	13.5	-	V
Low Level Output Current 1	I_{OL1}	-	V_{IL}=0V, V_{IH}=5V, V_{OL}=0.4V V_{DD}=5V, V_{SS}=0V Note 4	510	-	µA
Low Level Output Current 2	I_{OL2}	-	V_{IL}=0V, V_{IH}=15V, V_{OL}=1.5V V_{DD}=15V, V_{SS}=0V Note 4	3.4	-	mA
High Level Output Current 1	I_{OH1}	-	V_{IL}=0V, V_{IH}=5V, V_{OH}=4.6V V_{DD}=5V, V_{SS}=0V Note 4	-510	-	µA
High Level Output Current 2	I_{OH2}	-	V_{IL}=0V, V_{IH}=15V, V_{OH}=13.5V V_{DD}=15V, V_{SS}=0V Note 4	-3.4	-	mA
Output Leakage Current Third State Low Level Applied	I_{OZL}	3020	V_{IL}= 0V V_{IH}=15V V_{OL}=0V V_{DD}=15V, V_{SS}=0V	-	-400	nA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Leakage Current Third State High Level Applied	I_{OZH}	3021	V_{IL}= 0V V_{IH}=15V V_{OH}=15V V_{DD}=15V, V_{SS}=0V	-	400	nA
Threshold Voltage N-Channel	V_{THN}	-	MR Input at Ground All Other Inputs: V_{IN}=5V V_{DD}=5V, I_{SS}=-10µA	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	-	MR Input at Ground All Other Inputs: V_{IN}=-5V V_{SS}=-5V, I_{DD}=10µA	0.7	3	V
Input Clamp Voltage 1, to V_{SS}	V_{IC1}	-	I_{IN} (Under Test)= -100µA V_{DD}=Open, V_{SS}=0V All Other Pins Open	-	-2	V
Input Clamp Voltage 2, to V_{DD}	V_{IC2}	-	V_{IN} (Under Test)=6V R=30kΩ, V_{SS}=Open All Other Pins Open Note 5	3	-	V
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test)=0V V_{DD}= V_{SS}=0V f = 100 kHz to 1 MHz Note 6	-	7.5	pF
Propagation Delay High to Low 1, SO to DOR	t_{PHL1}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	320	ns
Propagation Delay High to Low 2, SI to DIR	t_{PHL2}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	270	ns
Output Enable Time High Impedance to Low Output, EN to Q0	t_{PZL}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	200	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Output Disable Time Low Output to High Impedance, EN to Q0	t_{PLZ}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	200	ns
Output Enable Time High Impedance to High Output, EN to Q0	t_{PZH}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	280	ns
Output Disable Time High Output to High Impedance, EN to Q0	t_{PHZ}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	280	ns
Transition Time Low to High, DIR, DOR	t_{TLH}	3004	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	150	ns
Transition Time High to Low, DIR, DOR	t_{THL}	3004	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Note 7	-	150	ns
Maximum Shift-In or Shift-Out rate, SI, SO	f_S	-	V_{IN}(Under Test)=Pulse Generator V_{IN} (Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=5V, V_{DD}=5V, V_{SS}=0V Notes 8, 9	1.5	-	MHz

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5) ^oC and T_{amb}=- 55(+5-0)^oC.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL}=0V,V_{IH}=3V V_{DD}=3V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL}=0V,V_{IH}=15V V_{DD}=15V,V_{SS}=0V Note 3 T_{amb}=+125^{o}C T_{amb}=- 55^{o}C	 - -	 30 1	µA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test)=0V V_{DD}=15V,V_{SS}=0V T_{amb}=+125^{o}C T_{amb}=- 55^{o}C	 - -	 -100 -50	nA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=15V V_{DD}=15V,V_{SS}=0V T_{amb}=+125^{o}C T_{amb}=- 55^{o}C	 - -	 100 50	nA
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL}=0V, V_{IH}=15V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	3007	V_{IL}=1.5V, V_{IH}=3.5V, I_{OL}=0A V_{DD}=5V, V_{SS}=0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	V_{OL3}	3007	V_{IL}=4V, V_{IH}=11V, I_{OL}=0A V_{DD}=15V, V_{SS}=0V	-	1.5	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL}=0V, V_{IH}=15V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	3006	V_{IL}=1.5V, V_{IH}=3.5V, I_{OH}=0A V_{DD}=5V, V_{SS}=0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	V_{OH3}	3006	V_{IL}=4V, V_{IH}=11V, I_{OH}=0A V_{DD}=15V, V_{SS}=0V	13.5	-	V

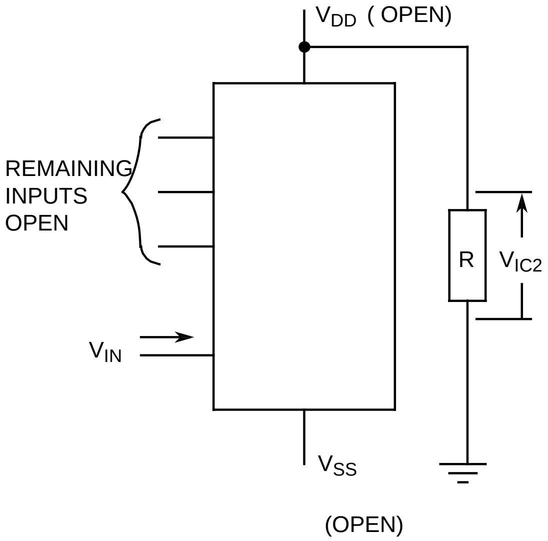
Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Current 1	I_{OL1}	-	V_{IL}=0V, V_{IH}=5V, V_{OL}=0.4V V_{DD}=5V, V_{SS}=0V Note 4			µA
			T_{amb}=+125^oC	360	-	
			T_{amb}=- 55^oC	640	-	
Low Level Output Current 2	I_{OL2}	-	V_{IL}=0V, V_{IH}=15V, V_{OL}=1.5V V_{DD}=15V, V_{SS}=0V Note 4			mA
			T_{amb}=+125^oC	2.4	-	
			T_{amb}=- 55^oC	4.2	-	
High Level Output Current 1	I_{OH1}	-	V_{IL}=0V, V_{IH}=5V, V_{OH}=4.6V V_{DD}=5V, V_{SS}=0V Note 4			µA
			T_{amb}=+125^oC	-360	-	
			T_{amb}=- 55^oC	-640	-	
High Level Output Current 2	I_{OH2}	-	V_{IL}=0V, V_{IH}=15V, V_{OH}=13.5V V_{DD}=15V, V_{SS}=0V Note 4			mA
			T_{amb}=+125^oC	-2.4	-	
			T_{amb}=- 55^oC	-4.2	-	
Output Leakage Current Third State Low Level Applied	I_{OZL}	3020	V_{IL}= 0V V_{IH}=15V V_{OL}=0V V_{DD}=15V, V_{SS}=0V			µA
			T_{amb}=+125^oC	-	-12	
			T_{amb}=- 55^oC	-	-0.4	
Output Leakage Current Third State High Level Applied	I_{OZH}	3021	V_{IL}= 0V V_{IH}=15V V_{OH}=15V V_{DD}=15V, V_{SS}=0V			µA
			T_{amb}=+125^oC	-	12	
			T_{amb}=- 55^oC	-	0.4	
Threshold Voltage N-Channel	V_{THN}	-	MR Input at Ground All Other Inputs: V_{IN}=5V V_{DD}=5V, I_{SS}=-10µA			V
			T_{amb}=+125^oC	-0.3	-3.5	
			T_{amb}=- 55^oC	-0.7	-3.5	
Threshold Voltage P-Channel	V_{THP}	-	MR Input at Ground All Other Inputs: V_{IN}=-5V V_{SS}=-5V, I_{DD}=10µA			V
			T_{amb}=+125^oC	0.3	3.5	
			T_{amb}=- 55^oC	0.7	3.5	

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be $V_{IN} = V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with $V_{OH} \geq V_{DD}$ -0.5V, $V_{OL} \leq$ 0.5V. The maximum time to output comparator strobe = 300µs.
3. Quiescent Current shall be tested using the following input conditions where 1 = V_{IH} and 0 = V_{IL}:

I_{DD} Test	Input Pattern No.	Input Conditions							
		EN	SI	SO	MR	D0	D1	D2	D3
(a)	1	0	1	0	1	1	1	1	1
(b)	2	0	1	0	0	1	1	1	1
(c)	3	1	0	1	1	0	0	0	0
(d)	4	0	1	1	0	0	0	0	0
SI = 16 pulses									
(e)	5	1	1	1	0	0	0	0	0

4. Interchange of forcing and measuring parameters is permitted.
5. Input Clamp Voltage 2 to V_{DD}, V_{IC2}, shall be tested on each input as follows:-

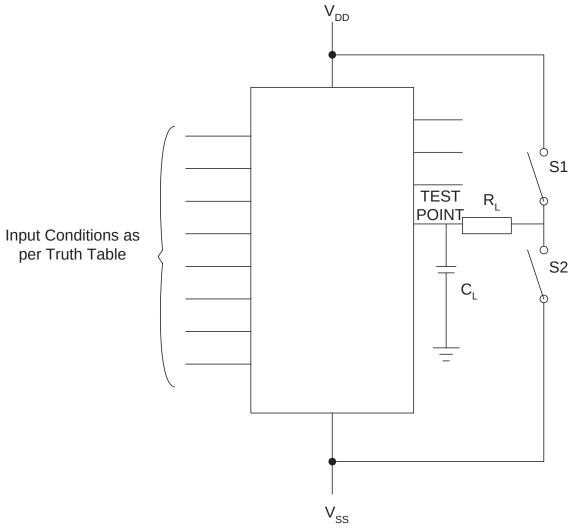


6. Guaranteed but not tested.
7. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.

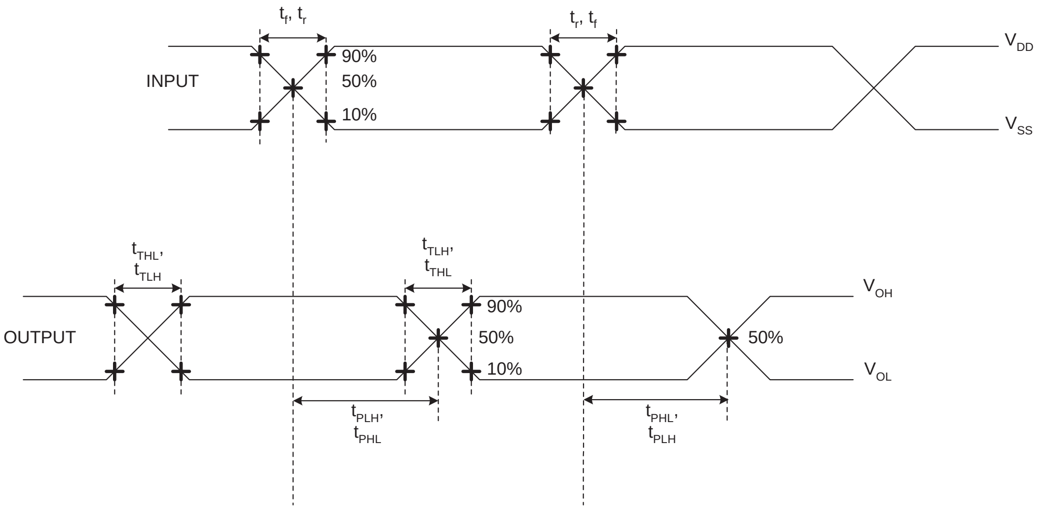
   The pulse generator shall have the following characteristics:

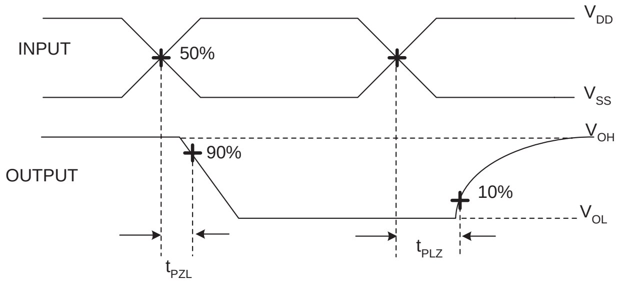
   V_{GEN} = 0 to V_{DD}; f_{GEN} = 500kHz; t_r and $t_f \leq$15 ns (10% to 90%); duty cycle = 50%; Z_{out} = 50Ω. Output load capacitance C_L = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture. Output load resistance R_L = 200kΩ ±5%.

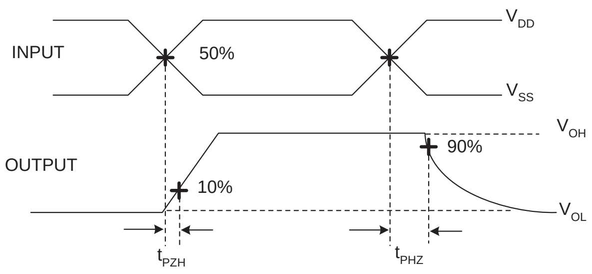
   Propagation delay and transition time shall be measured as follows:



Parameter	R_L	S1	S2
t_{PZH}	1kΩ	Open	Closed
t_{PZL}		Closed	Open
t_{PHZ}		Open	Closed
t_{PLZ}		Closed	Open
t_{PHL}, t_{PLH}, t_{THL}, t_{TLH}	200kΩ	Open	Closed







8. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.
9. A pulse, having the following conditions, shall be applied to the SI or SO input: V_P = 0V to V_{DD}. Maximum Shift-In or Shift-Out rate (f_S) is considered met if proper output state changes occur with the pulse repetition rate set to that given in the Limits column.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current	I_{DD}	±0.15	-	1	μA
Low Level Output Current 1	I_{OL1}	±15% (2)	510	-	μA
High Level Output Current 1	I_{OH1}	±15% (2)	-510	-	μA
Output Leakage Current Third State Low Level Applied	I_{OZL}	±60	-	-400	μA
Output Leakage Current Third State High Level Applied	I_{OZH}	±60	-	400	μA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:
1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Percentage of limit value if voltage is the measuring parameter.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb}=+22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Quiescent Current	I_{DD}	±0.15	-	1	µA
Low Level Input Current	I_{IL}	-	-	-50	nA
High Level Input Current	I_{IH}	-	-	50	nA
Low Level Output Voltage 1	V_{OL1}	-	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	-	-	500	mV
High Level Output Voltage 1	V_{OH1}	-	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	-	4.5	-	V
Low Level Output Current 1	I_{OL1}	±15% (3)	510	-	µA
Low Level Output Current 2	I_{OL2}	±15% (3)	3.4	-	mA
High Level Output Current 1	I_{OH1}	±15% (3)	-510	-	µA
High Level Output Current 2	I_{OH2}	±15% (3)	-3.4	-	mA
Output Leakage Current Third State Low Level Applied	I_{OZL}	±60	-	-400	nA
Output Leakage Current Third State High Level Applied	I_{OZH}	±60	-	400	nA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. Percentage of limit value if voltage is the measuring parameter.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs DIR, DOR, Qn	V_{OUT}	Open	V
Inputs MR, SO	V_{IN}	V_{SS}	V
Inputs EN, SI, Dn	V_{IN}	V_{DD}	V

Characteristics	Symbols	Test Conditions	Units
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs DIR, DOR, Qn	V_{OUT}	Open	V
Inputs MR, SO	V_{IN}	V_{DD}	V
Inputs EN, SI, Dn	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs DIR, DOR, Qn	V_{OUT}	$V_{DD}/2$	V
Inputs EN, MR	V_{IN}	V_{SS}	V
Inputs Dn	V_{IN}	V_{GEN1}	V
Inputs SI, SO	V_{IN}	V_{GEN2}	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	50k 25k 50% Duty Cycle	Hz
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Screening Tests - Chart F3	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255. Solderability is not applicable unless specifically stipulated in the Purchase Order.
Deviations from Qualification and Periodic Tests - Chart F4	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Deviations from High and Low Temperatures Electrical Measurements	High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.