# TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD

## ESCC Basic Specification No. 22900

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## DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

| DCR No. | CHANGE DESCRIPTION |
|---|---|
| 788, 935 | Specification upissued to incorporate changes per DCR.<br>Specification produced using MSWORD. Changes in presentation are possible. |

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## 1 SCOPE

This specification defines the basic requirements applicable to the steady-state irradiation testing of integrated circuits and discrete semiconductors suitable for space applications.

Two separate phases are distinguished in this Test Method to reflect different objectives. The requirements for the two phases are:

- Evaluation of the technology, especially oxide process variations and time dependent effects.
- Qualification and lot acceptance of high reliability devices.

This specification addresses two specific cases:

- The evaluation testing procedures and the qualification and lot acceptance testing procedures performed by a component manufacturer aiming at an ESCC qualification (Sections 5 and 6 respectively),
- The testing procedures for any other purpose, which are covered in Section 7.

Detailed requirements applicable to individual component types (e.g. test circuits, worst case for bias during irradiation) shall be specified in the applicable Component Detail Specification and the relevant Test Plan. The test shall be considered as destructive.

## 2 RELATED DOCUMENTS

### 2.1 APPLICABLE DOCUMENTS

The following ESCC specifications, at current issue, form part of and shall be read in conjunction with this specification.

- ESCC 21300 Terms, Definitions, Abbreviations, Symbols and Units
- ESCC 21500 Calibration System Requirements

Unless otherwise stated herein, references within the text of this specification to the Generic Specification or the Detail Specification shall mean the relevant ESCC Generic or Detail Specification respectively.

### 2.2 REFERENCE DOCUMENTS

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| ASTM E-668 | Practice for Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation Hardness Assurance Testing of Electronic Devices |
| ASTM E-1249 | Standard Practice for Minimising Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices Using Co 60 Sources |
| MIL-STD-883 | Method 1019, Ionizing Radiation (Total Dose) Test Procedure |
| MIL-HDBK-814 | Military Handbook: Ionizing dose and neutron hardness Assurance guidelines for microcircuits and semiconductor devices |

## 3 TERMS AND DEFINITIONS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition the following definitions and abbreviations are used:

### 3.1 DEFINITIONS

| | |
|---|---|
| Radiation Level and Lot Acceptance Doses | The test level used in device lot acceptance tests. It is derived from the calculated radiation exposure for a given application, multiplied by the radiation design margin considered appropriate. |
| In-Situ Testing | The testing of devices which are physically located in the irradiation exposure chamber during electrical measurements. Bias is continuously applied to the devices, except for momentary interruptions of bias during electrical measurements. Measurements are made during or after each radiation exposure. |
| Remote Testing | The testing of devices after removal from the irradiation chamber for measurement. The reasons for removal are of two kinds:<br>(a) Inability to pass signal leads from on-site measurement system into the irradiation chamber.<br>(b) Necessity of transporting samples to an off-site ("remote") measurement system.<br>The time intervals between exposure, measurement and re-exposure may be very different for (a) and (b). For (b), refer to the time interval for measurement, it may be necessary to extend the recommended intervals of 1 hour for measurement and 2 hours for re-exposure.<br>If devices have to be removed from their exposure sockets, then, during transport, the leads must be shorted together, either by insertion in conductive foam or by the use of an appropriate fixture. |
| Time-dependent effects | Effects of radiation exposure on electrical parameters which vary either with the time of exposure or after completion of the exposure. |
| Rebound | In MOS structures, a subset of TDE involving a net degradation of performance due to changes in trapped oxide charge and interface state density over periods of time of the order of several weeks. |
| Accelerated Ageing and Over-ageing | Use of elevated temperature and bias to accelerate TDE, especially rebound. If ageing gives excessive recovery of performance, this is termed over-ageing. |
| Level of Interest | The Level of Interest is a dose value having a specific significance for the test authority. The value may be the anticipated dose at a component location within a spacecraft, the average tolerance level or the minimum tolerance level required of a component. The maximum test level is usually higher than the Level of Interest to allow for design margins and lot to lot variability. |
| Enhanced Low Dose Rate Sensitivity | In some cases bipolar linear devices demonstrate increased electrical parameter degradation with decreasing dose rates. |
| True Dose Rate Effect | A true dose rate effect is observed if, for a given total dose exposure, the degradation after irradiation at low dose rate is different than the degradation at a higher dose rate followed by a room temperature anneal period at least equivalent to the low dose rate exposure time. |
| Total Ionising Dose Sensitivity | The level of Total Ionising Dose (TID) at which a part exceeds its parametric/functional requirements. |

### 3.2 ABBREVIATIONS

| | |
|---|---|
| ESCIES | European Space Components Information Exchange System (See https://escies.org) |
| PIE | Post-irradiation effects |
| TDE | Time-dependent effects |
| ELDRS | Enhanced Low Dose Rate Sensitivity |
| RADLAT | Radiation Lot Acceptance Testing |
| RVT | Radiation Verification Testing |
| TIDS | Total Ionising Dose Sensitivity |

## 4 EQUIPMENT AND GENERAL PROCEDURES

The equipment shall consist of the radiation source, electrical parameter measurement system, test circuit board(s), cabling, interconnect board or switching system, test fixtures and appropriate dosimetry instruments.

Precautions shall be taken to obtain an electrical parameter measurement system which, by use of sufficient insulation, ample shielding, satisfactory grounding etc. shall yield suitably low levels of interference from mains power supplies and other sources of noise and leakage. The magnitude of interference from each of these items shall be sufficiently small so as not to affect any electrical measurement.

### 4.1 RADIATION SOURCE AND DOSIMETRY

### 4.1.1 Sources for Ionisation Damage

The radiation source used for the test shall be the field of a Cobalt 60 gamma source or an electron accelerator beam. Alternative sources that can be correlated to these sources may be used but, in the case of dispute, the Cobalt 60 or electron accelerator methods shall govern. The dose at the device under test shall be measured to a resolution of better than 10% and the non-uniformity of the radiation field in the test area shall be a maximum of 10%. The field uniformity shall be verified if the geometry of the test setup is changed.

### 4.1.2 Cobalt 60 Source

The gamma-ray dose rate of a Cobalt 60 source shall be calibrated in accordance with the requirements of ESCC Basic Specification No. 21500 to 5% or better. Dosimetry shall be traceable to national standards. Corrections for source decay shall be made once per month.

Test specimens shall be surrounded by equilibrium material which will minimise dose enhancement from low-energy scattered radiation by producing charged-particle equilibrium. If it can be demonstrated that low-energy scattered radiation does not cause dosimetry errors due to dose enhancement, then the equilibrium material may be omitted. For equilibrium, the use of a container of at least 1.5mm Pb with an inner lining of at least 0.7mm Al is recommended.

### 4.1.3 Electron Source

The electron source used for the test shall be a steady-state type. The electron energy shall be sufficient to penetrate the package and shall be ≥1 MeV at the semiconductor die.

The electron beam shall be monitored with a Faraday Cup and a current integrator (which may also be used to terminate the radiation at the specified fluence level). Alternative monitoring methods may be used, but, in the case of dispute, the Faraday Cup and current integrator method shall govern. In the case of ionisation effects, the fluence for a given electron energy shall be accurately converted to Gy(Si) (and/or rad(Si)) at chip level, taking into account potential dose enhancement effects due to the component's package, high-Z materials, etc. The dose profile of the beam shall be uniform within ±10% for a distance of at least 24mm or 5 times the chip diagonal, whichever is the greater.

## 4.2 RADIATION LEVELS

The test devices shall be exposed to within 10% of the specified radiation dose level(s) or fluence(s). If multiple exposures are required for a set of test devices, then:

(a) The post-irradiation electrical parameter measurements shall be performed after each exposure.

(b) In the event of ESCC qualification and procurement lot acceptance (Section 6), there shall be a minimum of 3 exposures for which the increments in dose level(s) are specified in the table below. This table also shows the ESCC radiation hardness assurance (RHA) qualification levels. The radiation level shall be specified in the Test Plan.

| Letter | RHA Level (TID) | | Corresponding Exposure Levels | |
|---|---|---|---|---|
| | rad(Si) | Gy(Si) | rad(Si) | Gy(Si) |
| M | 3k | 30 | 1.5k / 3k / 4.5k | 15 / 30 / 45 |
| D | 10k | 100 | 5k / 10k / 15k | 50 / 100 / 150 |
| E | 20k | 200 | 10k / 20k / 30k | 100 / 200 / 300 |
| P | 30k | 300 | 15k / 30k / 45k | 150 / 300 / 450 |
| F | 50k | 500 | 25k / 50k / 75k | 250 / 500 / 750 |
| R | 100k | 1000 | 50k / 100k / 150k | 500 / 1000 / 1500 |
| A | 300k | 3000 | 150k / 300k / 450k | 1500 / 3000 / 4500 |
| G | 500k | 5000 | 250k / 500k / 750k | 2500 / 5000 / 7500 |
| H | 1000k | 10000 | 500k / 1000k / 1500k | 5k / 10k / 15k |

(c) In the event of ESCC evaluation and testing outside of an ESCC context, refer to Sections 5 and 7 respectively for radiation levels and intermediate steps.

## 4.3 RADIATION DOSE RATES

The Dose Rate shall be specified in the Test Plan. The dose rate shall be held constant within 10% during a given radiation exposure. Dose rates shall be chosen in such a way that the errors in dose coming from timing errors and initial beam adjustment are kept below 5%.

Two dose rate windows are specified:

Window 1 ("Standard Rate"): 0.36 to 180 krad(Si)/hour (3.6 to 1800 Gy(Si)/hour)

Window 2 ("Low Rate"): 36 to 360 rad(Si)/hour (0.36 to 3.6 Gy(Si)/hour)

Alternative dose rate windows may be agreed by the ESCC Executive (prior to the commencement of evaluation or qualification testing), or by the Orderer in the case of procurement.

Window 2 shall be used when strong time-dependent effects and/or true dose rate effects (e.g. ELDRS) are identified or suspected.

## 4.4 TEMPERATURE REQUIREMENTS

The devices under test shall be irradiated in an ambient temperature of +20 ±10°C which shall not vary by more than 3°C during the irradiation exposure. The room temperature annealing of the devices shall not differ by more than 5°C from the irradiation environment but shall not exceed 30°C, to minimize annealing. Electrical measurements shall be performed at the temperature specified in the Detail Specification for Electrical Measurements at Room Temperature. If the devices are transported to and from a remote electrical measurement site, the temperature of the test devices during transport shall not be allowed to increase by more than 10°C with respect to the temperature of the irradiation environment.

## 4.5 ELECTRICAL MEASUREMENT SYSTEMS

All instruments used for the electrical measurements shall have the stability, accuracy and resolution required for accurate measurement of the electrical parameters of the test devices as given in the Detail Specification. Any parts of the system required to operate within the irradiation chamber shall be insensitive to the required accumulated test doses or be shielded until that condition is achieved.

## 4.6 TEST FIXTURES

Devices to be irradiated shall be mounted on test circuit boards together with any associated circuitry necessary for application of bias during irradiation or for in-situ measurements. Other than devices under test, components that are placed on the board(s) shall be insensitive to the required accumulated test doses or be shielded so that that condition is achieved.

For these tests, the device terminals shall be electrically connected as prescribed in the Test Plan and/or Detail Specification. The geometry and materials of the completed board(s) shall allow uniform irradiation of the devices under test. If the radiation beam is unidirectional then, unless otherwise specified, the beam shall be perpendicular to the diffusion face of the semiconductor chip.

Design and construction practices shall be used to prevent damage by oscillation, and to minimise external noise pick-up and leakage currents and to obtain accurate measurements of device parameters. Only sockets which are radiation-resistant and do not exhibit any significant leakages (relative to the devices under test) shall be used to connect devices and associated circuitry to the test board(s). Similar precautions shall be taken in respect of cabling and switching systems. All equipment used repeatedly in radiation fields shall be checked periodically for physical and/or electrical degradation.

To assess interference and leakage, a circuit board shall be connected to the entire system, with no test devices installed, all sources of noise and interference operative, but no radiation field applied. The current as measured for the specified bias between any 2 terminals on each empty socket shall not exceed 10% of the lowest current value given in the specification of pre-irradiation values.

## 4.7 TEST SET-UP AND SITE REQUIREMENTS

The test specification shall state whether electrical parameters shall be measured in the irradiation chamber (in-situ) or after the devices have been removed from the chamber ("remote"). In the case of applications for which TDE is important, the advantages of each method shall be carefully weighed against the disadvantages.

### 4.7.1 In-Situ Testing

Prior to being irradiated, each test device shall be checked for operation according to the Test Plan and/or Detail Specification. When the entire system is in place for the in-situ radiation test, it shall be checked for proper interconnections, leakage and noise level. The system shall be monitored for oscillations and current drain. The test devices shall remain in place on the test circuit board which itself shall remain in its irradiation location throughout the irradiation and measurement sequence (except for source types which require removal of the board from the irradiation location to end an irradiation).

To ascertain the proper operation and stability of the measurement system, a control device shall be measured with the measurement system before the insertion of test devices and again upon completion of the irradiation and measurement series after removal of the test devices.

### 4.7.2 Remote Testing

Unless otherwise specified in the Test Plan, all terminals of the device under test shall be shorted together after removal from the irradiation bias fixture. Before and after all electrical measurements on irradiated devices, the control devices shall be measured according to the Test Plan and/or Detail Specification requirements to confirm proper operation of the measurement system.

### 4.7.3 Bias Conditions

(This paragraph applies to the voltage applied to high impedance terminals such as gates of MOSFETS and reverse bias to junctions).

While connected to the bias fixture, the biasing condition for the test devices, including the values of voltage and duty cycle, shall be maintained and monitored to remain within 10% of the conditions specified in the Test Plan and/or the Detail Specification. If these limits are exceeded the test shall be void. Unless otherwise specified, the bias applied to the test devices shall be worst case conditions to produce the greatest radiation-induced damage to those devices. The specified bias shall be maintained at all times on each device until removal of the device except for the periods required for electrical parameter measurements. The worst-case bias condition shall be determined during the evaluation phase. Devices to be annealed shall be mounted on boards providing the same bias condition as used for irradiation.

## 4.8 TIME INTERVALS FOR MEASUREMENT

Unless otherwise specified, the time intervals given below shall be observed. Justifications for longer intervals shall be reported together with appropriate bias conditions to be used during transport and storage.

(a) The time interval from the completion of an exposure to the start of the measurement of parameters shall be a maximum of 1 hour.
(b) The time interval from the completion of an exposure to the start of the next exposure shall be a maximum of 2 hours.

## 5 PROCEDURES FOR EVALUATION TESTING

The device technology shall be evaluated thoroughly for variations and average levels of radiation effects. For high impedance device terminals, e.g. MOS gates, the influence of voltage value and duty cycles of bias shall be studied so as to determine the worst case bias condition. The applicability of shorted terminals for transport and storage shall be validated for non-CMOS technologies. Time dependent effects (TDE) shall be studied for MOS devices or those technologies having inherent MOS structures such as bipolar devices with oxide isolation. Cases of "rebound" in N-channel MOS elements or their equivalent in other devices shall be identified and reported explicitly. The significance of other cases of time-dependence for tests conducted at low dose rates shall be reported.

ELDRS shall be studied for devices that contain bipolar transistors and optoelectronics, by comparing at a given dose level, low dose rate test results (within the low dose rate window for discrete devices and ≤ 36 rad(Si)/hour for Integrated Circuits) with high dose rate test results (at least 2 orders of magnitude higher than low dose rate) on parts from the same wafer lot. A part is considered as ELDRS sensitive if the enhancement factor observed at the lower dose rate is greater than 1.5 on the median value of the most sensitive measured parameter.

Devices containing bipolar transistors and MOS elements (e.g. BiCMOS) shall be evaluated for both ELDRS and MOS specific effects.

## 5.1 EVALUATION IRRADIATION TEST PLAN

The test devices shall be irradiated in accordance with an approved Test Plan. The Test Plan shall contain all relevant information according to the Test Plan Template and Test Plan Notes provided in the ESCC Forms section of https://escies.org. All electrical parameters to be tested and biasing conditions shall be clearly described. The evaluation plan shall be designed to determine worst-case bias conditions, to detect the degree of variation in radiation response from wafer lot to lot and the degree of time dependence of the radiation response. The use of Process Validation modules and representative test structures is encouraged for the evaluation stage.

## 5.2 SAMPLE SELECTION

A minimum sample of 10 test devices shall be selected at random from different wafers and wafer locations from a minimum of two different wafer lots, making a minimum of 20 samples in all. One additional sample shall be designated an "unirradiated control". For each wafer lot, the sample size for each unique set of test conditions as defined in the Test Plan shall be at least 5. As a minimum, the test conditions shall include biased and unbiased testing. The test samples shall have been screened to commercial or military grade and assembled in one of the final manufacturing packages (preferably with Kovar lids, if within the range of packages to be covered by evaluation and qualification). The devices shall originate from the same supplier, fabrication plant and processing line as intended for future hi-rel production.

## 5.3 SAMPLE SERIALISATION

Immediately after selection, each individual sample device shall be serialised to facilitate pre- and post-irradiation data identification and comparison. The system of marking shall be such as to ensure that the samples are clearly identified by:

(a) Date-code of the sample.
(b) Their individual identification.

## 5.4 RADIATION EXPOSURE AND TEST SEQUENCE

The sequence of steps for the radiation exposure and test sequence during technology evaluation shall be as given below. The Standard Dose Rate window shall be used unless otherwise specified. The value of bias voltage used shall not be altered between steps (c) and (g). The flow chart for the evaluation test sequence is given in Figure 1.

(a) Serialisation of all devices.

(b) Initial room temperature electrical characterisation of all devices, with special emphasis given to parameters monitored during/after irradiation. All measurements shall be read and recorded in the irradiation test report using the format provided in the ESCC forms section of ESCIES.

(c) Set-up of radiation source and bias of devices for irradiation as specified.

(d) Irradiation of devices until either the targeted ESCC radiation hardness assurance (RHA) qualification level is reached or functional failure (up to a maximum of 1.5Mrad(Si)) occurs. Multiple exposures shall be used, with monitoring of electrical parameters in between. 5 intermediate datapoints shall be aimed for prior to the level of interest.

(e) Post irradiation electrical characterisation should start within 1 hour of completion of exposure and the period between two irradiation steps shall be less than 2 hours. Control device parameters shall also be measured.

(f) Room temperature anneal (as defined in Para. 4.4) under bias (see Note 1). Unless otherwise specified, parameters shall be remeasured 24, 48 and 168 hours after completion of the final exposure.

(g) Accelerated ageing under bias (see Note 1). Devices shall be baked at +100 ±5°C under bias for 168 hours. Alternative conditions are allowed if these conditions have been demonstrated to cause equal or greater rebound effects (e.g. degradation in speed, timing and output drive). Lower temperatures and times are required if the above ageing conditions have been demonstrated to produce excessive performance recovery.

(h) Final room temperature characterisation of all devices.

**NOTES:**

1. Devices irradiated unbiased shall remain unbiased during steps (f) and (g).

## 5.5 ELECTRICAL MEASUREMENTS

The following electrical measurements are required:

(a) Initial electrical measurements shall be performed as specified in Note 1.

(b) Electrical measurements at intermediate points and/or at the end of exposure shall be performed as specified in Note 2.

(c) Final electrical measurement shall be performed as specified in Note 1.

**NOTES:**

1. Electrical test parameters shall be those of “Room Temperature Electrical Measurements” in the ESCC Detail Specification, if existing, or specified parameters in the Evaluation Test Plan expected to form the subsequent basis for such measurements.
2. Electrical test parameters shall as a minimum be those of “Electrical Measurements for Total Dose Radiation Testing” in the Detail Specification, if existing, or those specified with test conditions in the Irradiation Test Plan and expected to form the subsequent basis for such measurements.

### 5.6 REPORTING OF EVALUATION

Electrical test results and other observations shall be collected in a test report. Recommendations regarding the form of the tests in the next phase shall be given, including the requirements for:

(a) Worst case bias.
(b) Room temperature anneal times.
(c) Accelerated ageing temperature and time for MOS devices.
(d) Sample size.
(e) Detection of wafer lot to lot variation in radiation response
(f) A goal for Lot Acceptance Dose, i.e. the specified values of dose rates and multiple exposure requirements.
(g) Parameters and conditions to be entered in the “Electrical Measurements for Total Dose Radiation Testing” section of the Detail Specification.

## 6 PROCEDURES FOR QUALIFICATION AND PROCUREMENT LOT ACCEPTANCE

### 6.1 GENERAL

Knowledge of the absolute value and statistical spread of radiation tolerance in a device production line shall be established by qualification of a manufacturer/device type for a given radiation dose value under given conditions. For devices which are qualified, lot acceptance tests shall be performed on each wafer lot, in order to control the statistical spread and ensure compliance with the qualification level. For devices which are not qualified to a given radiation level, lot acceptance testing is performed to ensure that, within statistical limits, the procurement lot meets the requirements of the purchase order.

### 6.2 TEST PLAN

The test devices shall be irradiated in accordance with the Test Plan. The Test Plan shall essentially contain all information according to the Test Plan Notes provided in the ESCC Forms section of ESCIES. All electrical parameters to be tested and biasing conditions shall be clearly described. The plan shall be designed to establish qualification and lot acceptance of a specific type and to maintain awareness of (a) variation in radiation response from wafer lot to wafer lot and (b) of time dependence of the radiation response as reflected in the performance of a specific device type.

For devices identified as ELDRS sensitive during the Evaluation phase (Section 5), the dose rate shall be ≤36 rad(Si)/hour for Integrated Circuits and be within the Low Dose Window for discrete bipolar devices.

## 6.3 SAMPLE SELECTION

Unless otherwise specified in the Test Plan, a minimum of 11 test samples shall be selected at random from the part of the wafer lot intended to form the basis of the qualification or procurement lot at any stage during Production Control per Chart F2 of the Generic Specification. One sample shall be designated an “unirradiated control”. The sample size for each unique set of test conditions as defined in the Test Plan shall be at least 5. At least 5 samples shall be irradiated unbiased. Each wafer shall contribute at least 1 test sample to the irradiated group. All sample devices shall have met all of the requirements of the applicable ESCC Generic and/or Detail Specifications up to the point of the selection and be individually identifiable for the purpose of pre- and post-irradiation identification and comparison. Where evaluation testing has shown significant wafer to wafer variability then wafer by wafer acceptance may be required and the appropriate sampling plan shall be specified, based on the results of evaluation testing.

The devices shall then be submitted to radiation tests in accordance with the test sequence specified in the Radiation Exposure and Test Sequence (Para. 6.5).

## 6.4 SAMPLE SERIALISATION

Immediately after selection, each individual sample device shall be serialised to facilitate pre- and post-irradiation data identification and comparison. The system of marking shall be such as to ensure that the samples are clearly identified by:

(a) Date-code of the sample.
(b) Their individual serial number.

## 6.5 RADIATION EXPOSURE AND TEST SEQUENCE

The sequence of steps for the radiation exposure and test sequence for qualification and lot acceptance testing shall be as below. The flow chart for qualification and lot acceptance testing is given in Figure 2.

(a) Serialisation of all devices.
(b) Initial room temperature electrical testing of all devices, with special emphasis given to parameters monitored during/after irradiation. All monitored parameters shall be recorded in the irradiation test report.
(c) Set-up of radiation source and bias of devices for irradiation as specified.
(d) Irradiation of devices to the specified exposure level.
(e) Post-radiation electrical tests on exposed devices and control device.
(f) Multiple exposures are required (see Table in Para. 4.2), therefore steps (c), (d) and (e) shall be repeated until the specified Acceptance Dose Value specified in the Test Plan is reached. A maximum of 2 hours between consecutive irradiation exposures is allowed.
(g) 24 hour, room temperature anneal (as defined in Para. 4.4) under bias (see Note 1), followed by room temperature electrical testing of the exposed and control devices performed no more than two hours after completion of the room temperature anneal.
(h) Accelerated ageing under bias (see Note 1). Devices shall be baked at +100 ±5°C, or less if specified, under bias for 168 hours. Alternative conditions are allowed if these conditions have been demonstrated to cause equal or greater rebound effects (e.g. degradation in speed, timing and output drive). See Note 2.
(i) Final room temperature electrical characterisation.

**NOTES:**

1. Devices irradiated unbiased shall remain unbiased during steps (g) and (h).
2. When evaluation testing has clearly demonstrated that the device under test does not exhibit TDE, step (h) may be excluded with justification given in the Test Plan.

### 6.6 ELECTRICAL MEASUREMENTS

The parameters to be measured, their degree of allowable degradation and the test conditions shall be as stated below. In the event that the degradation exceeds the allowable limits at any measurement point on any of the tested parts, other than initial measurement, the lot shall be rejected. If any part exceeds any allowable limit at the initial measurement, that part shall be rejected and replaced by an acceptable part for the sample selection for radiation test.

(a) Initial electrical measurements shall be performed in accordance with "Room Temperature Electrical Measurements" of the Detail Specification.
(b) Electrical measurements at intermediate points and at the end of exposure shall be performed in accordance with "Electrical Measurements for Total Dose Radiation Testing" of the Detail Specification.
(c) Final electrical measurements shall be performed in accordance with "Electrical Measurements for Total Dose Radiation Testing" of the Detail Specification

### 6.7 REPORTING

Electrical test results and other observations from qualification and lot testing shall be collected in a test report. Recommendations derived from the qualification testing shall be given for procurement lot acceptance testing. Recommendations shall be entered in "Electrical Measurements for Total Dose Radiation Testing" of the Detail Specification. In the event of significant findings during lot acceptance testing recommendations shall be made for the modification of future lot acceptance tests.

### 6.8 CONFIGURATION CONTROL

In case of an ESCC evaluation and qualification and RVT or RADLAT of an ESCC qualified component the manufacturer is responsible for keeping Radiation Test Plans and Radiation Test Reports under configuration control. Copies are to be provided to the ESCC Executive in unencrypted electronic format.

In case of any other procurement with RADLAT the Radiation Test Plan and Radiation Test Report are deliverable to the customer.

## 7 PROCEDURES FOR TESTING OUTSIDE OF AN ESCC CONTEXT

### 7.1 GENERAL

Evaluation tests are performed when the TIDS of a part is unknown.

RVTs or RADLATs are performed to ensure that, within statistical limits, the procured lot meets the applicable procurement specification requirements or the requirements of a specific application.

NOTE: Any part type tested according to Section 7 is not compliant with the ESCC evaluation and ESCC qualification test requirements and cannot be considered as ESCC evaluated or qualified.

## 7.2 TEST PLAN

The test devices shall be irradiated in accordance with the Test Plan. All electrical parameters to be tested and biasing conditions shall be clearly described. As a minimum, the Test Plan should contain all information according to the Test Plan Notes provided in the ESCC Forms section of https://escies.org.

The dose rate shall be:

(a) Within the Standard or Low Dose Rate window for MOS and CMOS devices,
(b) Within the Low Dose Rate window for devices containing bipolar transistors, or
(c) As justified by application and/or mission conditions.

## 7.3 SAMPLE SELECTION

A sample size of 5 devices per set of unique test conditions shall be used. However smaller sample sizes may be used if agreed by the customer. One additional sample shall be designated an “unirradiated control”.

The devices shall then be submitted to radiation tests in accordance with the test sequence specified in the Radiation Exposure and Test Sequence (Para. 7.5).

## 7.4 SAMPLE SERIALISATION

Immediately after selection, each individual sample device shall be serialised to facilitate pre- and post-irradiation data identification and comparison. The system of marking shall be such as to ensure that the samples are clearly identified by:

(a) Date-code of the sample.
(b) Their individual serial number.

## 7.5 RADIATION EXPOSURE AND TEST SEQUENCE

The sequence of steps for the radiation exposure and test sequence shall be as listed below. The flow chart is given in Figure 3.

(a) Serialisation of all devices.
(b) Initial room temperature electrical testing of all devices, with special emphasis given to parameters monitored during/after irradiation. All monitored parameters shall be recorded in the irradiation test report.
(c) Set-up of radiation source and bias of devices for irradiation as specified.
(d) Irradiation of devices to the specified exposure level.
(e) Post-radiation electrical tests on exposed devices and control device.
(f) A minimum of 5 exposures should be aimed for. However fewer exposure levels can be used if agreed upon by the customer. Repetition of steps (c), (d) and (e) shall be carried out after each exposure until the specified Acceptance Dose Value specified in the Test Plan is reached. A maximum of 2 hours between consecutive irradiation exposures is allowed.
(g) 24 hour, room temperature anneal (as defined in Para. 4.4) under bias (see Note 1), followed by room temperature electrical testing of the exposed and control devices performed no more than two hours after completion of the room temperature anneal.
(h) Accelerated ageing under bias (see Note 1). Devices shall be baked at +100 ±5°C, or less if specified, under bias for 168 hours. Alternative conditions are allowed if these conditions have been demonstrated to cause equal or greater rebound effects (e.g. degradation in speed, timing and output drive).
(i) Final room temperature electrical characterisation.

**NOTES:**

1. Devices irradiated unbiased shall remain unbiased during steps (g) and (h).

## 7.6 ELECTRICAL MEASUREMENTS

The parameters to be measured and the test conditions shall be as stated below. If any part exceeds any allowable limit at the initial measurement, that part shall be rejected and replaced by an acceptable part for the sample selection for radiation test.

(a) Initial electrical measurements shall be performed in accordance with the Test Plan.
(b) Electrical measurements at intermediate points and at the end of exposure shall be performed in accordance with "Electrical Measurements for Total Dose Radiation Testing" of the applicable procurement Specification.
(c) Final electrical measurements shall be performed in accordance with "Electrical Measurements for Total Dose Radiation Testing" of the applicable procurement Specification.

## 7.7 REPORTING

Electrical test results and other observations from the test shall be collected in a test report.

# 8 DOCUMENTATION

For each irradiation test to be performed, 2 sets of documents are required:

(a) A Test Plan (prior to irradiation testing) defining the detailed requirements of the irradiation testing to be performed.

(b) A Test Report giving the actual test conditions and test results. As a minimum the Test Report shall include the following:

- Part traceability information
  - Full part type number
  - Serial number
  - Date code
  - Wafer lot number
  - Package type and marking
  - Die picture
  - Part technology/process
  - Wafer number (if known)
  - Die fab facility (if known)

- Irradiation conditions
  - Test date
  - Irradiation facility and radiation source type
  - Irradiation test sequence with detail of irradiation and annealing steps
  - Dose rate(s)
  - Accuracy of the dose levels

- Bias conditions during irradiation with identification of samples per bias conditions

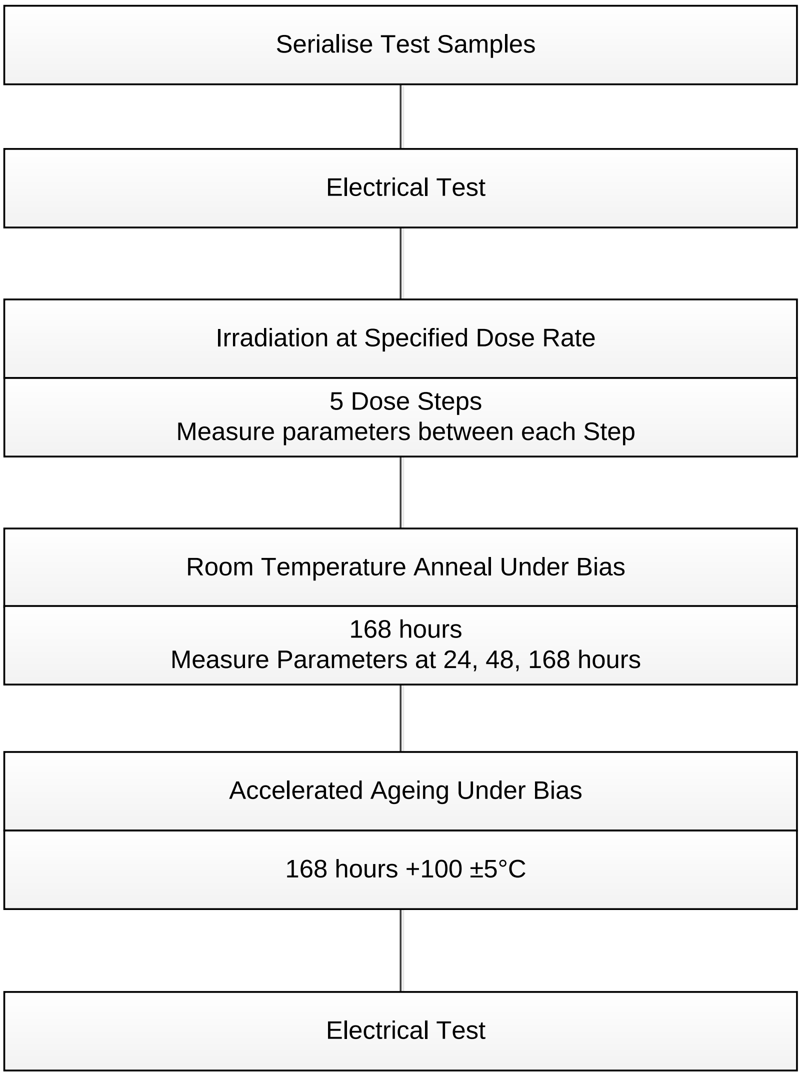
- Electrical measurements conditions and acceptable limits

- Test results (tabulated and figures) for each electrical parameter measured, showing the measurement results after each irradiation and annealing step of all irradiated parts and the control part

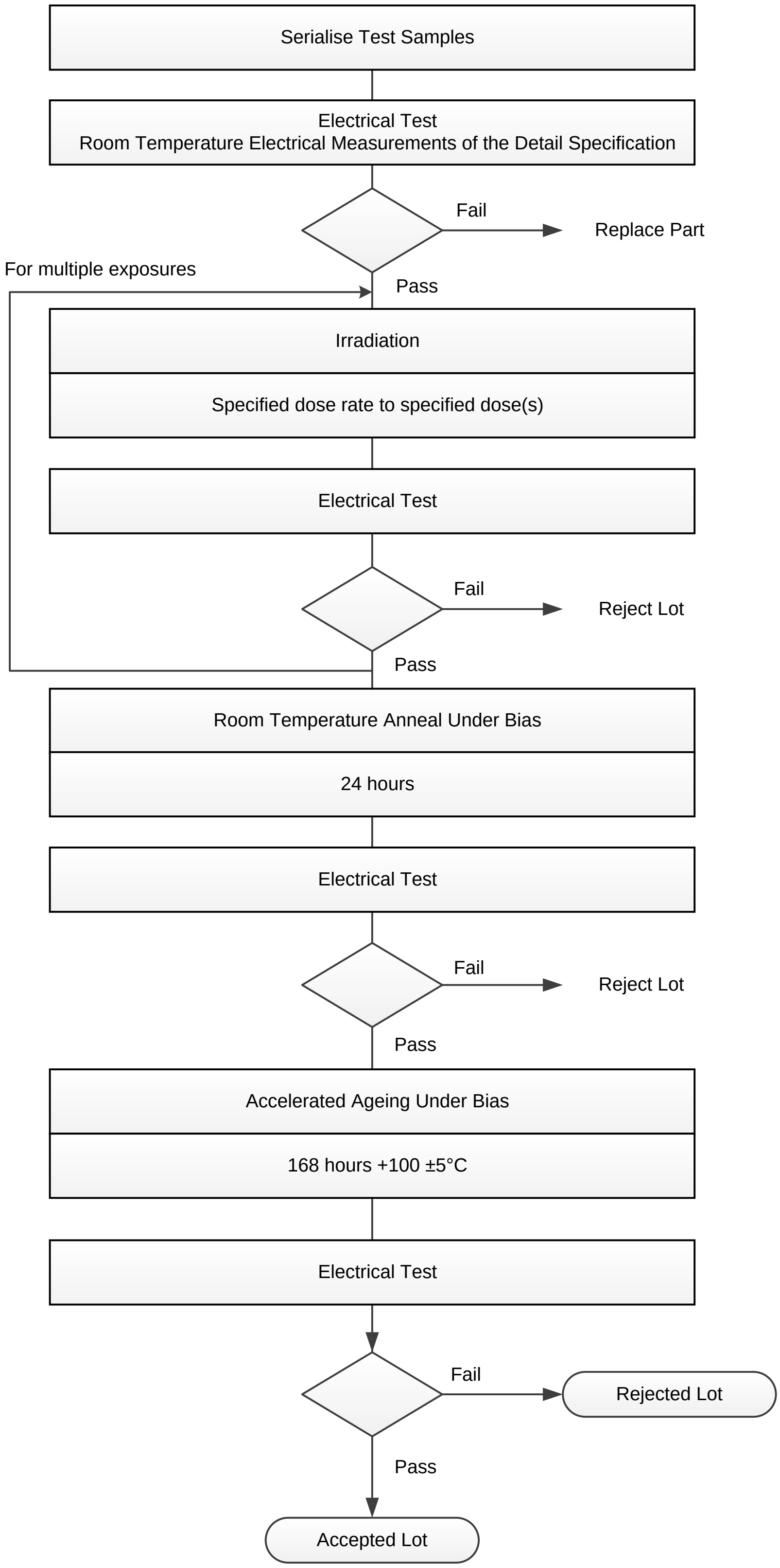
Any anomalies that occurred during the test shall be reported and fully described.

## 9 FIGURES

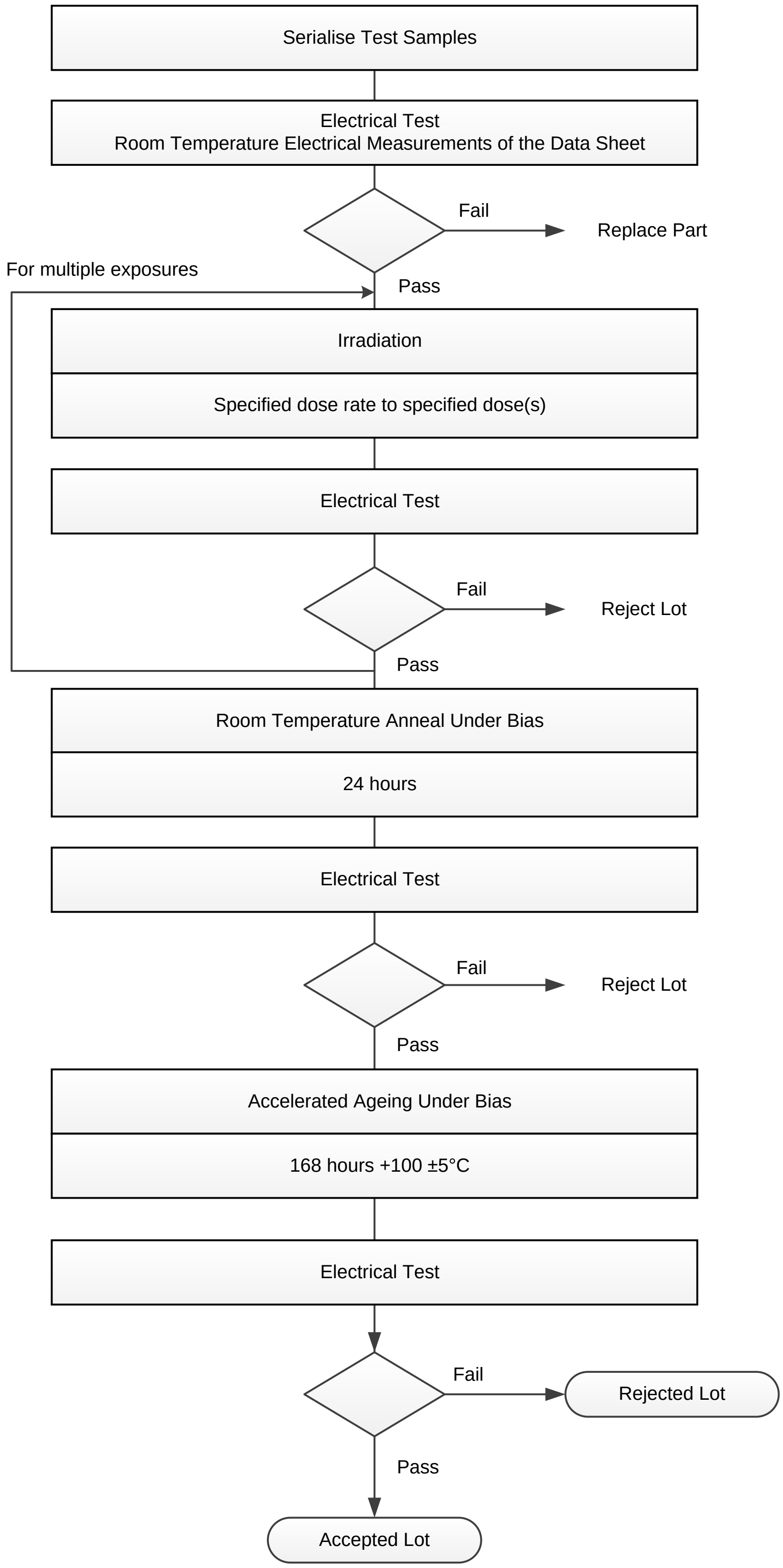
### 9.1 FIGURE 1 - FLOW CHART FOR EVALUATION TESTING



## 9.2 FIGURE 2 – FLOW CHART FOR QUALIFICATION AND LOT ACCEPTANCE TESTING



## 9.3 FIGURE 3 – FLOW CHART APPLICABLE OUTSIDE OF AN ESCC CONTEXT (NOTE 1)



**NOTES:**

1. The pass/fail criteria can be Project and/or application specific.