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MONOLITHIC MICROWAVE INTEGRATED CIRCUIT (MMIC) GaAs PHEMT D01PH

PROCESS FROM OMMIC

BASED ON TYPE CGY2135UH BARE DIE (K-BAND HIGH POWER AMPLIFIER)

ESCC Detail Specification No. 9012/005

Issue 1 November 2016





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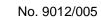




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1 **GENERAL**

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for the Microwave Monolithic Integrated Circuit (MMIC), in die form, K-Band High Power Amplifier, based on type CGY2135UH. The CGY2135UH, based on the GaAs PHEMT D01PH process from OMMIC, covers the frequency range from 18 to 23GHz. This document is based on, and should be read in conjunction with ESCC Generic Specification No. 9010, the requirements of which are supplemented herein.

1.2 <u>TYPE VARIANTS</u>

MMIC Variants of the basic type components specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the component specified here in, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The power dissipation de-rating curve is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the die and mechanical drawing specified herein are shown in Figure 2.

1.6 <u>FUNCTIONAL DIAGRAM</u>

The functional diagram, showing pad identification of the component specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and handling.

These chips are categorized as Class 0 with a Minimum Critical Path Failure Voltage of 50V for this Variant.

2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9010 for Monolithic Microwave Integrated Circuits (MMICs)
- (b) MIL-STD-883 Test Methods and Procedures for Microelectronics
- (c) ESCC No. 20600 Preservation, Packaging and Despatch of ESCC Components
- (d) ESCC No. 21300 Terms Definition, Abbreviations, Symbols and Units
- (e) ESCC No. 23800 Electrostatic Discharge Sensitivity Test Method

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

RTH (J-B) =Thermal Resistance, Junction to Backside of bare die

TABLE1(a) - TYPEVARIANTS

| (1) VARIANT | (2) TYPE | (3) CASE | (4) FIGURE | (5) PAD METALLISATION AND THICKNESS OF TOP LAYER | (6) BACKSIDE FINISH (METALLISATION AND THICKNESS) |
|----------------|-------------|-------------|---------------|---|--|
| 01 | CGY2135UH | CHIP | 2 | Au, 1μm | Au, 3.5μm |

TABLE 1(b) - MAXIMUM RATINGS (1)

| No. | CHARACTERISTICS | SYMBOL | MAXIMUM RATINGS | UNIT | REMARKS |
|-----|---|-----------------------------------|---------------------------|------|---|
| 1 | RF input power | P _{IN} | +18 | dBm | CW mode |
| 2 | Drain bias voltage | V _{Da} , V _{Db} | 5.5 | V | |
| 3 | Gate bias voltage | V _{Ga} , V _{Gb} | -2.5 < V _G < 0 | V | |
| 4 | Junction temperature | Tj | +175 | °C | |
| 5 | Drain bias current (V _{Ga} , V _{Gb} tuned) | I _{Da} , I _{Db} | 800 | mA | each |
| 6 | Operating Temperature Range | Ta | -40 to +85 | °C | T _j < 175°C |
| 7 | Storage Temperature Range | T _{stg} | -55 to +150 | °C | |
| 8 | Soldering Temperature (2) | T _{sol} | < +300 during 1 min | °C | AuSn80/20 |
| 9 | Thermal Resistance (3) | RTH (J-B) | 8 | °C/W | Junction to backside at 85°C |
| 10 | Dissipated power (4), (5) | P _{diss} | 6.3 | W | Maximum DC power (T _j < 175°C) |

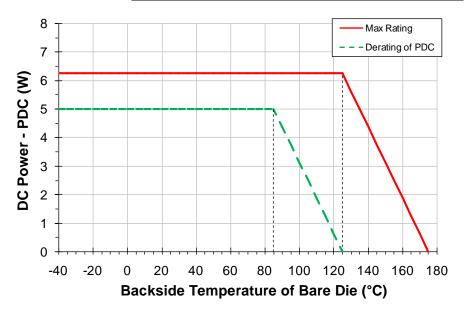
NOTES

- 1. Operation of this device above any one of these parameters may cause permanent damage.
- 2. During bonding or soldering, temperatures higher than 300°C should not be applied longer than 1 min.
- 3. For bare die junction to backside. Not a true maximum rating for information only.
- 4. For the assembled chip the relevant substrate or package should be taken into account.
- 5. For chip mounted in appropriate package. Not a true maximum rating for information only.



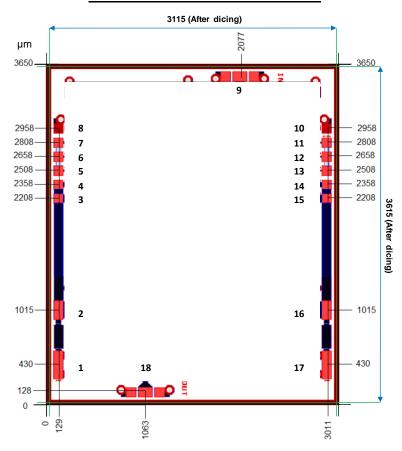
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FIGURE 1 – PARAMETER DERATING INFORMATION



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FIGURE 2 – PHYSICAL DIMENSIONS



| Pad number | Pad name | Description |
|------------|------------|------------------------|
| 1,8,10,17 | GND Ground | |
| 2,3,4 | VDa | Drain supply voltage a |
| 5,6,7 | VGa | Gate supply voltage a |
| 9 | IN | RF input |
| 11,12,13 | VGb | Gate supply voltage b |
| 14,15,16 | VDb | Drain supply voltage b |
| 18 | OUT | RF output |

NOTES

All dimensions are in micrometers

Chip size = $3650 \times 3150 \mu m^2$ before dicing ($3615 \times 3115 \mu m^2$ after dicing)

Chip thickness =100µm

RF pads $(9, 18) = 100 \times 150 \mu m^2$

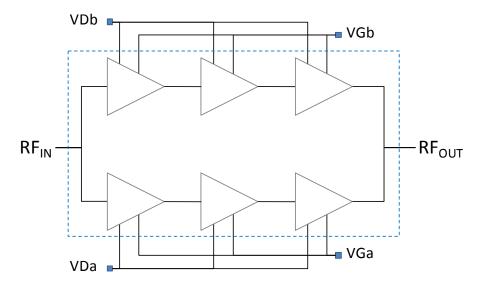
DC pads $VGx = 100 \times 100 \mu m^2$

DC pads $VDx = 100 \times 200 \mu m^2$

Chip width and length are given with a tolerance of \pm 5 μ m



FIGURE 3 – FUNCTIONAL DIAGRAM





4 **REQUIREMENTS**

4.1 GENERAL

The complete requirements for procurement of the naked MMIC die specified herein shall be as stated in this specification and ESCC Generic Specification No. 9010 for Monolithic Microwave Integrated Circuits (MMIC).

The test requirement for the MMIC lot validation shall be performed on mounted MMIC samples submitted to Burn-in and electrical measurements CHART III(b) and Lot Acceptance tests level 2 CHART V.

Deviations from the Generic Specification applicable to this specification only, are listed in Para.4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the MMIC chip reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

- 4.2.1 <u>Deviations from Production Control Wafer Lot Acceptance</u>
 - (a) Total Dose Radiation Testing: not required.
- 4.2.2 <u>Deviations from Production Control Wafer screening (CHART II(a))</u>
 - (a) Para.9.5.2.1: applicable on 5 bare dies assembled on appropriate substrate.
- 4.2.3 Deviations from Production Control Wafer acceptance testing (CHART III(a))
 - (a) Para.9.7.1 and 9.7.2 only applicable.
- 4.2.4 <u>Deviations from Final Production Tests (Chart II(b))</u>
 - (a) Chart II(b) shall not be performed.
- 4.2.5 <u>Deviations from Burn-in and Electrical Measurements (Chart III(b))</u>
 - (a) Para.9.15: shall not be performed.
 - (b) Para.9.16: shall apply as per condition MIL-STD-883, Test Method 1015, Condition 'B'. Duration shall be 240 hours at T_a = 125°C or equivalent T_a as per table 1 of MIL-STD-883, Test Method 1015. Junction temperature for Burn-in shall not exceed Tj = 175°C.
 - (c) Para.9.5.2.2: shall not be performed.
- 4.2.6 <u>Deviations from Qualification Tests (Chart IV)</u>

Chart IV shall not be performed.

4.2.7 Deviations from Lot Acceptance Tests (Chart V)

Chart V Level 2 - Endurance Subgroup plus electrical Subgroup shall apply.

Environmental / Mechanical Subgroups shall not be performed.

Deviations from the applicable Chart V level 2 to this specification are listed herein.

- (a) Level 3: Electrical measurements at room and high and low temperatures (-40°C / +85°C) on 3 samples per qualification lot shall be performed. Components Assembly and Capability Tests shall not be performed.
- (b) Level 3 Special testing para. 9.27, shall not be performed.



(c) Level 2 Endurance Subgroup shall be performed on 10 samples. The operating life test duration shall be 1,000 hours minimum at T_a = 125°C or equivalent T_a as per table 1 of MIL-STD-883, Test Method 1005. Junction temperature for operating life test shall not exceed Tj = 175°C.

4.3 <u>MECHANICAL REQUIREMENTS</u>

4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the components specified herein is negligible.

4.3.3 Terminal Strength

(a) Shall not be performed.

4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESCC Generic Specification No.9010. The test conditions shall be as described in MIL-STD-883, Test Method 2011, cond. D.

- (a) Condition: 'D'.
- (b) Bond Strengths: 20 wires (5 dies, 4 wires per die, No defect allowed)

4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESCC Generic Specification No.9010. The test conditions shall be as described in MIL-STD-883, Test Method 2019.

(a) Minimum acceptable on die shear strengths: 2.5kg (on 5 parts, No defect allowed).

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified here into meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

Bond Pad Metallization and Back-side metallization is Au.

4.5 <u>MARKING</u>

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence shall be as follows:

(a) The ESCC Component Number.



- (b) Manufacturer name or Symbol.
- Manufacturer Part Number. (c)
- Traceability as defined in ESCC: Lot, Wafer, Date code ... (d)

The primary package shall bear an "ESD Sensitive" label.

4.5.2 ESCC Component Number

Each component shall bear the ESCC Component Number which shall be constituted and marked as follows:

Detail specification Number: 9012/005 Type Variant (see Table1 (a)) 01 Testing Level (B or C, as applicable) B

4.5.3 Pad Identification

Pad identification shall be as shown in Figure 2 of this specification.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESCC Basic Specification No. 21700.

4.5.5 Packaging

The components shall be packaged in ESD safe Waffle / Gel packs to ensure that they are isolated from electrical, mechanical and environmental damage. The packages for the MMICs shall be purged with nitrogen or evacuated, so that the MMICs are not exposed to external environment. The individual packages and the intermediate packages shall be fixed within shipping package, which shall be resistant to mechanical shocks, humidity and dust.

4.6 **ELECTRICAL MEASUREMENTS**

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_a = +25 \pm 3^{\circ}C$.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at +85°C (or maximum temperature as indicated in Figure 1 taking into account thermal resistance of package), and -40°C.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Table 2 and Table 3 of this specification are shown in Figure 4.

4.7 **BURN-IN TESTS**

Burn-in shall be done in accordance with Chart III(b) of ESCC Generic Specification No. 9010.

4.7.1 Parameter Drift Values

The parameter and drift values applicable to Burn-In are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_a = +25 ±3°C. The parameter drift



values applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 <u>Conditions for Burn-In</u>

The requirements for Burn-In are specified in Section 9 of ESCC Generic Specification No. 9010. The conditions for Burn-In shall be as specified in Table 5 of this specification.

4.7.3 <u>Electrical Circuit for Burn-In</u>

The circuit for use in performing the Burn-In test is shown in Figure 5 of this specification.

4.8 ENDURANCE TESTS (CHART V OF ESCC GENERIC SPECIFICATION NO. 9010)

4.8.1 <u>Electrical Measurements at Intermediate Points and on Completion of Endurance Tests</u>

The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 2 of this specification. Unless otherwise stated, the measurements shall be performed at $T_a = +25 \pm 3$ °C.

4.8.2 <u>Conditions for Operating Life Test (Part of Endurance Testing)</u>

The requirements for operating life testing are specified in Section 9 of ESCC Generic Specification No. 9010. The conditions for operating life testing are specified in Table 5 of this specification.

4.8.3 Electrical Circuit for Operating Life Test

The circuit for use in performing the operating life test shall be the same as shown in Figure 5 of this specification for burn-in.

4.9 <u>TOTAL DOSE IRRADIATION TESTING</u>

Not applicable.

4.10 SPECIAL TESTING

Not applicable.



<u>TABLE 2 – ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE OF NAKED DIE – DC & RF PARAMETERS</u>

| No | CHARACTERISTICS | CVMDOL | TECT COMPLETIONS | | LIMITS | | UNIT |
|-----|---------------------------------|------------------|---|------|--------|------|------|
| No. | CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| 1 | Frequency range | Freq | $V_{Da} = V_{Db} = 4V$ $I_{Da} = I_{Db} = 600mA (1)$ | 18 | | 23 | GHz |
| | | | 18GHz | | 24 | | |
| 2 | Linear Gain | Gp | 20.5GHz | | 25.5 | | dB |
| | | | 23GHz | | 26.5 | | |
| 3 | Input Return Loss | RLin | 18 - 23GHz | | 12 | | dB |
| 4 | Output Return Loss | RLout | 18 - 23GHz | | 12 | | dB |
| | Output Power @1dB compression | P _{1dB} | 18GHz | | 30.5 | | dBm |
| 5 | | | 20.5GHz | | 31 | | |
| | | | 23GHz | | 32 | | |
| | Saturated Power | P _{sat} | 18GHz | | 32 | | |
| 6 | | | 20.5GHz | | 32 | | dBm |
| | | | 23GHz | | 33 | | |
| | | | 18GHz | | 38 | | |
| 7 | Output 3rd intercept point (2) | OIP3 | 20.5GHz | | 38 | | dBm |
| | | | 23GHz | | 39 | | |
| | | | 18GHz | | 21 | | |
| 8 | Power Added EffIciency @P3dB | PAE | 20.5GHz | | 24 | | % |
| | @P30B | | 23GHz | | 31 | | |

NOTES

- $\overline{1.}$ V_{Ga} , V_{Gb} tuned to $I_{Da} = I_{Db} = 600$ mA ($I_{dq} = I_{Da} + I_{Db} = 1200$ mA)
- 2. Sample basis

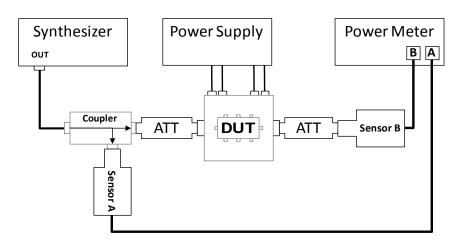


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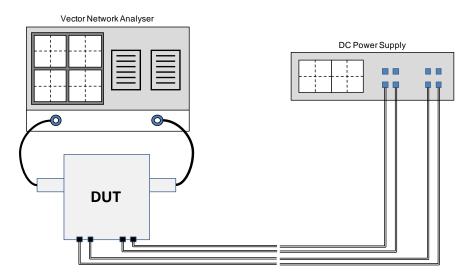
TABLE 3 - ELECTRICAL MEASUREMENTS AT LOW AND HIGH TEMPERATURE OF DUT IN JIG - DC & RF PARAMETERS

| No | CHARACTERISTICS | SYMBOL | TEST CONDITIONS | T | LINIT | |
|-----|--------------------------------|------------------|---|---------|---------|------|
| No. | | STIVIBUL | TEST CONDITIONS | -40°C | +85°C | UNIT |
| 1 | Frequency range | Freq | $V_{Da} = V_{Db} = 4V$ $I_{Da} = I_{Db} = 600 \text{mA}$ | 18 - 23 | 18 - 23 | GHz |
| 2 | Linear Gain | Gp | 20.5GHz | 27 | 23 | dB |
| 3 | Input Return Loss | RLin | 18 - 23GHz | 12 | 12 | dB |
| 4 | Output Return Loss | RLout | 18 - 23GHz | 12 | 12 | dB |
| 5 | Output Power @ 1dB compression | P _{1dB} | 20.5GHz | 32 | 30 | dBm |

FIGURE 4 - TEST CONFIGURATIONS FOR ELECTRICAL MEASUREMENTS [DUT IN JIG]



Power test set-up



S parameter test set-up

TABLE 4 – PARAMETER DRIFT VALUES

| No. | CHARACTERISTICS | SYMBOL | SPEC.AND/OR TEST METHOD | TEST CONDITIONS | LIMITS | UNIT |
|-----|-------------------------------|-----------------|----------------------------|--------------------|--------|------|
| 1 | Linear Gain | Gp | As per Table 2 | As per Table 2 | +/-1 | dB |
| 2 | Output Power @1dB compression | P1dB | As per Table 2 | As per Table 2 | +/-1 | dBm |
| 3 | Drain quiescent current (1) | I _{dq} | As per Table 2 | As per Table 2 | +/-20 | % |

NOTES

 $\overline{1.}$ $\overline{V}_{Da} = V_{Db} = 4V$ and $I_{dq} = I_{Da} + I_{Db}$

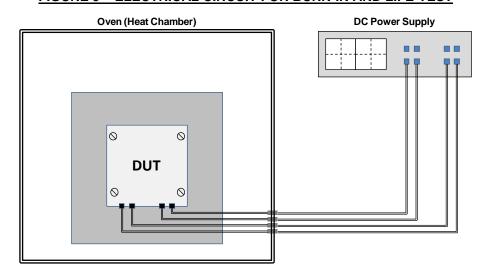
TABLE 5 – CONDITIONS FOR BURN-IN AND OPERATING LIFE-TESTS

| No. | CHARACTERISTICS | SYMBOL | VALUE | UNIT |
|-----|-------------------------|---------------------------------------|---------------|-------|
| 1 | Ambiant Temperature (1) | Ta | +125 | °C |
| 2 | Junction Temperature | Tj | ≤+175 | °C |
| 3 | Drain Current (2) | [I _{Da} ; I _{Db}] | [600 ; 600] | mA |
| 4 | Drain Voltage | $[\ V_{Da}\ ;\ V_{Db}\]$ | [4;4] | V |
| 5 | Duration for Burn-in | | 240 | hours |
| 6 | Duration for Life-Test | | 1000 | hours |

NOTES

- Junction temperature shall not exceed $T_j = +175$ °C.
- 2. Drain quiescent current $I_{dq} = I_{Da} + I_{Db} = 1200 \text{mA}$.

FIGURE 5 – ELECTRICAL CIRCUIT FOR BURN-IN AND LIFE-TEST





APPENDIX A AGREED DEVIATIONS FOR OMMIC TECHNOLOGIES

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|----------------------|---|
| Mil-Std-883 and ESCC | OM-CI-PR-CT-CO/005/IG Visual inspection Specification for GaAs MMIC (Internal OMMIC specification for Visual inspection; based on Mil-Std-883 and ESCC 2045010) |