MONOLITHIC MICROWAVE INTEGRATED CIRCUIT (MMIC) GaAs PHEMT D01PH

PROCESS FROM OMMIC

BASED ON TYPE CGY2145UH BARE DIE (LOW NOISE WIDE BAND AMPLIFIER)

ESCC Detail Specification No. 9012/006

Issue 1	November 2016

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

European Space Agency, Copyright © 2016. All rights reserved.

The European Space Agency disclaims any liability or responsibility, to any person or entity, with respect to any loss or damage caused, or alleged to be caused, directly or indirectly by the use and application of this ESCC publication.

This publication, without prior permission of the European Space Agency and provided it is not used for a commercial purpose, may be:

- copied in whole, in any medium, without alteration or modification.
- copied in part, in any medium, provided that the ESCC document identification, comprising the ESCC symbol, document number and document issue, is removed.

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1	GENERAL	6
1.1	SCOPE	6
1.2	TYPE VARIANTS	6
1.3	MAXIMUM RATINGS	6
1.4	PARAMETER DERATING INFORMATION	6
1.5	PHYSICAL DIMENSIONS	6
1.6	FUNCTIONAL DIAGRAM	6
1.7	HANDLING PRECAUTIONS	6
2	APPLICABLE DOCUMENTS	6
3	TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS	7
4	REQUIREMENTS	11
4.1	GENERAL	11
4.2	DEVIATIONS FROM GENERIC SPECIFICATION	11
4.2.1	Deviations from Production Control – Wafer Lot Acceptance	11
4.2.2	Deviations from Production Control – Wafer screening (CHART II(a))	11
4.2.3	Deviations from Production Control – Wafer acceptance testing (CHART III(a))	11
4.2.4	Deviations from Final Production Tests (Chart II(b))	11
4.2.5	Deviations from Burn-in and Electrical Measurements (Chart III(b))	11
4.2.6	Deviations from Qualification Tests (Chart IV)	11
4.2.7	Deviations from Lot Acceptance Tests (Chart V)	11
4.3	MECHANICAL REQUIREMENTS	12
4.3.1	Dimension Check	12
4.3.2	Weight	12
4.3.3	Terminal Strength	12
4.3.4	Bond Strength	12
4.3.5	Die Shear	12
4.4	MATERIALS AND FINISHES	12
4.5	MARKING	12
4.5.1	General	12
4.5.2	ESCC Component Number	13
4.5.3	Pad Identification	13
4.5.4	Traceability Information	13
4.5.5	Packaging	13
4.6	ELECTRICAL MEASUREMENTS	13
4.6.1	Electrical Measurements at Room Temperature	13

4.6.2 Electrical Measurements at High and Low Temperatures 13
4.6.3 Circuits for Electrical Measurements 13
4.7 BURN-IN TESTS 13
4.7.1 Parameter Drift Values 13
4.7.2 Conditions for Burn-In 14
4.7.3 Electrical Circuit for Burn-In 14
4.8 ENDURANCE TESTS (CHART V OF ESCC GENERIC SPECIFICATION NO.9010) 14
4.8.1 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests 14
4.8.2 Conditions for Operating Life Test (Part of Endurance Testing) 14
4.8.3 Electrical Circuit for Operating Life Test 14
4.9 TOTAL DOSE IRRADIATION TESTING 14
4.10 SPECIAL TESTING 14

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for the Microwave Monolithic Integrated Circuit (MMIC), in die form, Low Noise Wide Band Amplifier, based on type CGY2145UH.The CGY2145UH, based on the GaAs PHEMT D01PH process from OMMIC, covers the frequency range from 0.5 to 45GHz.This document is based on, and should be read in conjunction with ESCC Generic Specification No.9010, the requirements of which are supplemented herein.

1.2 TYPE VARIANTS

MMIC Variants of the basic type components specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the component specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

See Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the die and mechanical drawing specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing pad identification of the component specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and handling.

These chips are categorized as Class 0 with a Minimum Critical Path Failure Voltage of 50V for this Variant.

2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9010 for Monolithic Microwave Integrated Circuits (MMICs).
(b) MIL-STD-883 Test Methods and Procedures for Microelectronics.
(c) ESCC No. 20600 Preservation, Packaging and Despatch of ESCC Components.
(d) ESCC No. 21300 Terms Definition, Abbreviations, Symbols and Units.
(e) ESCC No. 23800 Electrostatic Discharge Sensitivity Test method.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

RTH (J-B) =Thermal Resistance, Junction to Backside.

TABLE 1(a) – TYPE VARIANTS

(1) VARIANT	(2) TYPE	(3) CASE	(4) FIGURE	(5) PAD METALLISATION AND THICKNESS OF TOP LAYER	(6) BACKSIDE FINISH (METALLISATION ANDTHICKNESS)
01	CGY2145UH	CHIP	2	Au,1µm	Au,3.5µm

TABLE 1(b) - MAXIMUM RATINGS (1)

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	RF input power	P_{IN}	+4	dBm	CW mode
2	Drain bias voltage	V_{DD}	8	V	
3	Gate bias voltage 1	V_{G1}	-5 < Vg <0	V	
4	Gate bias voltage 2	V_{G2}	-5 < Vg <4	V	
5	Junction temperature	T_j	+175	°C	
6	Drain bias current	I_{DD}	150	mA	Total current of the circuit
7	Operating Temperature Range	T_a	-20 to +85	°C	
8	Storage Temperature Range	T_{stg}	-55 to +150	°C	
9	Soldering Temperature (2)	T_{sol}	< +300 during 1 min	°C	AuSn 80/20
10	Thermal Resistance (3)	RTH(J-B)	22	°C/W	Junction to backside at 85°C
11	Dissipated power (4), (5)	P_{diss}	1.2	W	Maximum DC power (Tj < 175°C)

NOTES

1. Operation of this device above any one of these parameters may cause permanent damage.
2. During bonding or soldering, temperatures higher than 300ºC should not be applied longer than 1 min.
3. For bare die junction to backside. Not a true maximum rating-for information only.
4. For the assembled chip the relevant substrate or package should be taken into account.
5. For chip mounted in appropriate package. Not a true maximum rating-for information only.

FIGURE 1 – PARAMETER DERATING INFORMATION

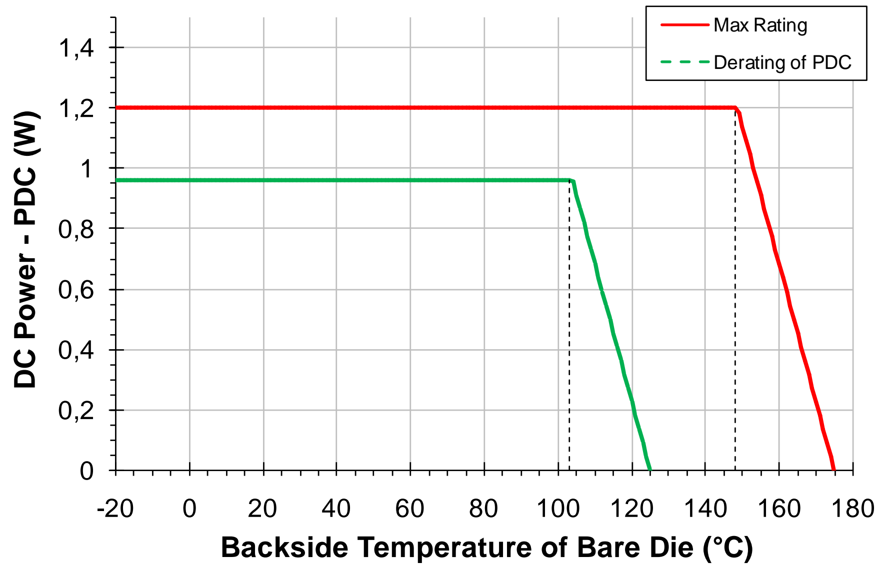
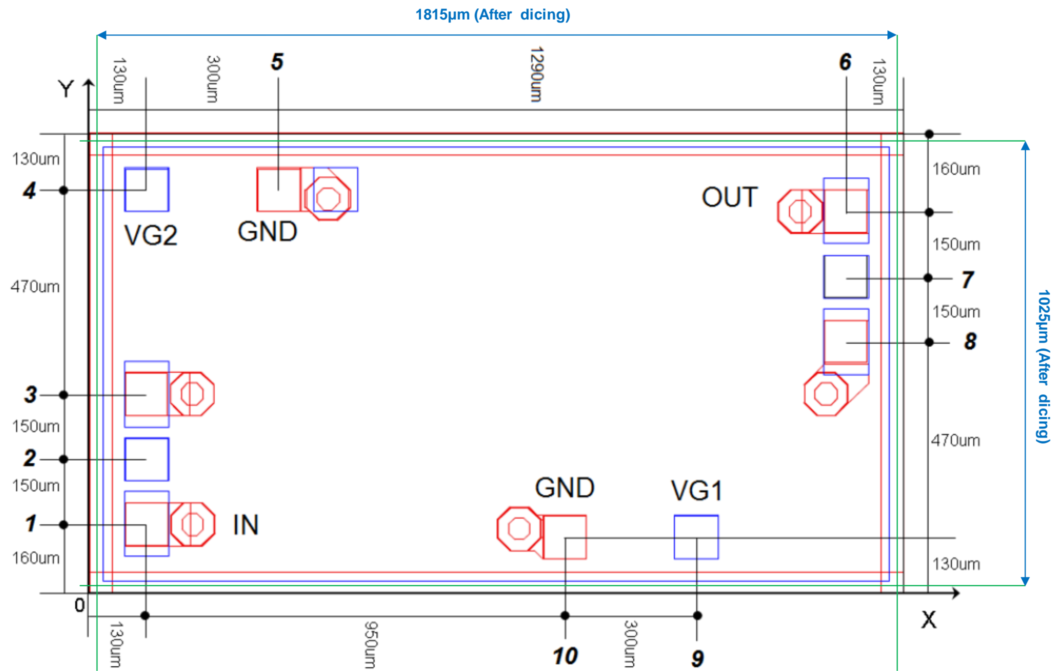


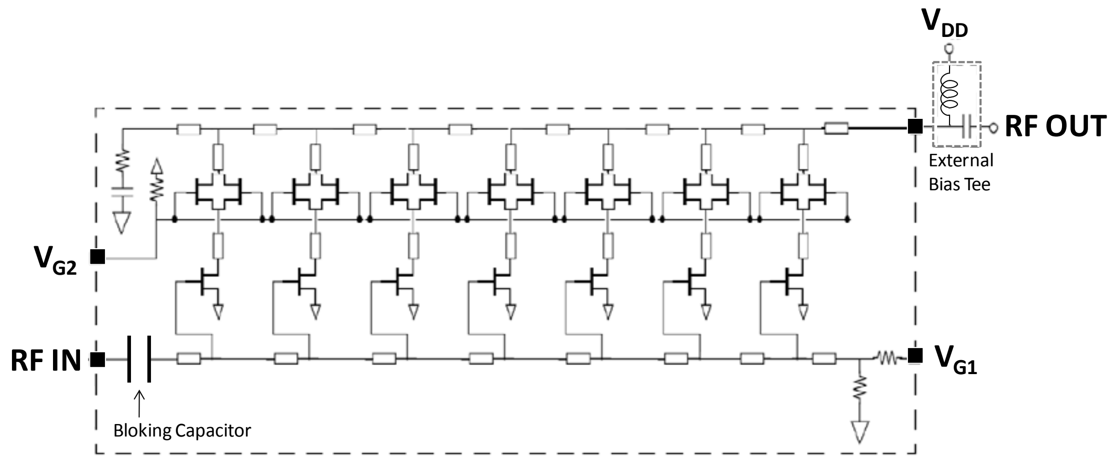
FIGURE 2 – PHYSICAL DIMENSIONS



NOTES
All dimensions are in micrometers
Chip size = 1850 x 1060µm² before dicing (1815 x 1025µm² after dicing)
Chip thickness = 100µm
RF pads (2, 7) =100 x 100µm²
DC pads = 100 x 100µm²
Chip width and length are given with a tolerance of ± 5 µm

Pad number	Pad name	Description
1,3,5,6,8,10	GND	Connected to ground with on-chip via hole
2	IN	RF input
4	VG2	Gate supply voltage 2, must be decoupled to ground using external capacitor(s) capacitor(s)
7	OUT	RF output , used to connect V_{DD} via bias Tee
9	VG1	Gate supply voltage 1, must be decoupled to ground using external capacitor(s) capacitor(s)

FIGURE 3 - FUNCTIONAL DIAGRAM



4 REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the naked MMIC die specified herein shall be as stated in this specification and ESCC Generic Specification No. 9010 for Monolithic Microwave Integrated Circuits (MMIC).

The test requirement for the MMIC lot validation shall be performed on mounted MMIC samples submitted to Burn-in and electrical measurements CHART III(b) and Lot Acceptance tests level 2 CHART V.

Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the MMIC chip reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Production Control – Wafer Lot Acceptance

(a) Total Dose Radiation Testing: not required.

4.2.2 Deviations from Production Control – Wafer screening (CHART II(a))

(a) Para.9.5.2.1: applicable on 5 bare dies assembled on appropriate substrate.

4.2.3 Deviations from Production Control – Wafer acceptance testing (CHART III(a))

(a) Para.9.7.1 and 9.7.2 only applicable.

4.2.4 Deviations from Final Production Tests (Chart II(b))

(a) Chart II(b) shall not be performed.

4.2.5 Deviations from Burn-in and Electrical Measurements (Chart III(b))

(a) Para.9.15: shall not be performed.
(b) Para.9.16: shall apply as per condition MIL-STD-883, Test Method 1015, condition ‘B’. Duration shall be 240 hours T_a = 125°C or equivalent T_a as per table 1 of MIL-STD-883, Test method 1015. Junction temperature for Burn-in shall not exceed T_j = 175°C.
(c) Para.9.5.2.2: shall not be performed.

4.2.6 Deviations from Qualification Tests (Chart IV)

Chart IV shall not be performed.

4.2.7 Deviations from Lot Acceptance Tests (Chart V)

Chart V Level 2 -Endurance Subgroup plus electrical Subgroup shall apply.
Environmental / Mechanical Subgroups shall not be performed.
Deviations from the applicable Chart V level 2 to this specification are listed herein.

(a) Level 3: Electrical measurements at room and high and low temperatures (-20°C / +85°C) on 3 samples per qualification lot shall be performed. Components Assembly and Capability Tests shall not be performed.
(b) Level 3 Special testing para. 9.27, shall not be performed.

(c) Level 2 Endurance Subgroup shall be performed on 10 samples. The operating life test duration shall be 1,000 hours minimum at T_a = 125°C or equivalent T_a as per table 1 of MIL-STD-883, Test method 1005. Junction temperature for operating life test shall not exceed T_j = 175°C.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the components specified herein is negligible.

4.3.3 Terminal Strength

(a) Shall not be performed.

4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESCC Generic Specification No. 9010. The test conditions shall be as described in MIL-STD-883, Test method 2011, cond. D.

(a) Condition: 'D'.
(b) Bond Strengths: 20 wires (5 dies, 4 wires per die, No defect allowed).

4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESCC Generic Specification No.9010. The test conditions shall be as described in MIL-STD-883, Test method 2019.

(a) Minimum acceptable on die shear strengths: 2.5kg (on 5 parts, No defect allowed).

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified here into meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

Bond Pad Metallization and Back-side metallization is Au.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence shall be as follows:
(a) The ESCC Component Number.
(b) Manufacturer name or Symbol.

(c) Manufacturer Part Number.
(d) Traceability as defined in ESCC: Lot, Wafer, Date code …
The primary package shall bear an "ESD Sensitive" label.

4.5.2 ESCC Component Number
Each component shall bear the ESCC Component Number which shall be constituted and marked as follows:

Detail specification Number: 9012/006
Type Variant (see Table 1(a)) 01
Testing Level (B or C, as applicable) B

4.5.3 Pad Identification
Pad identification shall be as shown in Figure 2 of this specification.

4.5.4 Traceability Information
Each component shall be marked in respect of traceability information in accordance with the requirements of ESCC Basic Specification No. 21700.

4.5.5 Packaging
The components shall be packaged in ESD safe Waffle / Gel packs to ensure that they are isolated from electrical, mechanical and environmental damage. The packages for the MMICs shall be purged with nitrogen or evacuated, so that the MMICs are not exposed to external environment. The individual packages and the intermediate packages shall be fixed within shipping package, which shall be resistant to mechanical shocks, humidity and dust.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature
The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_a = +25 ± 3°C.

4.6.2 Electrical Measurements at High and Low Temperatures
The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at +85°C and -20°C.

4.6.3 Circuits for Electrical Measurements
Circuits for use in performing electrical measurements listed in Table 2 and Table 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

Burn-in shall be done in accordance with Chart III(b) of ESCC Generic Specification No. 9010.

4.7.1 Parameter Drift Values
The parameter and drift values applicable to Burn-In are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_a = +25 ±3°C. The parameter drift values applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-In

The requirements for Burn-In are specified in Section 9 of ESCC Generic Specification No. 9010. The conditions for Burn-In shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuit for Burn-In

The circuit for use in performing the Burn-In test is shown in Figure 5 of this specification.

4.8 ENDURANCE TESTS (CHART V OF ESCC GENERIC SPECIFICATION NO.9010)

4.8.1 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 2 of this specification. Unless otherwise stated, the measurements shall be performed at T_a = +25 ±3 °C.

4.8.2 Conditions for Operating Life Test (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESCC Generic Specification No. 9010. The conditions for operating life testing are specified in Table 5 of this specification.

4.8.3 Electrical Circuit for Operating Life Test

The circuit for use in performing the operating life test shall be the same as shown in Figure 5 of this specification for burn-in.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.

TABLE 2 – ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE OF NAKED DIE – DC & RF PARAMETERS

T_a = 25°C, V_{DD} = 5V, V_{g2} = 2.3V, I_{DD} = 85 mA, V_{g1} = -0.3 V, R_L = 50Ω; The specifications mentioned below are measured on-wafer, using 50Ω RF probes. Unless otherwise specified.

No.	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
				MIN.	TYP.	MAX.	
1	Reference Gain (1)	G_p	3 GHz		12.6		GHz
2	High frequency cut-off	F_c	Gain @3GHz - 3dB	44	46		GHz
3	Gain ripple (2)		0.1GHz to 35GHz	-1		+1.5	dB
			35GHz to Fc	-3			dB
4	Input return loss	RLin	With 0.1nH bonding		-15		dB
5	Output return loss	RLout	With 0.1nH bonding		-15		dB
6	Noise Figure	NF	5 to 35 GHz		4.5		dB
7	Output Power @1dB compression	P1db	1 - 30GHz		18		dBm

NOTES

1. Measurement is guaranteed by correlation down to the lower frequency cut-off. 3 GHz is specified as a reference for convenience of measurement.
2. Low frequency gain ripple assumes the use of drain decoupling close to the chip.

TABLE 3 – ELECTRICAL MEASUREMENTS AT LOW AND HIGH TEMPERATURE OF DUT IN JIG - DC & RF PARAMETERS

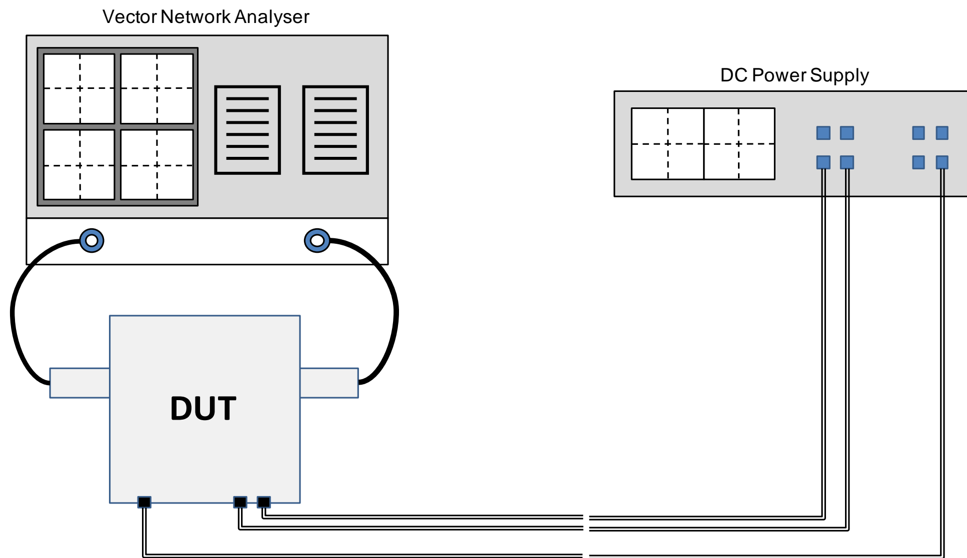
V_{DD} = 5V and I_{DD} = 85mA.

No.	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	TYP		UNIT
				-20°	+85°	
1	Reference Gain (1)	Gain	@3 GHz	14	12	dB
2	High frequency cut-off	Fc	Gain @3GHz - 3dB	45	45	GHz
3	Noise figure	NF	@12 GHz	4	5	dB
4	Input return loss	RLin	@12 GHz	-15	-15	dB
5	Output return loss	RLout	@12 GHz	-15	-15	dB

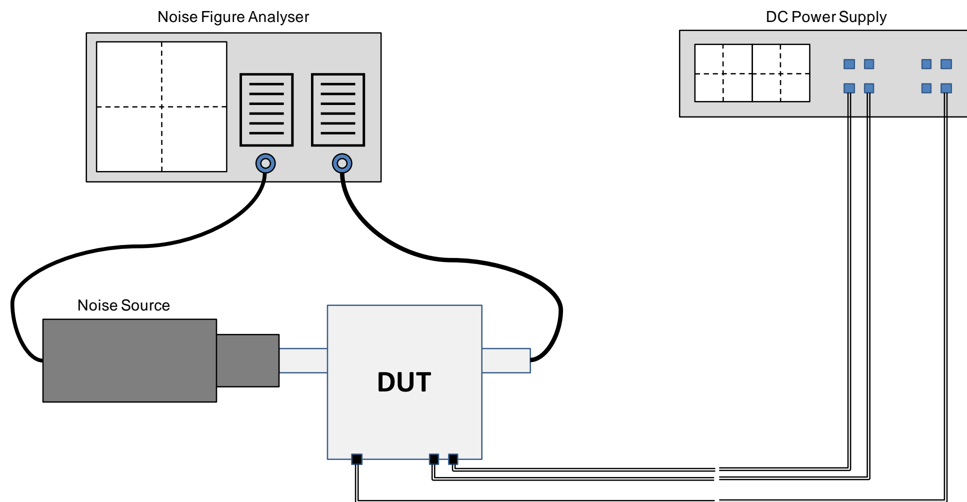
NOTES:

1. Measurement is guaranteed by correlation down to the lower frequency cut-off. 3GHz is specified as a reference for convenience of measurement.

FIGURE 4 – TEST CONFIGURATIONS FOR ELECTRICAL MEASUREMENTS [DUT IN JIG]



S parameter test set-up



Noise figure test set-up

TABLE 4 – PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS	UNIT
1	Linear Gain	G_p	As per Table 2	As per Table 2	+/-1	dB
2	Drain current (V_{DD} = 5V) for given V_{G1} & V_{G2}	I_{DD}	As per Table 2	As per Table 2	+/-20	%

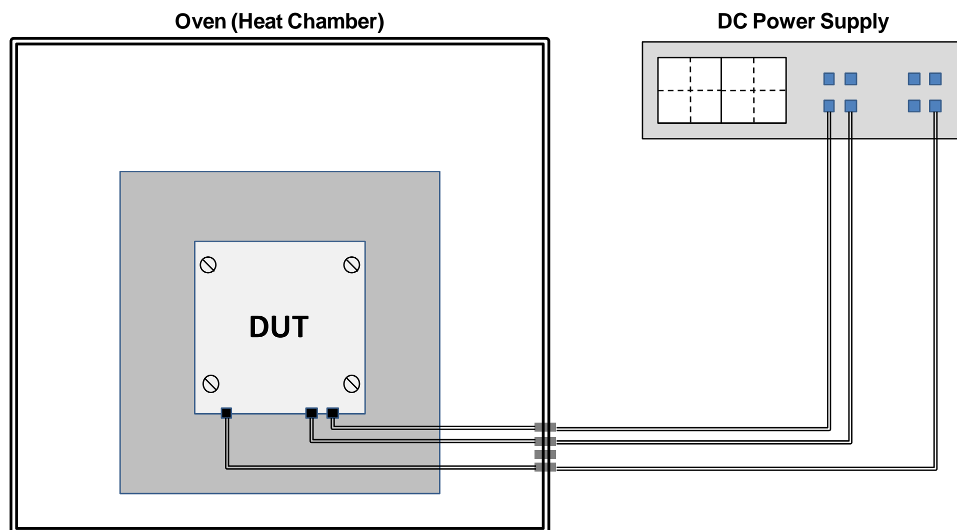
TABLE 5 – CONDITIONS FOR BURN-IN AND OPERATING LIFE-TESTS

No.	CHARACTERISTICS	SYMBOL	VALUE	UNIT
1	Ambient Temperature	T_a	+125°C	°C
2	Junction Temperature	T_j	≤ +175°C	°C
3	Drain Current	I_{DD}	85	mA
4	Drain Voltage	V_{DD}	5	V
5	Duration for Burn-In		240	hours
6	Duration for Life-Test		1000	hours

NOTES

1. Junction temperature shall not exceed T_j = +175°C.

FIGURE 5 – ELECTRICAL CIRCUIT FOR BURN-IN AND LIFE-TEST



APPENDIX A

AGREED DEVIATIONS FOR OMMIC TECHNOLOGIES

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Visual Inspection Mil-Std-883 and ESCC 2045010	OM-CI-PR-CT-CO/005/IG Visual inspection Specification for GaAs MMIC (Internal OMMIC specification for Visual inspection; based on Mil-Std-883 and ESCC 2045010)