MONOLITHIC MICROWAVE INTEGRATED CIRCUIT (MMIC) GaAs PHEMT ED02AH

PROCESS FROM OMMIC,

BASED ON TYPE CGY2173UH BARE DIE (6-BIT 6GHZ-18GHZ PHASE SHIFTER)

ESCC Detail Specification No. 9012/007

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for the Microwave Monolithic Integrated Circuit (MMIC), in die form, 6 Bit Phase Shifter, based on type CGY2173UH. The CGY2173UH, based on the GaAs PHEMT ED02AH process from OMMIC, covers the frequency range from 6 to 18GHz. This document is based on, and should be read in conjunction with ESCC Generic Specification No. 9010, the requirements of which are supplemented herein.

1.2 TYPE VARIANTS

MMIC Variants of the basic type components specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the component specified herein, are scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information is given in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the die and mechanical drawing specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing pad identification of the component specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and handling.

These chips are categorized as Class 0 with a Minimum Critical Path Failure Voltage of 50V for this Variant.

2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9010 for Monolithic Microwave Integrated Circuits (MMICs)
(b) MIL-STD-883 Test Methods and Procedures for Microelectronics
(c) ESCC No. 20600 Preservation, Packaging and Despatch of ESCC Components
(d) ESCC No. 21300 Terms Definition, Abbreviations, Symbols and Units
(e) ESCC No. 23800 Electrostatic Discharge Sensitivity Test method

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

TABLE 1(a) - TYPE VARIANTS

(1) VARIANT	(2) TYPE	(3) CASE	(4) FIGURE	(5) PAD METALLISATION AND THICKNESS OF TOP LAYER	(6) BACK SIDE FINISH (METALLISATION AND THICKNESS)
01	CGY2173UH	CHIP	2	Au, 1µm	Au, 3.5µm

TABLE 1(b) - MAXIMUM RATINGS (1)

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	RF input power	P_{IN}	+21	dBm	CW mode
2	Phase shift control inputs	P_N	$-4 < P_N < +0.5$	V	
3	Junction Temperature	T_j	+175	°C	
4	Operating Temperature Range	T_a	-40 to +85	°C	
5	Storage Temperature Range	T_{stg}	-55 to +150	°C	
6	Soldering Temperature (2)	T_{sol}	< +300 during 1 min	°C	

NOTES

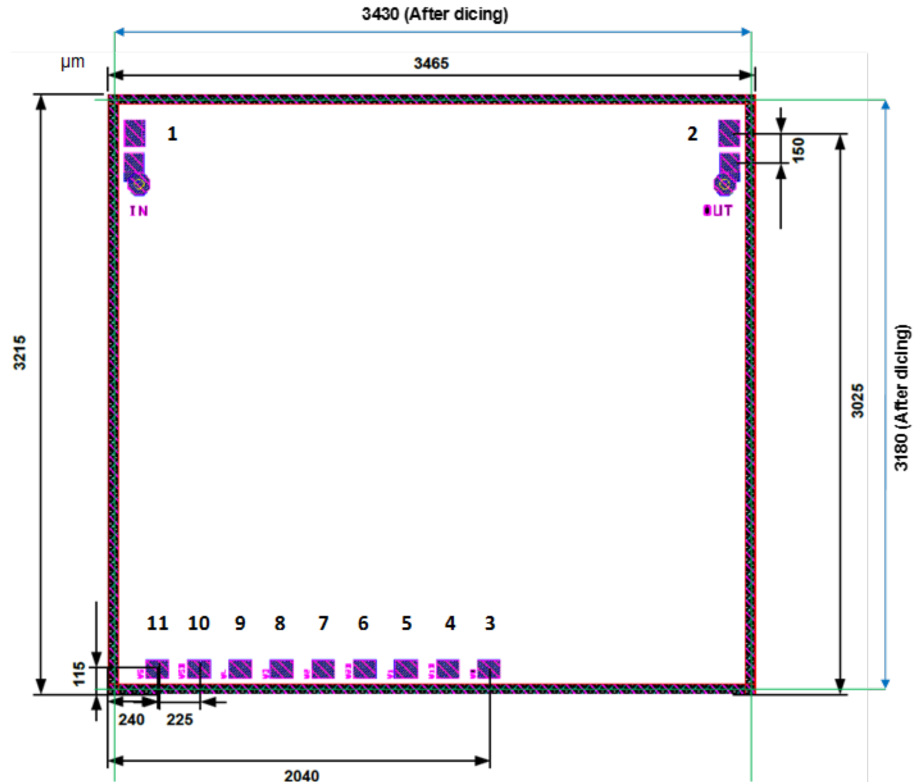
1. Operation of this device above any one of these parameters may cause permanent damage.
2. During bonding or soldering, temperatures higher than 300ºC should not be applied longer than 1 min.

FIGURE 1 - PARAMETER DERATING INFORMATION

The CGY2173 is a passive circuit without DC current.

The derating rules of the ECSS-Q-ST-30-11C have to be applied for input power and phase shift control inputs. The maximum derated channel temperature is 125°C.

FIGURE 2 - PHYSICAL DIMENSIONS



NOTES

All dimensions are in micrometres

Chip size = 3215 x 3465 µm² before dicing (3180 x 3430 µm² after dicing)

Chip thickness = 100µm

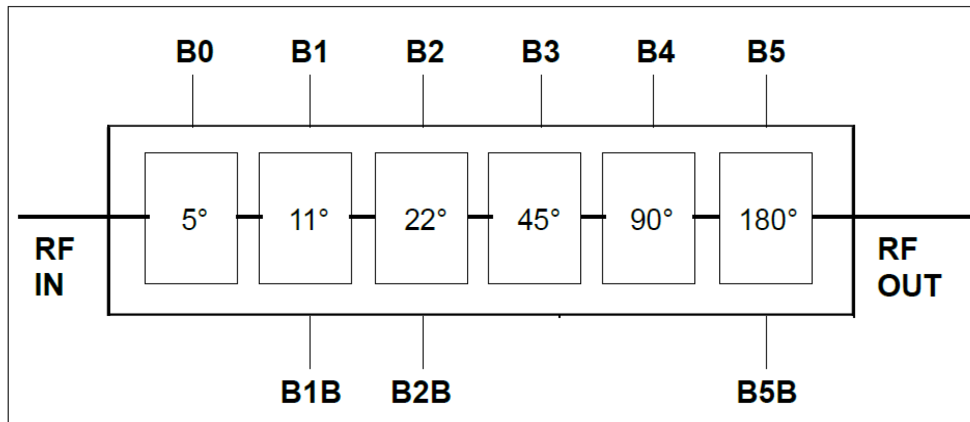
RF pads (1, 2) = 110 x 150 µm²

DC pads = 100 x 125 µm², spacing = 100µm

Chip width and length are given with a tolerance of ± 5µm

Pad number	Pad name	Description
1	IN	RF Input Port
2	OUT	RF Output Port
3	V5	180° cell control
4	V5B	180° complementary cell control
5	V4	90° complementary cell control
6	V3	45° cell control
7	V2	22° cell control
8	V2B	22° complementary cell control
9	V1	11° cell control
10	V1B	11° complementary cell control
11	V0	5° cell control

FIGURE 3 - FUNCTIONAL DIAGRAM



4 REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the naked MMIC die specified herein shall be as stated in this specification and ESCC Generic Specification No.9010 for Monolithic Microwave Integrated Circuits (MMIC).

The test requirement for the MMIC lot validation shall be performed on mounted MMIC samples submitted to Burn-in and electrical measurements Chart III(b) and Lot Acceptance tests level 2 Chart V.

Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the MMIC chip reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Production Control - Wafer Lot Acceptance

(a) Total Dose Radiation Testing: not required

4.2.2 Deviations from Production Control - Wafer screening (Chart II(a))

(a) Para. 9.5.2.1: applicable on 5 bare dies assembled on appropriate substrate

4.2.3 Deviations from Production Control - Wafer acceptance testing (Chart III(a))

(a) Para. 9.7.1 and 9.7.2 only applicable

4.2.4 Deviations from Final Production Tests (Chart II(b))

(a) Chart II(b) shall not be performed.

4.2.5 Deviations from Burn-in and Electrical Measurements (Chart III(b))

(a) Para. 9.15: shall not be performed
(b) Para. 9.16: shall apply as per condition MIL-STD-883, Test Method 1015, Cond. "B"
(c) Duration shall be 240 hours at T_a = 125°C or equivalent as per table1 of MIL-STD-883, Test Method 1015.
(d) Para. 9.5.2.2: shall not be performed.

4.2.6 Deviations from Qualification Tests (Chart IV)

Chart IV shall not be performed.

4.2.7 Deviations from Lot Acceptance Tests (Chart V)

Chart V Level 2 - Endurance Subgroup plus electrical Subgroup shall apply.

Environmental / Mechanical Subgroups shall not be performed.

Deviations from the applicable Chart V level 2 to this specification are listed herein.

(a) Level 3: Electrical measurements at room and high and low temperatures (-40°C / +85°C) on 3 samples per qualification lot shall be performed. Components Assembly and Capability Tests shall not be performed.
(b) Level 3 Special testing Para. 9.27, shall not be performed.
(c) Level 2 Endurance Subgroup shall be performed on 10 samples. The operating life test duration shall be 1,000 hours minimum at T_a = 125°C or equivalent as per table 1 of MIL-STD-883, Test Method 1005.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the components specified herein is negligible

4.3.3 Terminal Strength

(a) Shall not be performed

4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESCC Generic Specification No. 9010. The test conditions shall be as described in MIL-STD-883, Test Method 2011, Cond. "D".

(a) Condition: "D".
(b) Bond Strengths: 20 wires (5 dies, minimum 4 wires per die, No defect allowed)

4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESCC Generic Specification No. 9010. The test conditions shall be as described in MIL-STD-883, Test Method 2019.

(a) Minimum acceptable on die shear strengths: 2.5 kg (on 5 parts, No defect allowed).

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

Bond Pad Metallization and Back-side metallization is Au.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence shall be as follows:

(a) The ESCC Component Number.
(b) Manufacturer name or Symbol.
(c) Manufacturer Part Number.
(d) Traceability as defined in ESCC: Lot, Wafer, Date code…

The primary package shall bear an "ESD Sensitive" label.

4.5.2 ESCC Component Number

Each component shall bear the ESCC Component Number which shall be constituted and marked as follows:

Detail specification Number: 9012007

Type Variant (see Table 1(a)) 01

Testing Level (B or C, as applicable) B

4.5.3 Pad Identification

Pad identification shall be as shown in Figure 2 of this specification.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESCC Basic Specification No. 21700.

4.5.5 Packaging

The components shall be packaged in ESD safe Waffle / Gel packs to ensure that they are isolated from electrical, mechanical and environmental damage. The packages for the MMICs shall be purged with nitrogen or evacuated, so that the MMICs are not exposed to external environment. The individual packages and the intermediate packages shall be fixed within shipping package, which shall be resistant to mechanical shocks, humidity and dust.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_a = +25 ±3°C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at +85°C and -40°C.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Table 2 and Table 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

Burn-in shall be done in accordance with Chart III(b) of ESCC Generic Specification No. 9010.

4.7.1 Parameter Drift Values

The parameter and drift values applicable to Burn-In are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_a = +25 ±3°C. The parameter drift values applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Burn-In

The requirements for Burn-In are specified in Section 9 of ESCC Generic Specification No. 9010. The conditions for Burn-In shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuit for Burn-In

The circuit for use in performing the Burn-In test is shown in Figure 5 of this specification.

4.8 ENDURANCE TESTS (CHART V OF ESCC GENERIC SPECIFICATION NO. 9010)

4.8.1 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are scheduled in Table 2 of this specification. Unless otherwise stated, the measurements shall be performed at T_a = +25 ±3°C.

4.8.2 Conditions for Operating Life Test (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESCC Generic Specification No. 9010. The conditions for operating life testing are specified in Table 5 of this specification.

4.8.3 Electrical Circuit for Operating Life Test

The circuit for use in performing the operating life test shall be the same as shown in Figure 5 of this specification for burn-in.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.

TABLE 2 – ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE OF NAKED DIE – DC & RF PARAMETERS

T_a = 25°C, RF performance measured on wafer. RF performance at 12 GHz unless specified.

No.	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
				MIN.	TYP.	MAX.	
1	Bandwidth	BW		6		18	GHz
2	Phase shift control inputs	P_N		-3		0	V
3	Insertion loss	IL	Reference state		13		dB
4	Phase range	PH_{range}			360		deg
5	Input reflection coefficient	S_{11}	Reference state		-20	-12	dB
6	Output reflection coefficient	S_{22}	Reference state		-20	-12	dB
7	RMS Phase error vs phase setting (1)	$PH_{error\ (RMS)}$	6 main states		4		deg
8	Maximum Phase error vs phase setting (1)	$PH_{error\ (MAX)}$	6 main states		10		deg
9	RMS Attenuation variation with phase setting (1)	$ATT_{variation\ (RMS)}$	6 main states		0.6		dB
10	Maximum Attenuation variation with phase setting (1)	$ATT_{variation\ (MAX)}$	6 main states		1		dB

NOTES

1. The RMS value is the root mean square of the error defined as below:

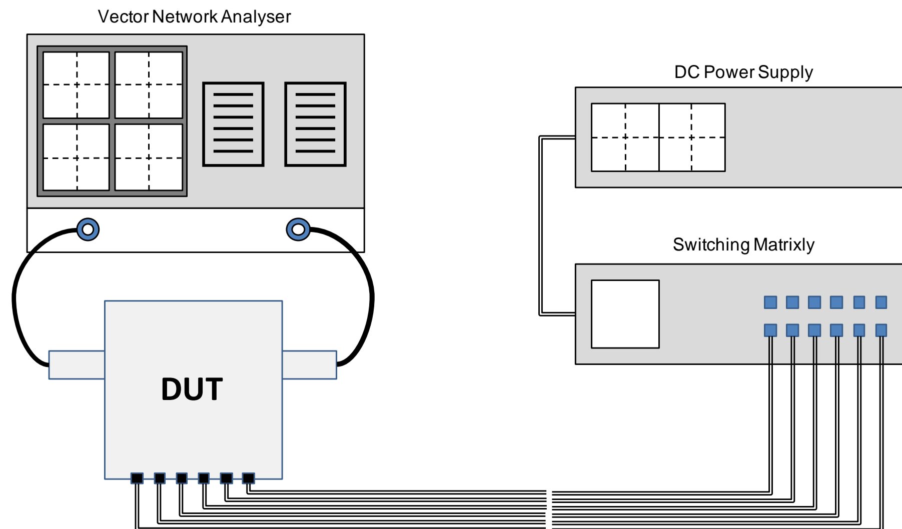
$$x_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\bar{x}_i^2 + \sigma_{xi}^2}$$

Where x_i is the difference between the measured value and the theoretical value (x_i is the error), x_i is the mean value of the N x_i, and σ_{xi} is the standard deviation of x_i.

TABLE 3 - ELECTRICAL MEASUREMENTS AT LOW AND HIGH TEMPERATURE OF DUT IN JIG - DC & RF PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	TYP		UNIT
				-40°C	+85°C	
1	Bandwidth	BW		6-18	6-18	GHz
2	Insertion loss	IL	Reference state	11	15	dB
3	Phase range	PH_{range}		360	360	deg
4	Input reflection coefficient	S_{11}	Reference state	-20	-20	dB
5	Output reflection coefficient	S_{22}	Reference state	-20	-20	dB
6	RMS Phase error vs phase setting	$PH_{error (RMS)}$	6 main states	4	4	deg
7	Maximum Phase error vs phase setting	$PH_{error (MAX)}$	6 main states	10	10	deg
8	RMS Attenuation variation with phase setting	$ATT_{variation (RMS)}$	6 main states	1	1	dB
9	Maximum Attenuation variation with phase setting	$ATT_{variation (MAX)}$	6 main states	1.2	1.2	dB

FIGURE 4 - TEST CONFIGURATIONS FOR ELECTRICAL MEASUREMENTS [DUT IN JIG]



S parameter test set-up

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC.AND/OR TESTMETHOD	TEST CONDITIONS	LIMITS	UNIT
1	Insertion Losses	IL	As per Table 2	As per Table 2	+/-1	dB
2	Phase Shift RMS	RMS PHi	As per Table 2	As per Table 2	+/-2	deg

TABLE 5 - CONDITIONS FOR BURN-IN AND OPERATING LIFE-TESTS

No.	CHARACTERISTICS	SYMBOL	VALUE	UNIT
1	Ambient Temperature	T_a	+125°C (see 4.2.5 and 4.2.7)	°C
2	Duration for Burn In		240 • 120 hours with maximum phase shift • 120 hours with minimum phase shift	Hours
3	Duration for Life-Test (1)		1000 • 500 hours with maximum phase shift • 500 hours with minimum phase shift	Hours

NOTES

1. Intermediate measurements shall be performed after 500 and 1000 hours of operating Life-test.

FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN AND LIFE-TEST

The setup is the same as presented in Figure 4. VNA is required only for Electrical Measurements and is not mandatory during burn in test. Switching matrix may be replaced by power supply (all bits are set to the same value).

As required, loads could be placed at RF input and RF output ports of DUTs under Burn-in and operating Life-tests.

APPENDIX A

AGREED DEVIATIONS FOR OMMIC TECHNOLOGIES

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Visual Inspection Mil-Std-883 and ESCC 2045010	OM-CI-PR-CT-CO/005/IG Visual inspection Specification for GaAs MMIC (Internal OMMIC specification for Visual inspection; based on Mil-Std-883 and ESCC 2045010)