EVALUATION TEST PROGRAMME FOR

INTEGRATED CIRCUITS:

MONOLITHIC AND MULTICHIP MICROCIRCUITS, WIRE-BONDED, HERMETICALLY SEALED

AND

FLIP-CHIP MONOLITHIC MICROCIRCUITS, SOLDER BALL BONDED, HERMETICALLY AND NON-HERMETICALLY SEALED

ESCC Basic Specification No. 2269000

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1 PURPOSE

The purpose of this specification is to establish the procedure to be followed in the evaluation of component capabilities as required for space applications and thereby to anticipate, as far as possible, component behaviour during qualification testing. Therefore, the aim of such testing shall be to overstress specific characteristics of the component concerned with a view to the detection of possible failure modes. Additionally, a detailed destructive physical analysis shall be performed to detect any design and construction defects which may affect the reliability of the component and to facilitate failure analysis activities. The evaluation shall also include a check of the susceptibility of the component to ESD damage.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect at the date of commencement of the evaluation.

2.1 ESCC SPECIFICATIONS

- No. 9000, Integrated Circuits, Monolithic.
- No. 20400, Internal Visual Inspection.
- No. 20500, External Visual Inspection.
- No. 20900, Radiographic Inspection.
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 22600, Requirements for the Evaluation of Standard Electronic Components for Space Application.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23800, Electrostatic Discharge Sensitivity Test Method.

NOTE:
Unless otherwise stated herein, reference within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

- IEC Publication No. 68, Basic Environmental Testing Procedures.
- IEC Publication No. 747, Semiconductor Devices: Discrete Devices and Integrated Circuits.
- MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.
- MIL-STD-883, Test Methods and Procedures for Microelectronics.
- ECSS-Q-ST-70-02, Thermal Vacuum Test for the Screening of Space Materials.
- J-STD-020, IPC/Jedec Standard For Moisture/Reflow Sensitivity Classification For Non-Hermetic Surface-Mount Devices.
- JESD22-A110, EIA/Jedec Standard Test Method: Steady-State Temperature Humidity Bias Life Test.
- JESD22-A101, EIA/Jedec Standard Test Method: Highly-Accelerated Temperature and Humidity Stress Test (HAST).
- JESD22-B117, EIA/Jedec Standard Test Method: Solder Ball Shear.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following shall apply:

- Wire-bonded Integrated Circuit: A monolithic or multichip microcircuit with the die (dice) backside(s) bonded to the package cavity or substrate, and wire-bonded to the package leads.
- Flip-chip Integrated Circuit: A monolithic microcircuit with solder balls attached to the active side of the die, connected top-side down to a substrate, with or without underfill.
- Hermetic Package: A component encapsulation which by design and construction is able to pass a seal test.
- Non-Hermetic Package: A component encapsulation which by design or construction is unable to pass a seal test.
- Add-on Components: Capacitors mounted in and electrically connected to a flip-chip integrated circuit assembly. Other component types are not permitted.

4 PROCEDURE

Standard components shall be selected from a homogeneous lot at the Manufacturer to be evaluated. These components shall not have been submitted to any screening or burn-in, but must have been manufactured in conformity with high reliability practice and an established Process Identification Document (PID) or an identifiable process which shall form the basis for the PID.

The tests specified in the programme shall be performed in the sequence shown in the appropriate Chart I, where:

- Chart I(A) is the Evaluation Test Programme for Wire-bonded Integrated Circuit components
- Chart I(B) is the Evaluation Test Programme for Hermetic Flip-chip Integrated Circuit components
- Chart I(C) is the Evaluation Test Programme for Non-Hermetic Flip-chip Integrated Circuit components

All results shall be recorded and failed components submitted to a failure analysis. Probable failure modes and mechanisms shall be determined.

The evaluation test programme shall be performed, under the supervision of the ESCC Executive, by the Manufacturer or at a test laboratory approved by the ESCC Executive.

4.1 AGREED DEVIATIONS TO CHART I TEST REQUIREMENTS

Deviations to the test requirements of Chart I may be approved subject to full justification being provided by the manufacturer to the ESCC Executive. Approved deviations shall be fully documented and all details shall be included in the Evaluation Test Programme.

4.2 MANDATORY PREREQUISITES FOR FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS

Prior to the start of an evaluation implementing the requirements of this ETP, and in order to adequately comply with the requirements of ESCC Basic Specification Nos. 20100 and 22600, the manufacturer shall have completed a development and process qualification plan specifically including assessments of, and creating specifications for, the following:

- Solder ball dimension and co-planarity.
- Electromigration at solder ball level.
- Alloy composition in compliance with ECSS-Q-ST-60.
- Ionic contamination resulting from the use of flux, and within the underfill.
- Electrical characterisation over the temperature range pre- and post- column attachment.
- Level 2 interconnect (e.g. balls, columns) attachment to package, representative of manufacturing and screening effects.
- Package mounting on PCB.

Such assessments may be performed on representative test structures but, in any case, shall be fully documented and must be repeated in the event of material, process and supply chain changes.

The manufacturer shall have systematic control over all materials used in the construction of the flip-chip integrated circuit components, particularly for underfill and thermal interface material. This shall be documented in the PID.

5 TEST PROGRAMME SEQUENCE AND SAMPLE DISTRIBUTION

5.1 SELECTION OF COMPONENTS FOR EVALUATION TESTING

The number of components to be selected for evaluation testing shall depend on whether a single component type or a family of parts is evaluated and the number of component types chosen to represent the family.

For Wire-bonded Integrated Circuit components with Hermetic Packages, not less than 103 specimens (plus additional samples as specified) shall be used for each test programme.

For Flip-chip Integrated Circuit components with Hermetic Packages, not less than 101 specimens (plus additional samples as specified) shall be used for each test programme.

For Flip-chip Integrated Circuit components with Non-Hermetic Packages, not less than 111 specimens (plus additional samples as specified), with or without columns attached, shall be used for each test programme. The total number of specimens may be a combination of components and representative test structures as agreed by the ESCC Executive.

The component types chosen to represent a family shall cover the range of components to be evaluated and be representative of the different package and pin configurations under consideration. They shall also be the most suitable for highlighting those characteristics and parameters that are pertinent to an investigation into failure modes and weaknesses.

The samples shall be as specified by, or as agreed with, the ESCC Executive.

The above mentioned quantity shall be submitted to the full evaluation procedure whenever a new technology has been applied to the components concerned, where there is insufficient experience in their production.

5.2 DETAIL SPECIFICATIONS

Should a Detail Specification for the device(s) to be evaluated not exist, the Manufacturer shall prepare such a document(s) in accordance with the established ESCC format and submit it to the ESCC Executive for provisional approval. This shall then serve as a basis for the ordering and testing of the relevant components.

5.3 INSPECTION RIGHTS

The ESCC Executive reserves the right to inspect at any time the components processed for evaluation purposes. The Manufacturer shall notify the ESCC Executive at least three working days in advance of the date of internal visual inspection (but see Para. 5.4).

5.4 CONTROL DURING FABRICATION

The components shall be produced as defined in Para. 4 of this specification. Internal visual inspections shall be performed on the lot to be tested to the extent that this forms part of the Manufacturer's standard procedures. Progress of the components shall be observed closely and recorded together with an analysis of any reject. A chart showing the numbers in/out and failure cause for each fabrication stage shall be submitted to the ESCC Executive.

6 INSPECTION

6.1 GENERAL

The components shall be checked to verify their suitability for the Evaluation Test Programme. Defects or deviations from the established ESCC requirements may invalidate the evaluation. For each measurement or inspection performed, the results shall be summarised in terms of quantity tested, quantity passed and quantity rejected. If devices are rejected, the reason shall be clearly identified.

6.2 DIMENSIONS (100%)

All devices shall be inspected (go-no-go) in accordance with Physical Dimensions and Terminal Identification in the Detail Specification. Where gauges exist for performance of measurements, these may be used. For packages with a high pin count, the measurements may be performed using a sampling scheme which shall be approved by the ESCC Executive. Rejected components shall be replaced.

6.3 WEIGHT (100%)

All devices shall be weighed (go-no-go). Any devices that exceed the weight defined in the Detail Specification shall be rejected and replaced.

6.4 ELECTRICAL MEASUREMENTS (100%)

These measurements shall be performed (go-no-go) in accordance with Room Temperature Electrical Measurements in the Detail Specification at an ambient temperature of +22 ±3°C. Rejected components shall be replaced.

6.5 EXTERNAL VISUAL INSPECTION (100%)

All devices shall be inspected in accordance with ESCC Basic Specification No. 20500. Rejected components shall be replaced.

6.6 PARTICLE IMPACT NOISE DETECTION (PIND) (100%)

All devices shall be tested in accordance with the defined in ESCC Generic Specification No. 9000. Rejected components shall be replaced.

6.7 RADIOGRAPHIC INSPECTION (100%)

Not applicable to Flip-chip Integrated Circuit components.

All devices shall be inspected in accordance with ESCC Basic Specification No. 20900. Additional axes to those specified in the relevant ancillary specification of ESCC Basic Specification No. 20900. may be radiographed if, by so doing, it is possible to observe any faults. Rejected components shall be replaced.

6.8 HERMETICITY (100%)

Applicable to hermetically sealed components only.

Fine and gross leak tests shall be performed on all components in accordance with the requirements defined in ESCC Generic Specification No. 9000. Rejected components shall be replaced.

6.9 MARKING AND SERIALISATION (100%)

All components shall be marked and serialised in accordance with the standard procedures of the Manufacturer concerned.

6.10 MATERIALS AND FINISHES

All non-metallic materials and finishes, that are not within a hermetically sealed enclosure, of the components specified herein shall be tested in accordance with ECSS-Q-ST-70-02 to verify its outgassing requirements, unless relevant data is available. See also Para. 8.3.4.2 herein for components with Non-Hermetic Packages.

6.11 COMPLETION OF INSPECTION

The completion of inspection shall result in a batch of components that have been verified as to their suitability for the Evaluation Test Programme, i.e. each component has satisfied the requirements of Paras. 6.2 to 6.10 inclusive.

7 INITIAL ELECTRICAL MEASUREMENTS (100% READ AND RECORD)

These measurements shall be made according to the Room, High and Low Temperatures Electrical Measurements Paras. in the Detail Specification. All characteristics shall be recorded against serial numbers.

8 EVALUATION TEST PROGRAMME

8.1 GENERAL

The evaluation tests shall be performed as specified in Chart I. The components shall be randomly divided into groups and their associated subgroups in the quantities indicated in Chart I. When a family of components is under investigation, the variations within that family must be represented in each group/subgroup.

The Subgroup 2A tests shall be completed and the results analysed before the Subgroup 3B tests are commenced.

All failed components shall be analysed. The depth of analysis shall depend upon the circumstances in which failure occurred and upon whether useful information may be gained. As a minimum, the failure mode shall be determined in each case. Components not failing catastrophically, i.e. those displaying out-of-tolerance electrical parameters, shall not be removed from the test sequence but monitored to observe degradation trends.

8.2 GROUP 1 - CONTROL GROUP

This group shall be retained for comparison purposes. Whenever electrical measurements are made on any devices under test, these devices shall also be measured.

8.3 GROUP 2 - DESTRUCTIVE TESTS

8.3.1 General

This group shall be randomly divided into subgroups in the quantities indicated in Chart I.

Testing of flip-chip integrated circuit components may be performed on parts without columns unless otherwise specified.

The use of representative test structures (incl. empty packages) for flip-chip integrated circuit components is subject to agreement with the ESCC Executive and to be specified in advance in the applicable test plan.

8.3.2 Subgroup 2A - Step-Stress Tests

8.3.2.1 General

This subgroup shall be randomly divided into further subgroups in the quantities indicated in Chart I. The step-stress sequence shall be terminated when 50% (rounded up) of the specimens have been destroyed, unless practical reasons prevent this.

8.3.2.2 Subgroup 2A(i) - Determination of Thermal Resistance/Conductivity

MIL-STD-883, Method 1012. A special constructed device or test structure might be necessary for the performance of this test.

8.3.2.3 Parameters to be measured during Step-Stress Tests

During step-stress tests, electrical measurements shall be made in accordance with Parameter Drift Values in the Detail Specification. If parameter drift values are not specified in the Detail Specification, then the parameters to be measured shall be selected from Room Temperature Electrical Measurements in the Detail Specification. In the case of doubt as to the applicability of any given parameter, the parameter shall be measured. Quiescent current (if applicable) shall be measured in all cases. At the termination of the step-stress sequences, any surviving devices shall have their thermal resistance/conductivity measured as specified in Para. 8.3.2.2.

8.3.2.4 Subgroup 2A(ii) - Temperature Step-Stress Test

The tests in this subgroup shall be performed as specified in Chart II. Electrical measurements shall be made as defined in Para. 8.3.2.3 above. The starting temperature (which will be no higher than the maximum operating temperature as defined in the Detail Specification) and the temperature steps (with a maximum step of 25°C) to be employed will be decided by the ESCC Executive.

8.3.2.5 Subgroup 2A(iii) - Power Step-Stress Test

(a) Applicability

This test is only applicable to devices where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(b) Procedure

The tests in this subgroup shall be performed as specified in Chart III. Electrical measurements shall be made as defined in Para. 8.3.2.3 above. The starting power (which will be no higher than the maximum input power as defined in the Detail Specification) and the power steps (with a maximum step of 20%) to be employed will be decided by the ESCC Executive.

8.3.2.6 Analysis of Subgroup 2A

The analysis of Subgroup 2A shall be presented to the ESCC Executive in a graphical form, supported by the actual results, as follows:

- The number of functional failures shall be plotted against each temperature or power level (if applicable) applied. The cumulative failure rate shall also be plotted.
- The parameters (as defined in Para. 8.3.2.3 above) shall be monitored, recorded and plotted against time for each temperature or power level (if applicable) as appropriate.
- The average drift of the parameters at each temperature or power level applied shall be plotted against temperature or power (if applicable) as appropriate.

The analysis of the results of Subgroup 2A(ii and iii (if applicable)) shall be used to determine the most effective temperatures and power (if applicable) for the accelerated electrical endurance test (Subgroup 3B).

8.3.3 Subgroup 2B - Radiation Tests

8.3.3.1 Total Dose Steady-State Radiation Test

In accordance with ESCC Basic Specification No. 22900.

8.3.4 Subgroup 2C - Construction Analysis

8.3.4.1 Internal Water Vapour Content

Applicable to components with hermetic packages only.

MIL-STD-883, Method 1018, Procedure 1.

8.3.4.2 *Outgassing*

Applicable to components with non-hermetic packages only.

ECSS-Q-ST-70-02 (performed on suitable raw material samples of all those used in the component)

8.3.4.3 *Opening*

The devices shall be opened using a technique which does not contaminate the internal structure or in any way impair the ability to observe defects.

8.3.4.4 *Internal Visual Inspection*

Each device shall be visually inspected in accordance with ESCC Basic Specification No. 20400. Photographs shall be taken as follows:

(a) An overall photograph of the opened device.
(b) An overall photograph of the die (see note)
(c) Photographs of any anomalies found.

NOTE:
May be excluded for Flip-chip Integrated Circuit components with thermal interface material between the die and the lid/heat-spreader.

8.3.4.5 *Scanning Electron Microscope (SEM) Inspection*

This inspection shall include, but shall not necessarily be limited to, examination of the following:

(a) Detailed examination of any anomalies identified by the internal visual inspection (Para. 8.3.4.4 above).
Photographs shall be taken of the above.

(b) Low magnification (up to 500x) shall be used to assess:
  (i) Clearance of bond wires at the die edge.
  (ii) Quality of bonding at the die.
  (iii) Quality of bonding at the post.
Photographs shall be taken of the above.

(c) High magnification (1000x or greater) shall be used to assess:
  (i) Metallisation coverage and consistency at steps.
  (ii) Metallisation coverage at contact windows, bonding pads, etc.
Photographs shall be taken of the above.

In the case of devices with a glassivated surface, this examination shall first be attempted through the glassivation.

If the resolution is inadequate, the glassivation shall be removed. This step must be postponed until the bond strength (Para. 8.3.4.6) test has been performed.

For devices with multi-level metallisation, the upper layer(s) shall be removed to permit assessment of the above mentioned features. This step shall also be postponed until the bond strength test (Para. 8.3.4.6) has been performed.

For deep sub-micron devices, SEM inspection of the die may be impracticable; in which case the Manufacturer shall fully justify any deviations in accordance with Para. 4.1.

8.3.4.6 *Bond Strength Test*

Not applicable to Flip-chip Integrated Circuit components.

In accordance with Bond Strength in ESCC Generic Specification No. 9000.

8.3.4.7 Die Shear or Substrate Attach Strength or Flip-Chip Pull-Off Test

(a) Precautions
If it is known, or believed, that beryllium oxide or other toxic substances are used in the construction of the device, precautionary measures shall be employed.

(b) Procedure
In accordance with Die Shear or Substrate Attach Strength or Flip-chip Pull-Off in ESCC Generic Specification No. 9000.

8.3.4.8 Microsectioning

(a) Precautions
As per Para. 8.3.4.7(a) above.

(b) Glassivation Layer Integrity (if applicable)
MIL-STD-883, Method 2021.

(c) Mounting
The device(s) shall be mounted on a carrier or in a transparent thermosetting resin. This shall have a curing temperature below the maximum storage temperature of the device(s). The resin shall be evacuated after mixing and after the device has been mounted in the uncured resin.

(d) Microsectioning
The device(s) shall be ground and polished to achieve a surface finish of at least 0.1 micron. To improve definition and detail, chemical etches shall be used to highlight junction definition, metallographic features, etc. The following, not exhaustive, features shall be assessed:

(i) Diffusion and oxide characteristics.
(ii) Metal/semiconductor interfaces.
(iii) Metal/metal interfaces.
(iv) Thickness and consistency of layers; particularly insulating layers in devices with multiple layer metallisation.
(v) Plating thickness and consistency on posts and pins.
(vi) For CGA packages, columns shall be included.

Photographs shall be taken of the above.

8.3.4.9 Solder Ball Shear

Applicable to Flip-chip Integrated Circuit components only.

50 solder balls shall be tested in accordance with JESD22-B117.

8.3.5 Subgroup 2D - Package Tests

8.3.5.1 General

This group shall be randomly divided into subgroups in the quantities indicated in Paras. 8.3.5.2, 8.3.5.3, 8.3.5.4, 8.3.5.5 and 8.3.5.6 (as applicable). Any devices from Paras. 8.3.5.2 or 8.3.5.3 that have not been destroyed shall then also be subjected to Para. 8.3.5.4.

8.3.5.2 Subgroup 2D(i) - Thermal Tests

8.3.5.2.1 Thermal Tests for Components with Hermetic Packages

(a) Applicability
These tests must be performed on electrically good devices.

(b) Procedure
(i) Temperature Cycling
All devices shall be subjected to the test defined in Chart F3 ESCC Generic Specification No. 9000 - 100 cycles instead of 10 cycles.
(ii) Seal Test
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000.
(iii) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.
(iv) Thermal Shock
Not required for Flip-chip Integrated Circuit components.
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000. 100 cycles instead of 10 cycles.
(v) Seal Test
Not required for Flip-chip Integrated Circuit components.
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000.
(vi) Electrical Measurements
Not required for Flip-chip Integrated Circuit components.
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.
(vii) Destructive Physical Analysis
Not applicable to wire-bonded integrated circuit components.
A DPA shall be carried out on one hermetic flip-chip integrated circuit component, selected from the 15 samples.

8.3.5.2.2 Thermal Tests for Flip-chip Integrated Circuit Components with Non-Hermetic Packages
(a) Applicability
These tests must be performed on electrically good devices.

(b) Procedure
(i) Scanning Acoustic Microscopy (SAM) – Initial Inspection
MIL-STD-883, Method 2030.
(ii) Preconditioning
J-STD-020. Preconditioning per applicable Moisture Sensitivity Level as specified by the Manufacturer. Conditions shall be agreed with the ESCC Executive prior to evaluation testing.
(iii) Scanning Acoustic Microscopy (SAM) – Intermediate Inspection
MIL-STD-883, Method 2030.
(iv) Temperature Cycling
All devices shall be subjected to the test defined in Chart F4 of ESCC Generic Specification No. 9000. 1500 cycles instead of 100 cycles.
(v) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.
(vi) Scanning Acoustic Microscopy (SAM) – Final Inspection
MIL-STD-883, Method 2030.
(vii) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.
(viii) Destructive Physical Analysis
A DPA shall be carried out on two hermetic flip-chip integrated circuits, selected from the 15 samples.

8.3.5.3 Subgroup 2D(ii) - Mechanical and Thermal Vacuum Tests

8.3.5.3.1 Subgroup 2D(ii-a):

(a) Applicability
These tests must be performed on electrically good devices.

(b) Procedure

(i) Preconditioning
Applicable to Flip-chip Integrated Circuit components with Non-Hermetic Packages only. Preconditioning shall be performed in accordance with J-STD-020, per the applicable Moisture Sensitivity Level specified by the Manufacturer. Conditions shall be agreed with the ESCC Executive prior to evaluation testing.

(ii) Mechanical Shock
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000. 50 pulses (per orientation) instead of 5 pulses (per orientation).

(iii) Seal Test
Not applicable to components with Non-Hermetic Packages.
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(iv) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(v) Vibration
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000. 120 sweeps (total) instead of 12 sweeps (total).

(vi) Seal Test
Not applicable to components with Non-Hermetic Packages.
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(vii) Electrical Measurements
These measurements shall be made in accordance with Room Temperature Electrical Measurements in the Detail Specification.

8.3.5.3.2 Subgroup 2D(ii-b) – Thermal Vacuum Test

(a) Applicability
3 of the samples specified in this subgroup shall be subjected to these tests.

These tests must be performed on electrically good devices.

(b) Procedure

(i) Scanning Acoustic Microscopy (SAM) – Initial Inspection
MIL-STD-883, Method 2030.

(ii) Thermal Vacuum
All devices shall be subjected to thermal vacuum with the following conditions:

- 20 cycles
- T_{amb} = -30°C to + 70°C
- pressure: ≤ 1mPa
- dwell time : 2 hours
- slope 2°C/min

(iii) Scanning Acoustic Microscopy (SAM) – Final Inspection
MIL-STD-883, Method 2030.

8.3.5.3.3 Subgroup 2D(ii-c):

(a) Applicability
All components subjected to Mechanical Subgroup 2D(ii-a) tests, including any failures, may be subjected to these tests.

(b) Procedure:

(i) Solderability
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000. For flip-chip integrated circuit components Solderability shall be performed on parts with columns attached.

(ii) Permanence of Marking
All devices shall be subjected to the test defined in ESCC Generic Specification No. 9000.

(iii) Lid Torque
Applicable to packages which use a glass-frit-seal to lead frame, lead or package body only (i.e. wherever frit seal establishes hermeticity or package integrity).
MIL-STD-883, Method 2024.

(iv) Lid Pull
Applicable to non-hermetic flip-chip integrated circuit components only.
MIL-STD-883, Method 2027.

(v) Solder Column Pull Strength (as applicable)
MIL-STD-883, Method 2038.

8.3.5.4 Subgroup 2D(iii) - Resistance to Soldering Heat

(a) Applicability
2 of the samples specified in this subgroup in Chart I plus any devices from Paras. 8.3.5.2 or 8.3.5.3 that have not been destroyed shall be subjected to these tests. These tests must be performed on electrically good devices. Devices previously subjected to Subgroup 2D(i) may be replaced.

(b) Procedure
IEC Publication No. 68-2-20 Test 'Tb', Method '1A' with no thermal screen or flux for 10 ±1s, or MIL-STD-750, Method 2031. Following each cycle, electrical measurements shall be performed (go-no-go) in accordance with Room Temperature Electrical Measurements in the Detail Specification and a seal test shall be performed in accordance with Para. 8.3.5.2(iii) above. The test shall be repeated until the device has failed or 5 cycles have been performed whichever is the sooner.

8.3.5.5 Subgroup 2D(iv) - Pin To Pin Isolation

(a) Applicability
This test must be performed on empty package(s) that have been through the normal assembly procedures up to sealing.

(b) Procedure
MIL-STD-883, Method 1003.

8.3.5.6 Subgroup 2D(v) – Humidity Test

(a) Applicability
These tests must be performed on electrically good devices.

(b) Procedure
Either JESD22-A101, Steady-State Temperature Humidity Bias Life Test or JESD22-A110, Highly-Accelerated Temperature and Humidity Stress Test (HAST). The standard to be followed, and the applicable test conditions, are subject to the approval of the ESCC Executive.

8.3.6 Subgroup 2E - Electrical Tests

8.3.6.1 General

The components in this subgroup shall be randomly divided between those tests that are performed.

8.3.6.2 Electrostatic Discharge Sensitivity (ESDS) Test

ESD testing shall be performed in accordance with ESCC Basic Specification No. 23800. If the component under examination is not categorised into one of the 3 classes listed, then the component shall be termed "unclassified".

When the evaluation covers a family or series of components, the types selected for this test shall be representative of all protection circuits within this family or series.

8.3.6.3 Characterisation

(a) Safe Operating Area

(i) Applicability

This test is only applicable to devices where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. Additionally, it shall only be applied to integrated circuit components that do not have internal output protection circuitry. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(ii) Procedure

IEC Publication No. 747-7, Para. 11.3.4. The ESCC Executive shall review the component type and technology to determine the test conditions.

(b) Current Limits

The design of each device under investigation shall be examined to ensure that no part of the device carries more than the maximum current defined by the technology or process design rules.

(c) Breakdown Voltage, Input or Output

(i) Applicability

Applicable to digital devices only.

(ii) Procedure

MIL-STD-883, Method 3008 shall be applied to find the limiting value.

(d) Input Interaction

(i) Applicability

Applicable to digital devices only.

(ii) Digital Devices Procedure

The truth table shall be applied at the maximum operating frequency under the conditions specified in the truth table.

(e) Verification of Functionality

The functionality of the device shall be explored over varying temperature ranges, levels of supply voltage, etc. The ESCC Executive shall review the component type and technology to determine the exact procedure to be adopted. Data shall be presented, preferably, in a graphical form: Schmoo plots for example.

8.3.7 Subgroup 2F - Wafer Tests

8.3.7.1 Solder Ball Shear

JESD22-B117 on a minimum of 50 solder balls (a special test structure might be necessary for the performance of this test).

8.4 GROUP 3 - ENDURANCE TESTS

8.4.1 General

This group shall be randomly divided into subgroups in the quantities indicated in Chart I (as applicable).

8.4.2 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test

Unless otherwise specified in the Detail Specification, all devices shall be subjected to the test defined in ESCC Generic Specification No. 9000.

8.4.3 Subgroup 3B - Accelerated Electrical Endurance Test

This group shall be randomly divided into 3 subgroups in the quantities indicated in Chart I. The applicable tests shall not be performed until the subgroup 2A tests have been completed and analysed, and 3 test conditions selected. The tests in this group shall be performed as specified in Chart IV.

The temperatures T_1, T_2 and T_3 shall be chosen such that within approximately 1000, 500 and 168 hours, the parameter(s) defined in Para. 8.3.2.3 above can be expected to have drifted to an extreme of the permitted range. A common applied power (if applicable) also determined from the Subgroup 2A tests, shall be used. If the power step-stress test was not performed, the devices shall be operated at their maximum rated dissipation. Intermediate electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times:

T_1 (1000 hrs)	T_2 (500 hrs)	T_3 (168 hrs)
168 (+24 -0) hrs	168 (+24 -0) hrs	168 (+24 -0) hrs
500 (+24 -0) hrs	500 (+24 -0) hrs	-
1000 (+24 -0) hrs	-	-

Failed components shall be removed for analysis as specified in Para. 8.1.

8.4.4 Subgroup 3C - Extended Burn-in Test

The devices shall be tested for 1000 hours at the conditions defined in the Detail Specification for burn-in. Intermediate electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times: 168 (+24 -0) hrs, 500 (+24 -0) hrs and 1000 (+24 -0) hrs. If the conditions determined for the 1000 hour subgroup in 8.4.3 above are identical to those defined for burn-in, this test shall not be performed.

8.4.5 Subgroup 3D - Extended Life Test

The Devices shall be subject to a Life test for 4000 hours at T_{amb} = +125°C per MIL-STD-883, Method 1005. Time temperature regression per MIL-STD-883 Method 1005 Class S may be applied.

Intermediate electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times: 168 (+24 -0) hrs, 500 (+24 -0) hrs, 1000 (+24 -0) hrs, 2000 (+24 -0) and 4000 (+24 -0) hrs.

8.5 GROUP 4 - RESERVE

Should any additional tests be considered necessary, the devices in this subgroup shall be used.

9 DATA DOCUMENTATION

9.1 GENERAL REQUIREMENTS

An evaluation test report shall be established. This shall comprise the following:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Sample identification.
(e) Production data.
(f) Inspection data.
(g) Initial electrical measurements.
(h) Group 1 - Control Group data.
(i) Subgroup 2A(i) - Thermal Resistance/Conductivity data.
(j) Subgroup 2A(ii) - Temperature Step-Stress test data.
(k) Subgroup 2A(iii) - Power Step-Stress test data (if applicable).
(l) Subgroup 2B - Radiation tests data.
(m) Subgroup 2C - Construction Analysis data.
(n) Subgroup 2D - Package tests data including Subgroups 2D(i), 2D(ii-a), 2D(ii-b), 2D(ii-c), 2D(iii), 2D(iv), 2D(v) (as applicable).
(o) Subgroup 2E - Electrical tests data.
(p) Subgroup 2F – Wafer Tests data (if applicable).
(q) Subgroup 3A - High Temperature Reverse Bias (HTRB) test data (if applicable).
(r) Subgroup 3B - Accelerated Electrical Endurance test data (if applicable).
(s) Subgroup 3C - Extended Burn-in test data (if applicable).
(t) Subgroup 3D – Extended Life Test data (if applicable).
(u) Group 4 - Reserve data (if applicable).
(v) Summary of results and conclusions.

Items (a) to (v) inclusive shall be grouped, preferably as subpackages, and for identification purposes, each page shall include the following information:

- Manufacturer's/test house's name.
- Lot identification.
- Date of establishment of the document.
- Page number.

9.2 COVER SHEET(S)

The cover sheet (or sheets) of the evaluation test report shall include as a minimum:

(a) Reference to this document, including issue and date.
(b) Component type and number.
(c) Lot identification.
(d) Manufacturer's/test house's name and address.
(e) Location of the manufacturing plant/test house.
(f) Signature on behalf of the Manufacturer/test house.
(g) Total number of pages of the evaluation test report.

9.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be included in the evaluation test report. Where applicable, this list shall contain the inventory number, Manufacturer type number, serial number, calibration status data, etc. This list shall indicate for which tests such equipment was used.

9.4 LIST OF TEST REFERENCES

This list shall include all references or codes which are necessary to correlate the test data provided with the applicable tests.

9.5 SAMPLE IDENTIFICATION (PARA. 5.1)

This shall identify the criteria used for the selection of the particular components used for the tests, when evaluating a range of components by means of representative samples.

9.6 PRODUCTION DATA (PARA. 5.4)

The progress of the components through the normal manufacturing processes shall be documented. The components failing a particular process shall be detailed, together with the reason for their removal.

9.7 INSPECTION DATA (PARA. 6)

The number of components subjected to each test shall be identified together with the number and reason for any rejects. Radiographs of any failed components shall be presented.

9.8 INITIAL ELECTRICAL MEASUREMENTS (PARA. 7)

All data shall be recorded against serial numbers. A histogram of device parameters shall be produced.

9.9 GROUP 1 - CONTROL GROUP DATA (PARA. 8.2)

All data shall be recorded against serial numbers.

9.10 SUBGROUP 2A - STEP-STRESS TESTS DATA

9.10.1 Subgroup 2A(i) - Thermal Resistance/Conductivity Data (Para. 8.3.2.2)

All data shall be recorded against serial numbers.

9.10.2 Subgroup 2A(ii) - Temperature Step-Stress Test Data (Para. 8.3.2.4)

All data shall be recorded against serial numbers. This shall include:

(a) Starting temperature.
(b) Temperature steps.
(c) Electrical measurements tabulated for each step.
(d) Graphical output as defined in Para. 8.3.2.6.
(e) Analysis of any failed components as defined in Para. 8.1.
(f) Thermal resistance/conductivity measurements from surviving devices as defined in Para. 8.3.2.2.

9.10.3 Subgroup 2A(iii) - Power Step-Stress Test Data (Para. 8.3.2.5) (if applicable)

All data shall be recorded against serial numbers. This shall include:

(a) Starting power.
(b) Power steps.
(c) Electrical measurements tabulated for each step.
(d) Graphical output as defined in Para. 8.3.2.6.
(e) Analysis of any failed components as defined in Para. 8.1.
(f) Thermal resistance/conductivity measurements from surviving devices as defined in Para. 8.3.2.2.

9.11 SUBGROUP 2B - RADIATION TESTS DATA (PARA. 8.3.3)

All data shall be recorded against serial numbers. This shall include:

(a) Total dose steady-state test data.

9.12 SUBGROUP 2C - CONSTRUCTION ANALYSIS DATA (PARA. 8.3.4)

All data shall be recorded against serial numbers. This shall include:

(a) Internal water vapour content data.
(b) Outgassing data (if applicable).
(c) Photographs.
(d) SEM photographs.
(e) Results of bond strength test (if applicable).
(f) Results of die shear test.
(g) Glassivation layer integrity test data (if applicable).
(h) Microsectioning photographs.

9.13 SUBGROUP 2D - PACKAGE TESTS DATA (PARA. 8.3.5)

All data shall be recorded against serial numbers. This shall include:

(a) Subgroup 2D(i) - Thermal tests data.
(b) Subgroup 2D(ii-a), 2D(ii-b) (if applicable) and 2D(ii-c) - Mechanical and Thermal Vacuum tests data.
(c) Subgroup 2D(iii) - Resistance to soldering heat test data.
(d) Subgroup 2D(iv) - Pin to pin isolation test data.
(e) Subgroup 2D(v) – Humidity test data (if applicable).

9.14 SUBGROUP 2E - ELECTRICAL TESTS DATA (PARA. 8.3.6)

All data shall be recorded against serial numbers. This shall include:

(a) ESDS test data.
(b) Characterisation data.

9.15 SUBGROUP 2F – WAFER TEST DATA (PARA. 8.3.7)

All data shall be recorded against serial numbers. This shall include:

(a) Solder Ball test data (if applicable).

9.16 GROUP 3 - ENDURANCE TESTS DATA

9.16.1 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test Data (Para. 8.4.2)

All data shall be recorded against serial numbers.

9.16.2 Subgroup 3B - Accelerated Electrical Endurance Test Data (Para. 8.4.3) (If Applicable)

All data shall be recorded against serial numbers. This shall include:

(a) Temperatures T_1, T_2 and T_3 chosen.
(b) Power chosen.
(c) Electrical measurements tabulated and plotted for each intermediate time as defined in Para. 8.4.3.
(d) Drift values referred to the initial electrical measurements (Para. 7).
(e) Analysis of any failed components as defined in Para. 8.1.

9.16.3 Subgroup 3C - Extended Burn-in Test Data (Para. 8.4.4) (If Applicable)

All data shall be recorded against serial numbers.

9.16.4 Subgroup 3D - Extended Life Test Data (Para. 8.4.4) (If Applicable)

All data shall be recorded against serial numbers.

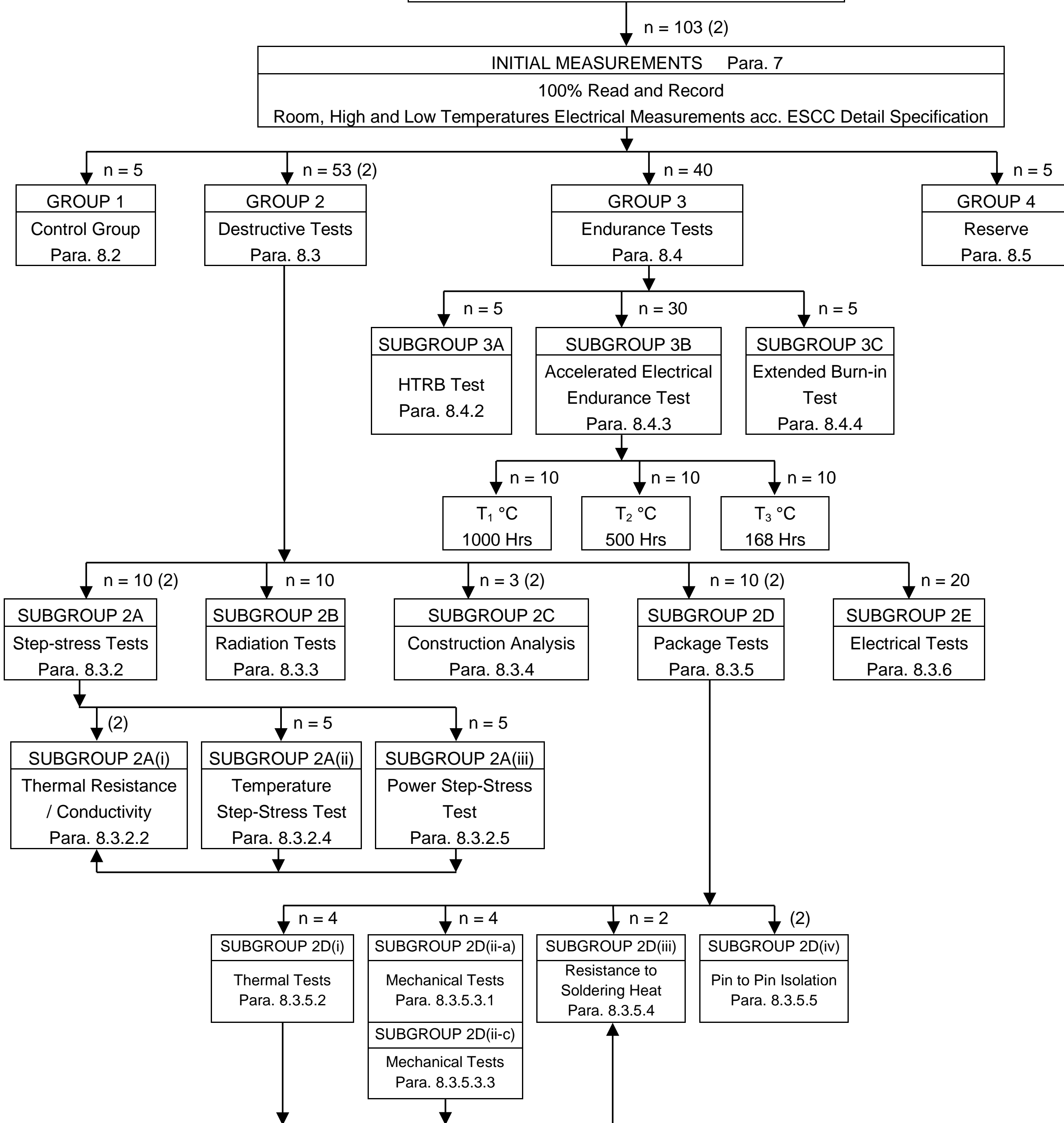
9.17 GROUP 4 - RESERVE DATA (PARA. 8.5) (IF APPLICABLE)

All data shall be recorded against serial numbers.

9.18 SUMMARY OF RESULTS AND CONCLUSIONS

The above shall be briefly reviewed, indicating the success or otherwise of the evaluation test programme. Any production screens that need to be introduced into the PID shall be outlined.

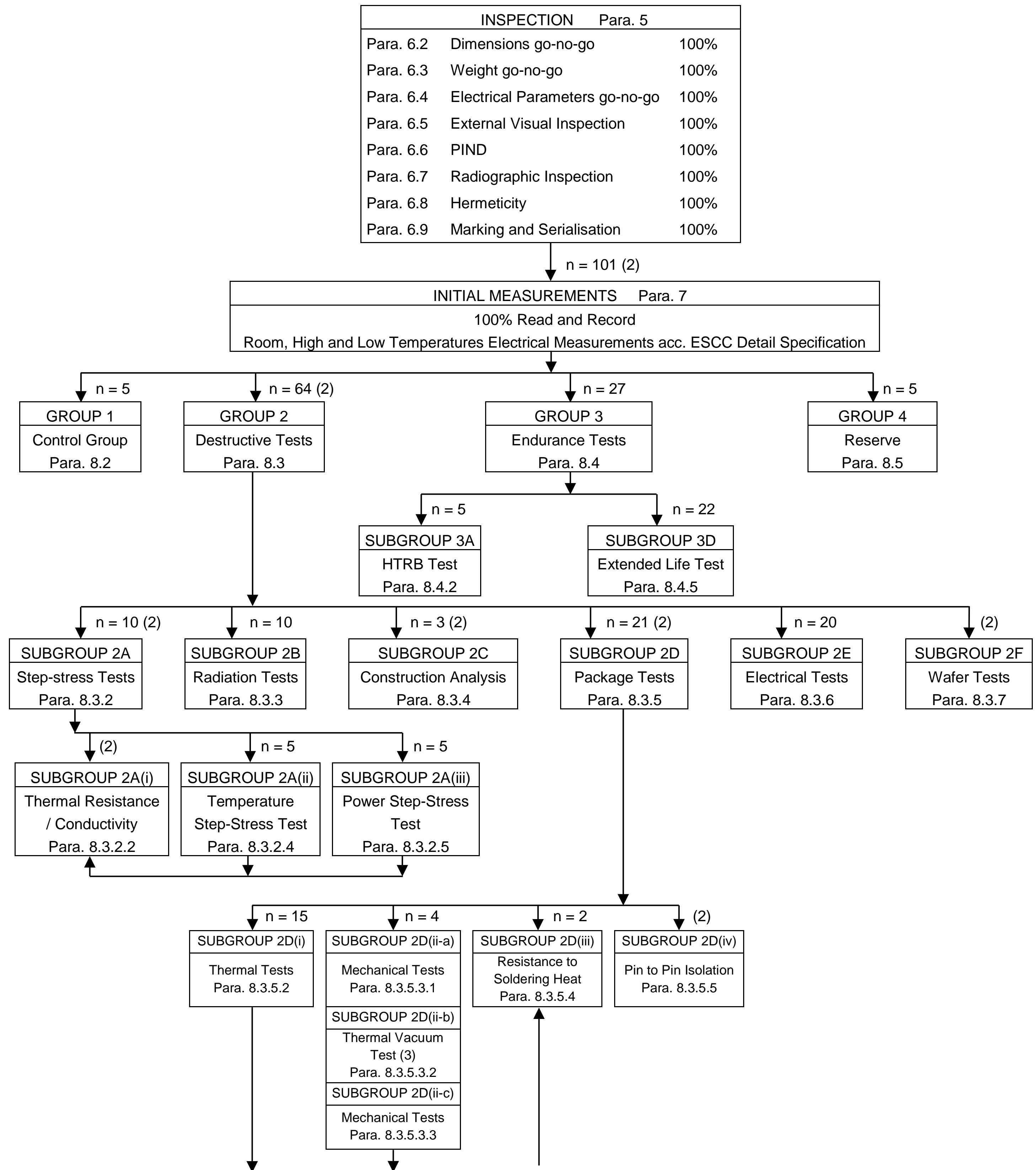
CHART I(A) – EVALUATION TEST PROGRAMME FOR WIRE-BONDED INTEGRATED CIRCUIT COMPONENTS (1)



NOTES:

1. The quantity of components required for testing in each Group and Subgroup is indicated by the letter n.
2. Additional test devices/structures/materials may also be required. See reference paragraph for details.

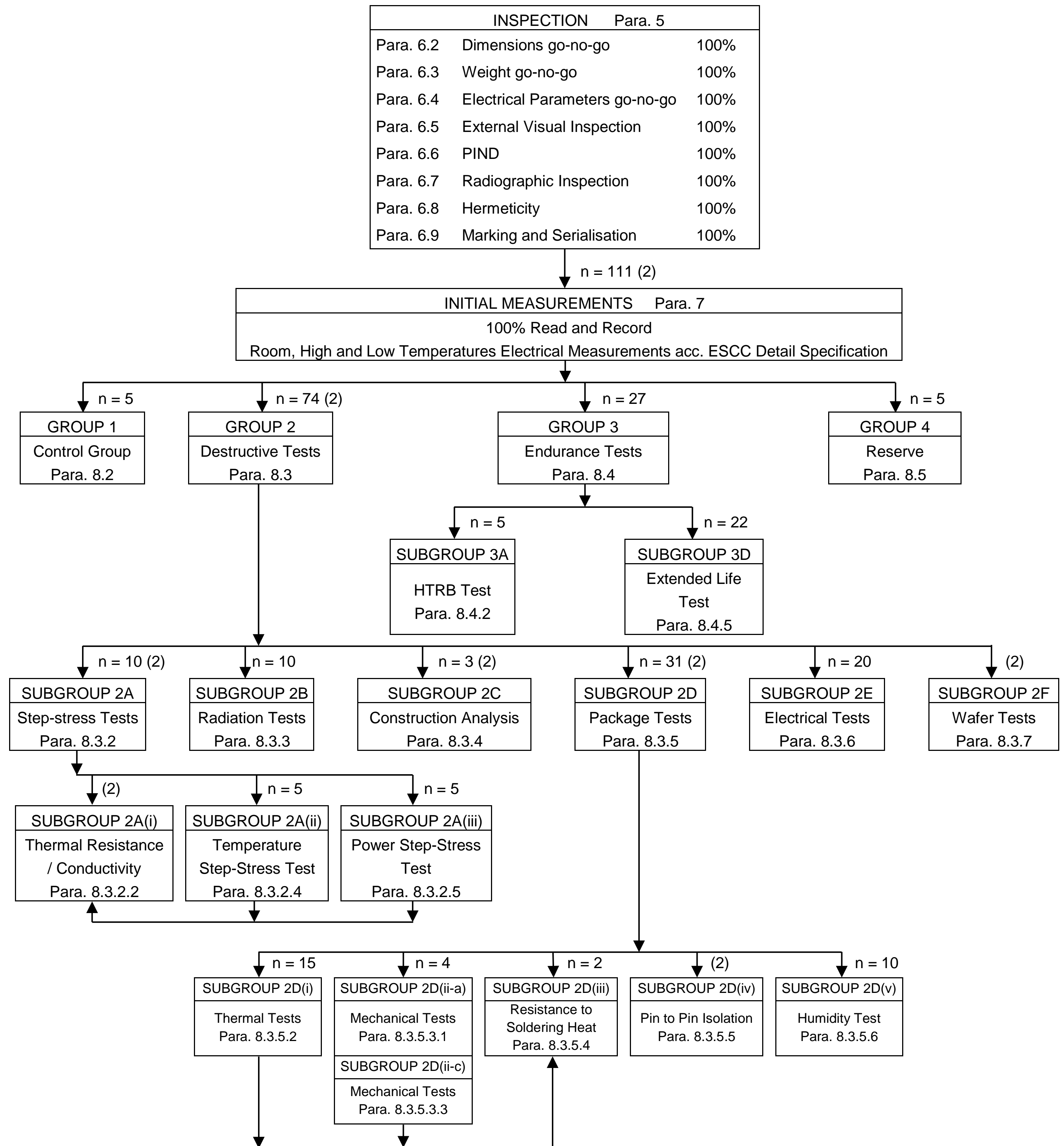
CHART I(B) – EVALUATION TEST PROGRAMME FOR HERMETIC FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS (1)



NOTES:

1. The quantity of components required for testing in each Group and Subgroup is indicated by the letter n.
2. Additional test devices/structures/materials may also be required. See reference paragraph for details.
3. Thermal Vacuum Test shall only be performed on components which have thermal interface material between the die and the lid / heat-spreader.

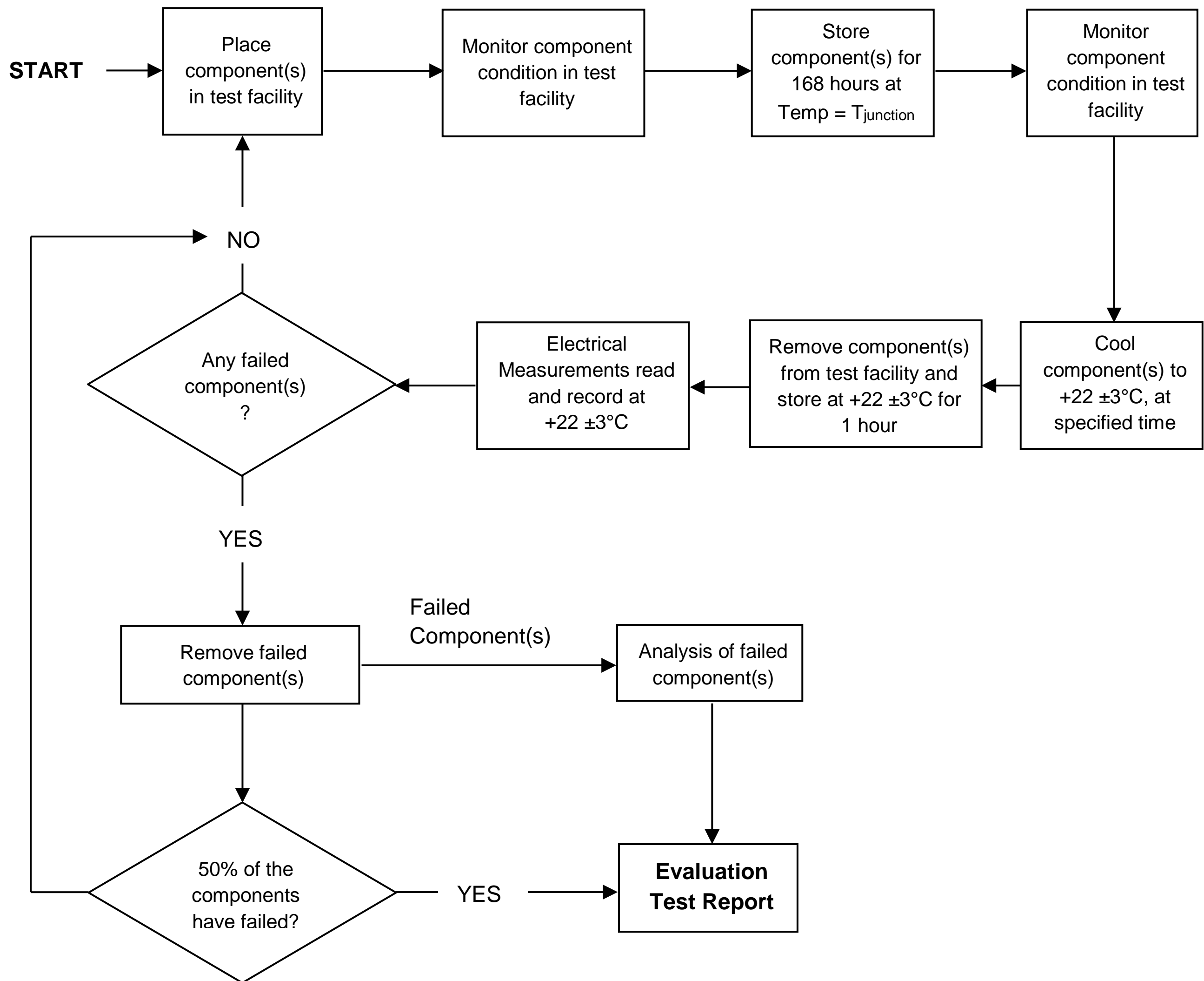
CHART I(C) – EVALUATION TEST PROGRAMME FOR NON-HERMETIC FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS (1)



NOTES:

1. The quantity of components required for testing in each Group and Subgroup is indicated by the letter n.
2. Additional test devices/structures/materials may also be required. See reference paragraph for details.

CHART II – TEMPERATURE STEP-STRESS SEQUENCE



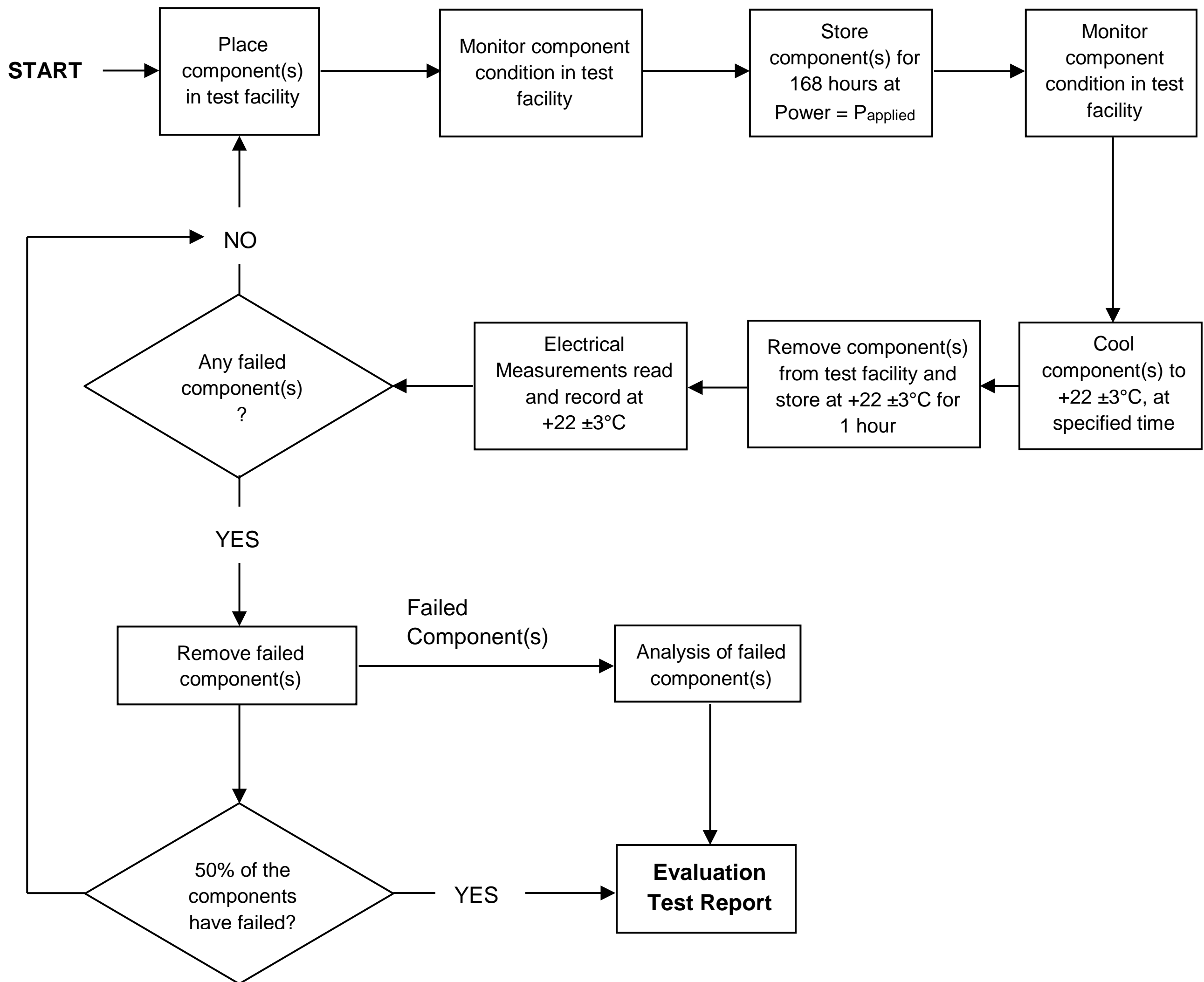
NOTES

1. Temperature steps with $T_{junction}$:

First step:	T_0	(°C)
	T_1	(°C)
	T_2	(°C)
Last step:	T_n	(°C)

with (T_n > … T_2 > T_1 > T_0)

CHART III - POWER STEP-STRESS SEQUENCE



NOTES

1. Power steps with $P_{applied}$:

First step:	P_0	(W)
	P_1	(W)
	P_2	(W)
Last step:	P_n	(W)

with ($P_n > \ldots P_2 > P_1 > P_0$)

CHART IV – ACCELERATED ELECTRICAL ENDURANCE TEST