REQUIREMENTS FOR THE

PROCESS CAPABILITY APPROVAL

FOR

MANUFACTURING LINES

OF

HERMETIC HYBRID MICROCIRCUITS

ESCC Basic Specification No. 2566000

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DCR No.	CHANGE DESCRIPTION
1119	Specification upissued to incorporate changes per DCR.

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1 PURPOSE AND SCOPE

The purpose of this specification is to define the requirements for the Process Capability Approval (PCA) of a manufacturing line of Hermetic Hybrid Microcircuits intended for space application.

This specification:

- provides the specific requirements which a manufacturer has to fulfil in order to be successfully evaluated and capability approved for a set of materials and processes used on a manufacturing line to construct hermetic Hybrid Microcircuits and for this capability to be described and published in REP007 (ESCC List of PCA certificates).
- is applicable to substrate and interconnect technologies (see paragraph 3.2)
- shall be read in conjunction with ESCC Basic Specification 25600 which provides the general requirements for Process Capability Approval.

NOTES

- This specification does not provide requirements for the PCA of a manufacturing line of any devices which are not designed to be hermetic.

2 APPLICABLE DOCUMENTS

The following specifications form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect at the date of commencement of a particular task, as applicable and as required for each stage of the sequence of activities which may lead to the PCA certification of the manufacturing line.

2.1 ESCC SPECIFICATIONS

ESCC 25600 Requirements for the Process Capability Approval

ESCC 21300 Terms, Definitions, Abbreviations, Symbols and Units

ESCC 21500 Calibration System Requirements

ESCC 24600 Minimum Quality Management System Requirements

ESCC 22800 ESCC Non-Conformance Control System

ESCC 24900 Minimum requirements for controlling environmental contamination of components

ESCC 24800 Resistance to solvents of marking, materials and finishes

ESCC 2026000 Checklist for Hybrids Manufacturers and Line survey

ESCC 2276000 Guidelines for the PID of Hybrid manufacturers

2.2 OTHER APPLICABLE DOCUMENTS

The following documents are applicable to the extent specified herein. The relevant issues shall be those in effect at the date of commencement of a particular task, as applicable and as required for each stage of the sequence of activities which may lead to the PCA certification of the manufacturing line.

ECSS-Q-ST-60-05	Generic Procurement Requirements for Hybrids
ECSS-S-ST-00-01	Glossary of Terms
MIL-STD-883	Test Method Standard Microcircuits
MIL-STD-750	Test Method Standard Test Methods for Semiconductor Devices
MIL-STD-202	Test Method Standard Electronic and Electrical component parts
ISO 14644-1	Cleanrooms and Associated Controlled Environments - Part 1: Classification of Air Cleanliness
IPC-9191	General Guidelines for Implementation of Statistical Process Control
IPC-9199	Statistical Process Control (SPC) Quality Rating

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

3.1 TERMS FROM OTHER STANDARDS

For the purpose of this Standard, the terms, definitions, abbreviations, symbols and units defined in ESCC Basic Specification No. 21300 and ECSS-S-ST-00-01 apply, plus specific terms as in 3.2.

3.2 TERMS SPECIFIC TO THE PRESENT STANDARD

Hybrid microcircuit

Combination of elements (interconnection substrate, added active or passive chips) sealed inside a package, in order to perform an electronic function

NOTES

1. Interconnection substrate (e.g. thick film, thin film, co-fired, DBC) can be with or without integrated passive components (e.g. resistors, inductors, capacitors).
2. Active parts can be monolithic or discrete, chips or packaged components.
3. Electronic functions that are performed by hybrids include digital or analog, low frequency or radiofrequency, low power or high power functions. These functions may be mixed according to the application.
4. The terms “hybrid circuits” and “hybrids” are synonymous for “hybrid microcircuits”.

Production lot

Number of units of a single device type manufactured on the same production line using the same production techniques, in one uninterrupted period, according to the same component or part design and having the same chip lots and the same materials (as defined in ECSS-Q-ST-60-05)

Statistical Process Control (SPC)

Statistical Process Control is the use of statistical techniques and tools for monitoring a process through the use of control charts, to warn when the process is moving away from predetermined limits always before non conformance occurrence, in accordance with IPC-9191 and IPC-9199.

Design of Experiments (DoE)

Design of Experiments is a structured, organized method for determining, with a reduced number of experiments, the effect of process parameters on a process result (for determination of influent parameters) and the correlation between parameters (for process optimization).

Semi-finished Product

A Semi-finished product is a product performing a specific function procured from an external supplier entering the fabrication flow of a hybrid (for example: package, interconnection substrate etc.) not produced by the hybrid manufacturer itself.

External Sub-contractor

A company different from the hybrid manufacturer that performs a particular process step used in the hybrid fabrication flow mentioned in the PID

Rework

Action to correct a defect of a product that does not lead to a configuration item change

1. Unlike repair, rework does not affect or modify parts of the defective product.
2. No NCR needs to be raised.

Repair

Action to correct a defect of a product that leads to a configuration item change

1. Unlike rework, repair affects or modifies parts of the defective product.
2. An NCR needs to be raised for the configuration item change.

3.3 ABBREVIATED TERMS

The following abbreviations are used within this document:

Abbreviation	Meaning
CTA	Circuit Type Approval
DBC	Direct Bond Copper
DoE	Design of Experiments
DPA	Destructive Physical Analysis
ECSS	European Cooperation for Space Standardisation
ESCC	European Space Components Cooperation
ESD	Electrostatic discharge
ETP	Evaluation Test Programme
HTCC	High Temperature Co-fired Ceramic
HTIF	Hybrid Technology Identification Form
I/O	Input / Output
ISP	Integrated Substrate Package
LAT	Lot Acceptance Testing
LF	Low Frequency
LTCC	Low Temperature Co-fired Ceramic
NCR	Non Conformance Report

PCA	Process Capability Approval
PID	Process Identification Document
PIND	Particle Impact Noise Detection
QA	Quality Assurance
QS	Quality System
RF	Radio Frequency
RGA	Residual Gas Analysis
SEC	Standard Evaluation Circuit
SEM	Scanning Electron Microscope
SPC	Statistical Process Control
TCR	Temperature Coefficient of Resistance
TRB	Technology Review Board
TVCA	Test Vehicle for Capability Approval
TVE	Test Vehicle for Evaluation

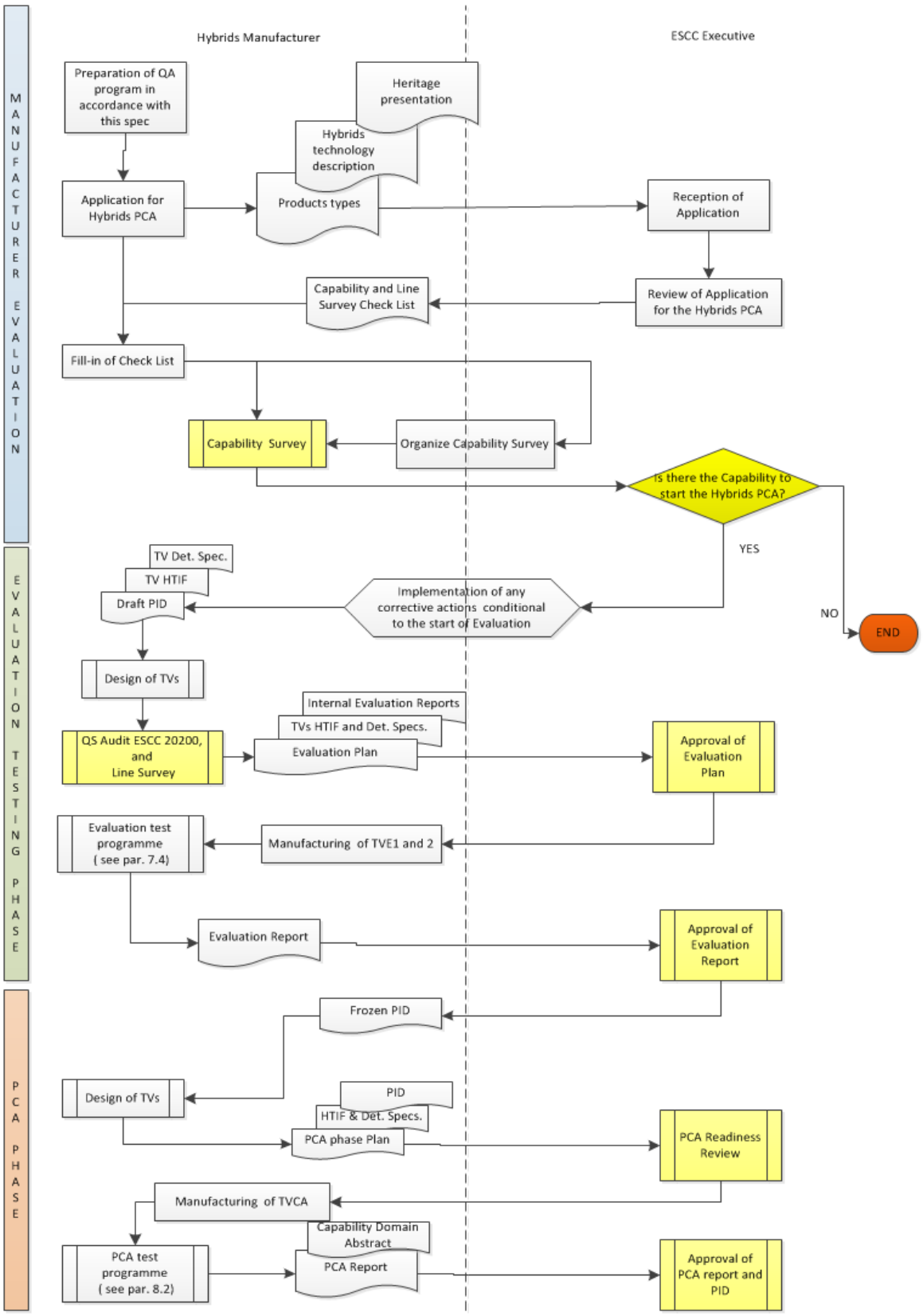
4 DEFINITION OF PROCESS CAPABILITY APPROVAL FOR HYBRID LINES

The ESCC Process Capability Approval (PCA) of Hermetic Hybrid Manufacturing Lines shall include the 4 stages specified in ESCC Basic Specification 25600, namely

- Manufacturer Evaluation,
- Definition of the Capability Domain,
- Evaluation Phase and
- PCA Phase testing.

The successful completion of these stages requires, therefore, the definition of the PCA and its boundaries, the preparation, review and approval of the relevant PID and the actual completion of test sequences specified for Evaluation testing and PCA testing.

The flow to attain the PCA of an Hybrid Line is described in Flow Chart 1.


MANUFACTURER EVALUATION
EVALUATION TESTING PHASE
PCA PHASE
Hybrids Manufacturer
ESCC Executive
Preparation of QA program in accordance with this spec
Heritage presentation
Hybrids technology description
Application for Hybrids PCA
Products types
Reception of Application
Capability and Line Survey Check List
Review of Application for the Hybrids PCA
Fill-in of Check List
Capability Survey
Organize Capability Survey
Is there the Capability to start the Hybrids PCA?
YES
NO
END
TV Det. Spec.
TV HTIF
Draft PID
Implementation of any corrective actions conditional to the start of Evaluation
Design of TVs
Internal Evaluation Reports
TVs HTIF and Det. Specs.
QS Audit ESCC 20200, and Line Survey
Evaluation Plan
Approval of Evaluation Plan
Evaluation test programme (see par. 7.4)
Manufacturing of TVE1 and 2
Evaluation Report
Approval of Evaluation Report
Frozen PID
Design of TVs
PID
HTIF & Det. Specs.
PCA phase Plan
PCA Readiness Review
Manufacturing of TVCA
Capability Domain Abstract
PCA test programme (see par. 8.2)
PCA Report
Approval of PCA report and PID

Flow Chart 1

5 DEFINITION OF THE PROCESS CAPABILITY DOMAIN AND ITS BOUNDARIES

In addition to the requirements of ESCC 25600, the following is specific and applicable to the Definition of the capability domain, and the preparation of the Capability Abstract, of Hybrid Manufacturers for the purpose of PCA.

5.1 GENERAL

The Manufacturer shall define the process capability domain for which process capability approval is sought as required in ESCC 25600. This definition shall result in the Capability Abstract and the PID.

The Capability Abstract and the PID have to demonstrate that the Process capability domain represents a structured, properly controlled and monitored manufacturing process for hybrid microcircuits.

The definition of the process capability domain shall address the areas listed in the rest of this paragraph at least to the extent detailed therein. Additional information shall be supplied whenever necessitated by the particular capability domain under approval.

Within the definition of the PCA for Hybrid manufacturing lines, the following areas are of particular concern and are therefore the object of specific requirements in the rest of this paragraph:

- Materials, Processes and add-on parts
- Physical design
- Inspection and test
- Traceability

The manufacturer shall describe the type of functions / products which are planned to be developed and manufactured, in term of power dissipation (Low/ High Power), maximum current / voltage, signal frequency (Low / Radio Frequency), digital / analog functions, mixed functions, etc.

When existing, heritage of hybrids design, qualification and manufacturig activities shall be presented in order to define the capability abstract. Existing PID shall be considered.

5.1.1 Materials and processes

Annex 1 gives requirements guidelines for the materials and processes description anticipated to be included in the PCA application

5.1.2 Physical Design

The manufacturer shall specify physical design rules that define the construction and composition of all items foreseen for the production of hybrid microcircuits within the process capability domain. Methodologies and procedures used by the manufacturer to validate their design shall also be addressed.

The design rules shall at least cover the following:

- Substrate and carrier physical constraints
- Conductor, termination and wire bonding physical constraints
- Thick film, thin film circuit physical constraints
- Electrical design constraints, including Multipaction and Corona effects
- Package Assembly and encapsulation

5.1.3 Inspection and test

The Manufacturer shall describe the methods applicable for inspections and test, including references to the documents specifying those methods.

At least the following areas shall be covered:

- Materials, piece parts and EEE add-on parts Incoming Inspection
- In-process inspections
- Internal and external visual inspection

5.1.4 Traceability

The Manufacturer shall describe his methods for assuring traceability of materials, piece parts, EEE add-on parts, test and manufactured items. At least the following points shall be covered:

- The use of purchase orders and specifications
- The use of route sheets and travellers
- The traceability of materials, piee parts and EEE add-on parts
- The traceability of test structures
- The traceability of manufactured items

5.2 THE PID OF A HYBRID MANUFACTURER

5.2.1 General

A PID for the process capability domain to be approved shall be prepared per ESCC 2276000.

5.2.2 Review and approval of the PID

The PID will contain the complete definition of the Capability Domain and will be updated into a stable state at the end of the Evaluation phase so that its review and approval by the ESCC Executive becomes a mandatory pre-requisite for the commencement of the PCA testing phase.

The complete PID, comprising all called-up specifications, shall be kept by the manufacturer at the production plant. It shall be made available to the ESCC Executive or its designated representative for review.

Any deviation from the PID shall be subjected to the ESCC Executive for approval.

A condensed PID, comprising all basic information, e.g. flow-charts, lists of specifications, materials, processes, organization/responsibility, equipments and layouts but complemented by copies of only the agreed specifications, shall be kept by the ESCC Executive and treated as proprietary information.

6 MANUFACTURER EVALUATION

In addition to the requirements of ESCC Basic Specification 25600, the following is specific and applicable to the Evaluation of Hybrid Manufacturers for the purpose of PCA.

The following activities shall be carried out during the manufacturer evaluation phase:

- Capability survey. This survey is made to assess a manufacturer's general capability for the production of reliable Hybrid Microcircuits.

– Line survey. This survey consists of an assessment of a manufacturer's technology and production line based on applied processes and controls and a detailed review of existing test data.

In general, to enable the survey team of the ESCC Executive to carry out the capability survey, the line survey and the manufacturer audit, the manufacturer shall grant free access to the facilities concerned. He shall also enable the team to witness any development, engineering, production and quality assurance operations involved in the processes for which approval is sought.

To facilitate the evaluation procedure for capability survey, line survey and manufacturer audit, the checklist based on ESCC Basic Specification 2026000 shall be used.

7 EVALUATION OF THE PROCESS CAPABILITY DOMAIN

7.1 GENERAL

The evaluation phase of the process capability domain of Hybrid Manufacturing Lines shall be as specified in ESCC Basic Specification 25600 with additional requirements set in the rest of this paragraph.

7.2 EVALUATION TEST PROGRAMME

7.2.1 General

The Evaluation testing to be performed on test structures representative of the hybrid process under approval shall be in accordance with an Evaluation Test Programme (ETP) which shall, as a minimum, conform to the requirements of this paragraph.

The test structures used for Evaluation testing are called Test Vehicles (TVE). The quantity and type of samples to be used for the ETP shall be agreed by the ESCC Executive and the manufacturer. The samples shall also be the most suitable for highlighting those characteristics and parameters that are pertinent to an investigation on failure modes and weaknesses.

Upon completion of evaluation testing, the final definition of the process capability domain and its boundaries shall be agreed between the Manufacturer and the ESCC Executive, and the Process Capability Abstract shall be issued.

7.2.2 Description of Test Vehicles (TVE)

7.2.2.1 General

On the basis of materials, processes and sub-techniques proposed by the manufacturer for approval, the manufacturer shall define the test vehicles implementing the different sub-techniques and their related limits.

To cover all the different sub-techniques, a minimum of two types of test vehicle shall be used:

– One type addressing the substrate technology (TVE1)
– One type addressing the assembly of added-on parts and the actual packaging technique (TVE2)

TVE1 test vehicle shall consist of the main substrate mounted and connected with a selected packaging technology that is representative of the packaging technique used for the hybrid process. The number of I/O pins shall be enough to perform the electrical measurements.

TVE2 test vehicle shall be encapsulated with the actual packaging technique. The package used for TVE2 may be different from the actual package planned for the hybrid but shall in any case cover the technology domain under approval.

In order to cover the full Process Capability Domain it might be necessary to define several Test Vehicles of the type TVE1 and/or TVE2 above.

If proposed by the manufacturer, and in accordance with the ESCC Executive, some Evaluation test vehicles may be intentionally repaired (and/or reworked) and the traceability of the various repair/rework operations established accordingly. These repaired/reworked devices shall be clearly identified and submitted to the same test campaign as the non-repaired/reworked hybrid components.

The manufacturer shall write a specification in accordance with ECSS-Q-ST-60-05, Annex B, for each test vehicle to be evaluated and submit it to the ESCC Executive for approval.

7.2.2.2 Definition of TVE1 test vehicle

This test vehicle shall be representative in terms of:

- Maximum X Y dimensions, minimum thickness package and bulk substrates
- Maximum number of conductive layers and associated dielectric layers
- Typical thicknesses of conductive and dielectric layers
- Minimum and typical line width/space
- Minimum and typical via/holes dimensions and typical density
- Minimum and maximum dimensions of resistors in all paste decades for both trimmed and un-trimmed resistors
- Protective coverglaze on conductive and/or resistive layer (if any): material, deposition process, thickness

NOTE: In case of matrix production, the vendor shall assess the worst position on the tile and include in the test vehicles configuration

This type of test vehicle shall be designed with specific patterns to assess the performance of :

- The conductor/dielectric network (multilayer structure) :
  - Conductor resistance
    - On each conductor layer through Greek pattern (about one substrate perimeter long) with a minimum of two different line widths (see example TVE1, pattern A1, A2)
    - On a chain of a minimum of 200 vias between two adjacent conductive layers (one chain on the substrate and one chain on the top of the multilayer network) with a minimum of two different line widths (see example TVE1, pattern B)
    - On a chain of a minimum of N* vias interconnecting all the conductive layers with a minimum of two different line widths (* N = 100 x number of conductive layers) (see example TVE1, pattern D)

- Insulation resistance
  - Between two coplanar adjacent lines through Greek pattern (about one substrate perimeter long) with different space widths (see example TVE1, pattern A1, A2)
  - Between one couple of interlaced lines (about one substrate perimeter long) with different space widths (one couple on the substrate and one couple on the top of the multilayer network) (see example TVE1, pattern B)
  - Between two ground planes (about 10 % of the total substrate area) located on each conductor layer (see example TVE1, pattern E)

- Capacitance
  - Between coplanar adjacent lines in Greek pattern (about one substrate perimeter long) with two different line widths (see example TVE1, pattern A1, A2)
  - Between each Greek line and a ground plane separated by one dielectric level (see example TVE1, pattern A1, A2)
  - Between two ground planes (about 10 % of the total substrate area) separated by one dielectric level (see example TVE1, pattern E)

- Dielectric strength
  - Between all ground planes (about 10 % of the total substrate area) separated by one dielectric level

– The conductor network (monolayer structure) for high power and/or high current applications
  - Conductor resistance on the conductor layer with different line width
  - Current density on the conductor layer with different line width for long term current density evaluation and for destructive test on specific patterns.

– The resistor network (deposited directly on substrate or on dielectric/ trimmed or not/encapsulated or not):
  - Resistor value
  - Temperature coefficient of resistance (TCR)
  - Maximum power dissipation

  For minimum/medium/maximum resistivity, the minimum number of resistors shall be: 4 resistors of minimum length and 4 resistors of maximum length.
  NOTE: Each combination of resistor / conductor termination shall be evaluated.

7.2.2.3 Definition of TVE2 test vehicle

This test vehicle shall be representative in terms of:

– Maximum X Y, Minimum Z dimensions.
– Representative substrate in terms of :
  - Total number of dielectric layers for multilayer structures
  - Total thickness (Z)
  - External conductor layers
  - Configurations of wire interconnections at different conductor layer level (if applicable)
  - Metallized holes in contact with attachment medium (grounding connections, if applicable)
– Added-on parts (active and passive components/carrier/substrate)
  - Types and manufacturers
  - Termination finish
  - Minimum and maximum dimensions (two components per size)
– Added-on parts assembly

- Attachment medium
- Interconnection technologies
  - Each part shall be connected to the substrate/package
  - In addition, a “daisy chain” consisting of a minimum of 100 loops per process/material/diameter wire (or ribbon) shall be implemented in the case of Chip & Wire technology (according to the manufacturer technology the number of loops may be reduced in case of heavy wires)

– Encapsulation
  - Hermetic

This test vehicle shall be designed to evaluate :

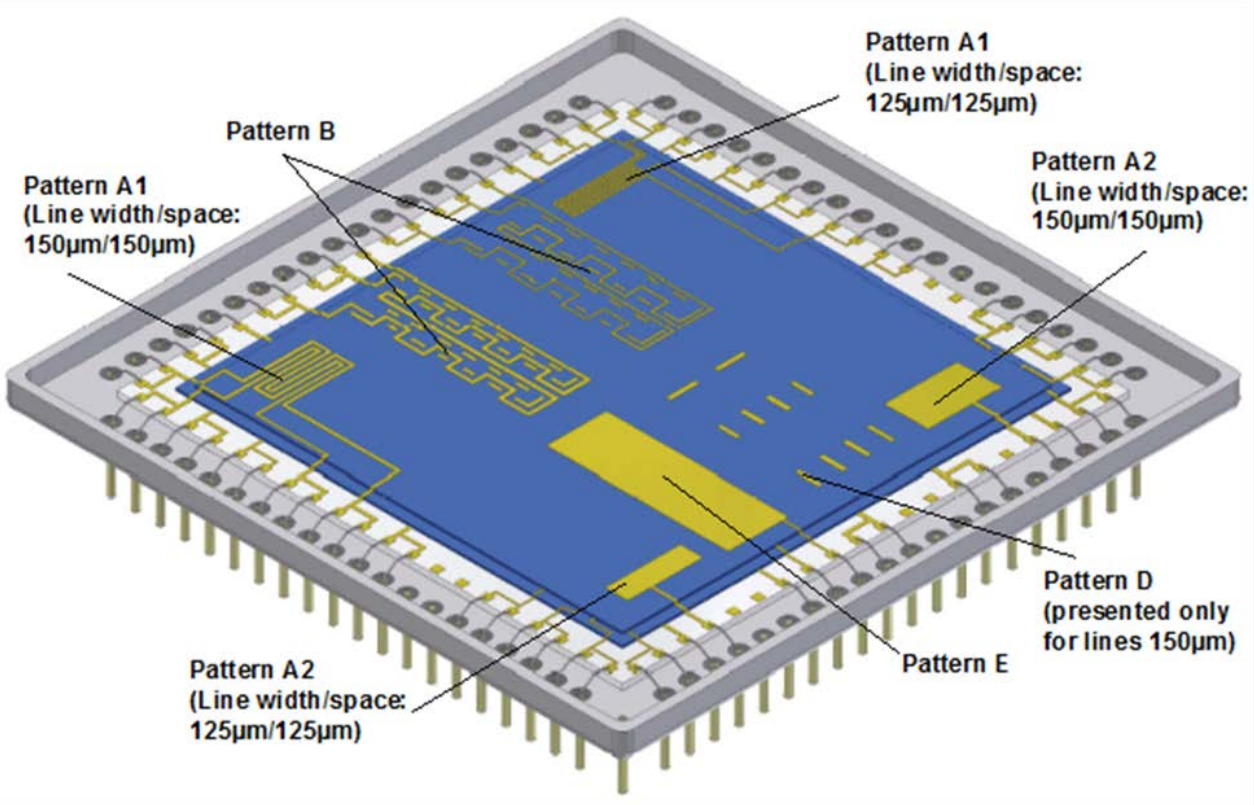
– The main electrical parameters related to the added-on passive and discrete active components (and integrated circuits, if possible)
– The mechanical (and electrical, when applicable) performance of attachment medium (adhesive bonded or soldered joints)
– The mechanical and electrical performance of bonding wires or ribbons
– The behavior of the encapsulation with respect to the environmental stresses (thermo-mechanical, humidity, contamination)

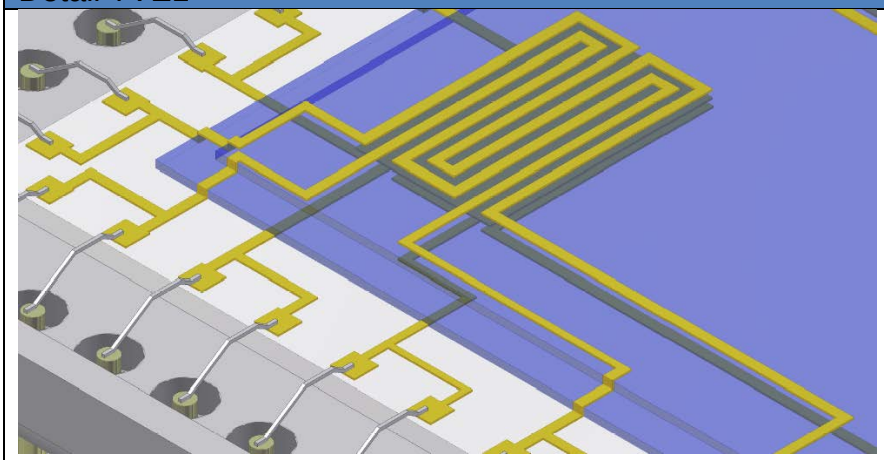
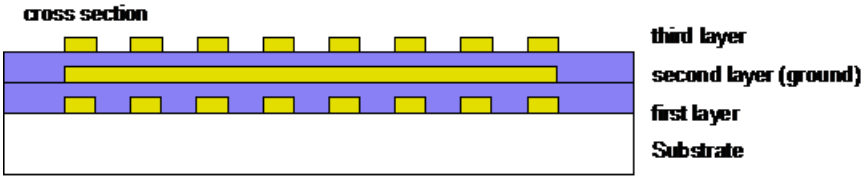
7.2.3 Examples of the two Evaluation Test Vehicles

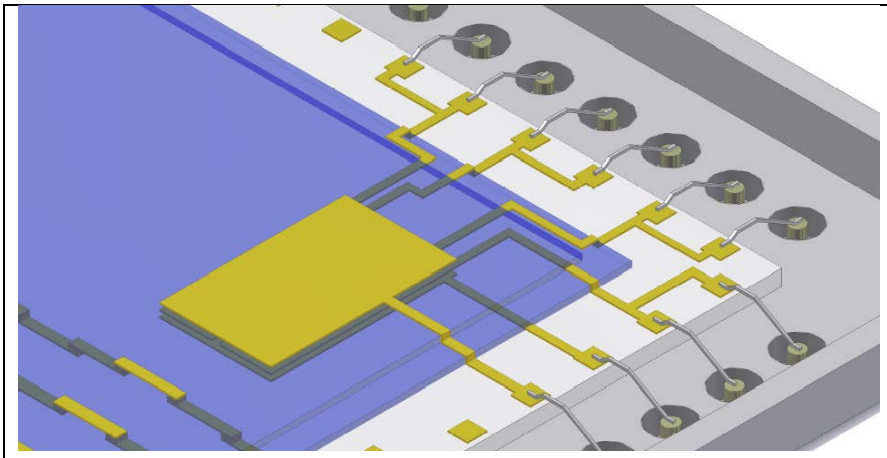
The following drawings are provided for general guidance. The manufacturer shall propose, for its evaluation, layouts that cover the full domain of technologies and added-on parts that he wishes to evaluate.

TVE1 test vehicle (thick film multilayer, 3 conductive levels)

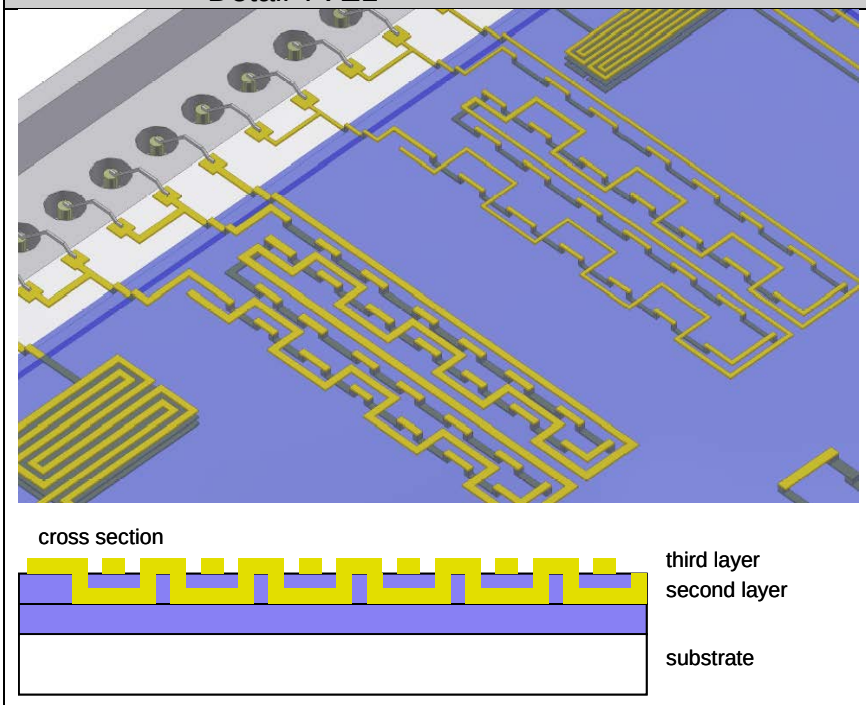
Overview

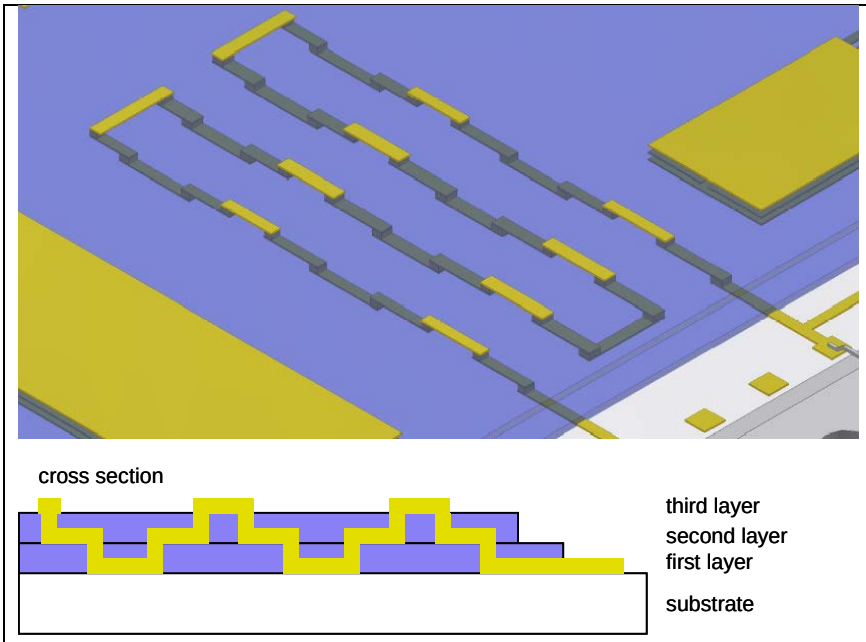
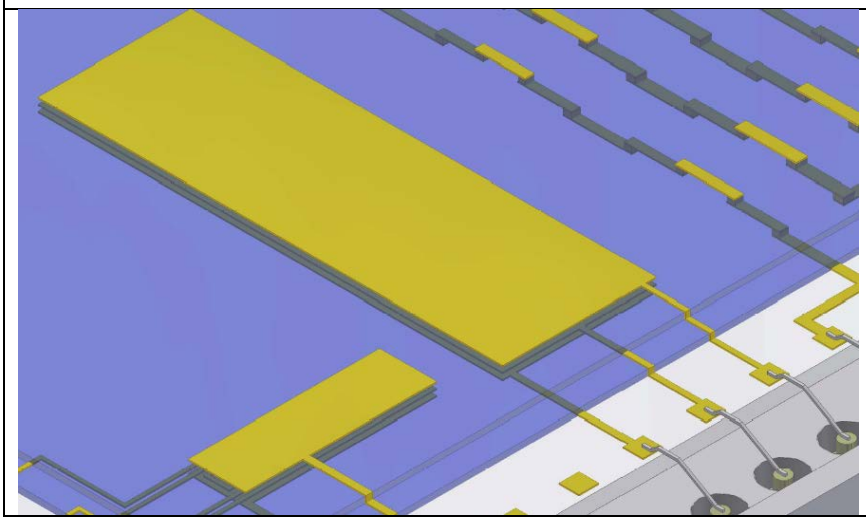


Detail TVE1	Description
 	**Pattern A1** Measurement of : – Conductor resistance at first layer (conductor on substrate) and third layer (conductor on top dielectric layer) – Insulation resistance between the adjacent coplanar lines – Capacitance between the adjacent coplanar lines – Capacitance between each line and the ground plane (second layer)

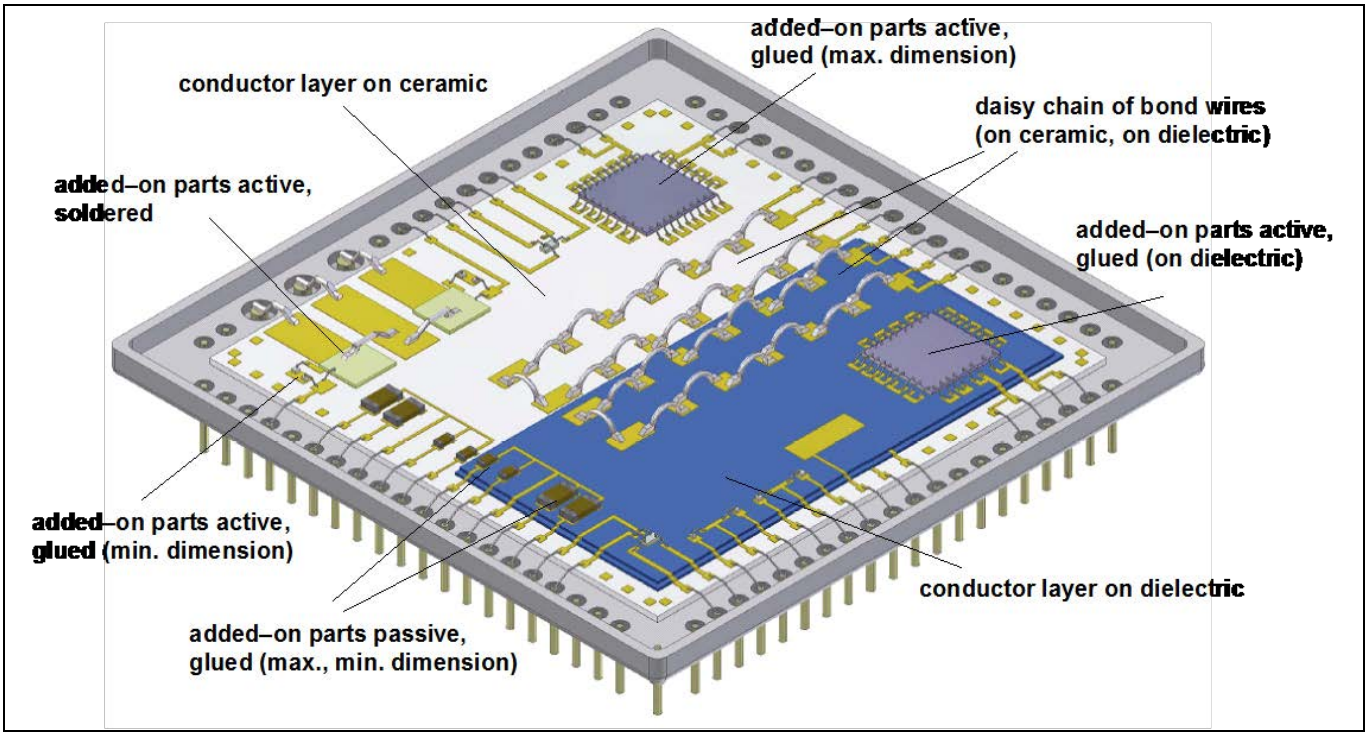


Pattern A2
Measurement of :
- Conductor resistance at the Greek pattern on second layer (same as in pattern A1)
- Insulation resistance between the coplanar adjacent lines
- Capacitance between the coplanar adjacent lines
- Capacitance between each line and the ground planes (first and third layer)

Detail TVE1	Description
	**Pattern B** Measurement of : – Resistance of a chain of vias between second and third conductive layer (on top of the multilayer network) – Insulation resistance between different interlaced lines on coplanar adjacent and superposed adjacent layers (on top of the multilayer network)

	**Pattern D** Measurement of the conductor resistance of a chain (lines and vias), interconnecting all of the three conductive layers .
	**Pattern E** Measurement of : – Insulation resistance between the ground planes on the different conductive layers (first-second, second-third) – Capacitance between the superposed adjacent ground planes

TVE2 test vehicle (thick film multilayer, 3 conductive levels)



7.3 MANUFACTURER'S AUDIT

The Manufacturer Quality Management System Audit shall take place as part of the PCA Evaluation stage. This audit shall assess the manufacturer's quality management system and his ability to successfully execute a contract for the supply of high reliability Hybrid Microcircuits. The manufacturer shall have in place a Quality System according to ESCC 24600. The Line Survey, shall take place in parallel to the QMS Audit, and shall be performed against the Check List ESCC 2026000.

7.4 EVALUATION TESTING

7.4.1 General

Evaluation testing of test structures shall generally consist of the tests and subgroups given in Chart 2.1 of this specification. Samples to be submitted to Chart 2.2 shall be test structures as defined in Para. 7.2.2 of this specification and the PID. Test structures shall be randomly divided into the various test subgroups. Unless otherwise agreed with the ESCC Executive, when different types of test structure are being tested, each type shall be represented in each subgroup.

All test structures shall be serialized prior to testing. For each measurement or inspection performed, the results shall be recorded and summarized in terms of serials number and quantity tested, quantity passed and quantity rejected failed. If test structures are rejected failed, the reason shall be clearly identified through an adequate failure analysis.

All failed test structures shall be subjected to failure analysis. The depth of the analysis shall depend on the circumstances in which failure occurred and upon whether useful information can be gained. As a minimum, the failure mode shall be determined in each case. Test structures not failing catastrophically, i.e. those displaying out of tolerance electrical rejects, shall not be removed from the test sequence but may be used, with the agreement of the ESCC Executive, as additional

test samples for evaluation testing as defined in Chart 1 in order to monitor and observe the degradation trends. In no case shall these parts substitute good parts.

For TVEs representative of large or complex hybrids, the sample size may be reduced, provided that the design of TVE includes statistically meaningful number of each subtechniques. A proposal of sample size shall be introduced in the test plan to be submitted to ESCC Executive approval

7.4.2 Initial DPA and Reference devices

A reference device of each type of test structure shall be kept for comparison purposes. Whenever electrical measurements are performed on any test structure during evaluation testing the reference deviceof the same type shall also be measured.

A supplementary test vehicle shall be used for initial DPA without burn-in simulation (TVE1) or with burn-in simulation (TVE2) for internal water-vapor content test

7.4.3 Test plans

Testing, analysis of test results and definition of the evaluation test programme shall be in accordance with the test plan and tables specified herein for each test vehicle.

The test plans and the definition of test vehicles proposed by the manufacturer shall be submitted to the ESCC Executive for approval prior to commencing the tests.

The following test plans shall be applicable to the test vehicles TVE1 and TVE2.

The numbers in brackets for each test correspond to the test number of the table “test methods and conditions” (paragraph 7.4.4).

CHART 2.1. EVALUATION TEST PLAN FOR TEST STRUCTURES TVE1 (NOTE 0).

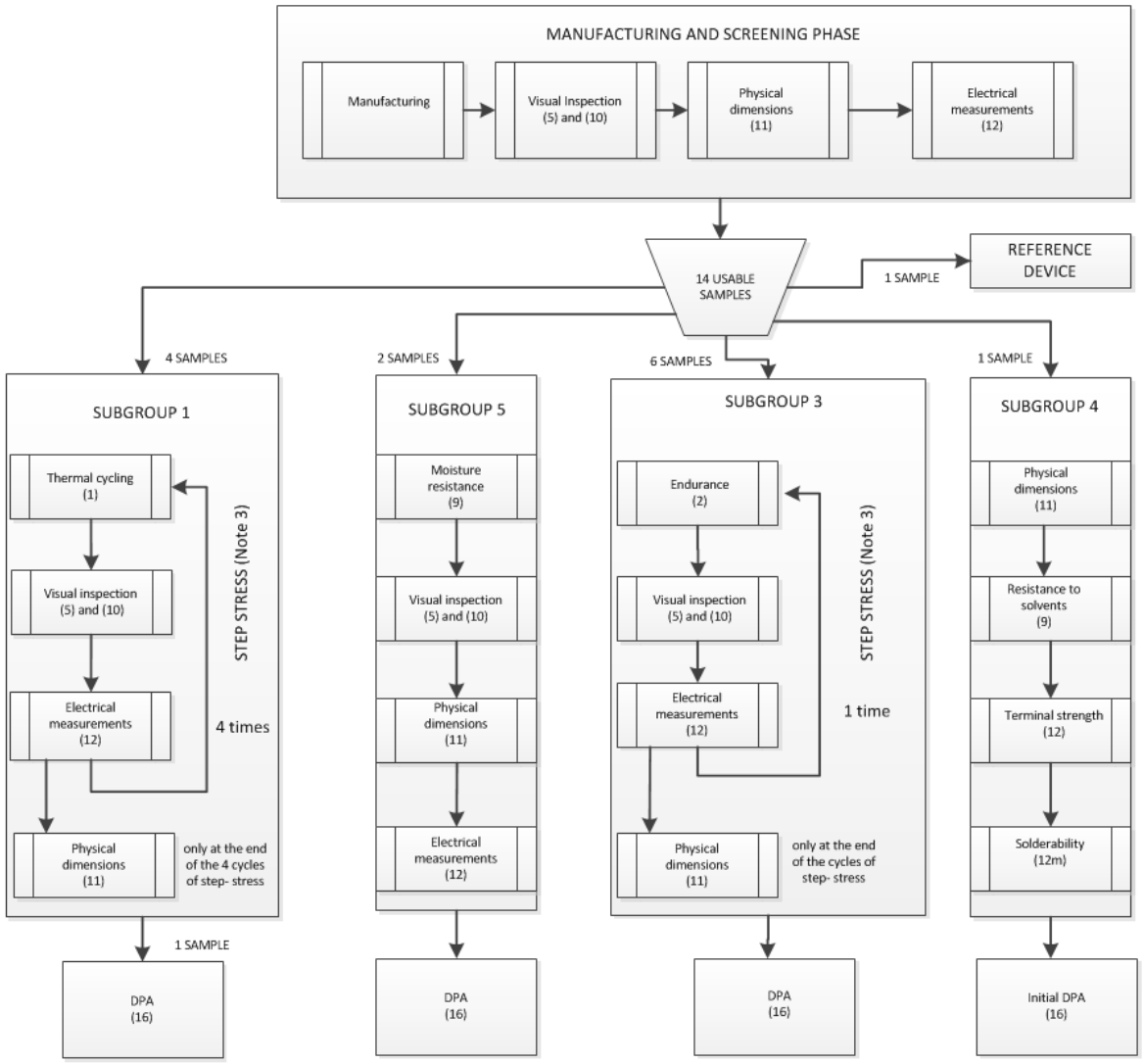
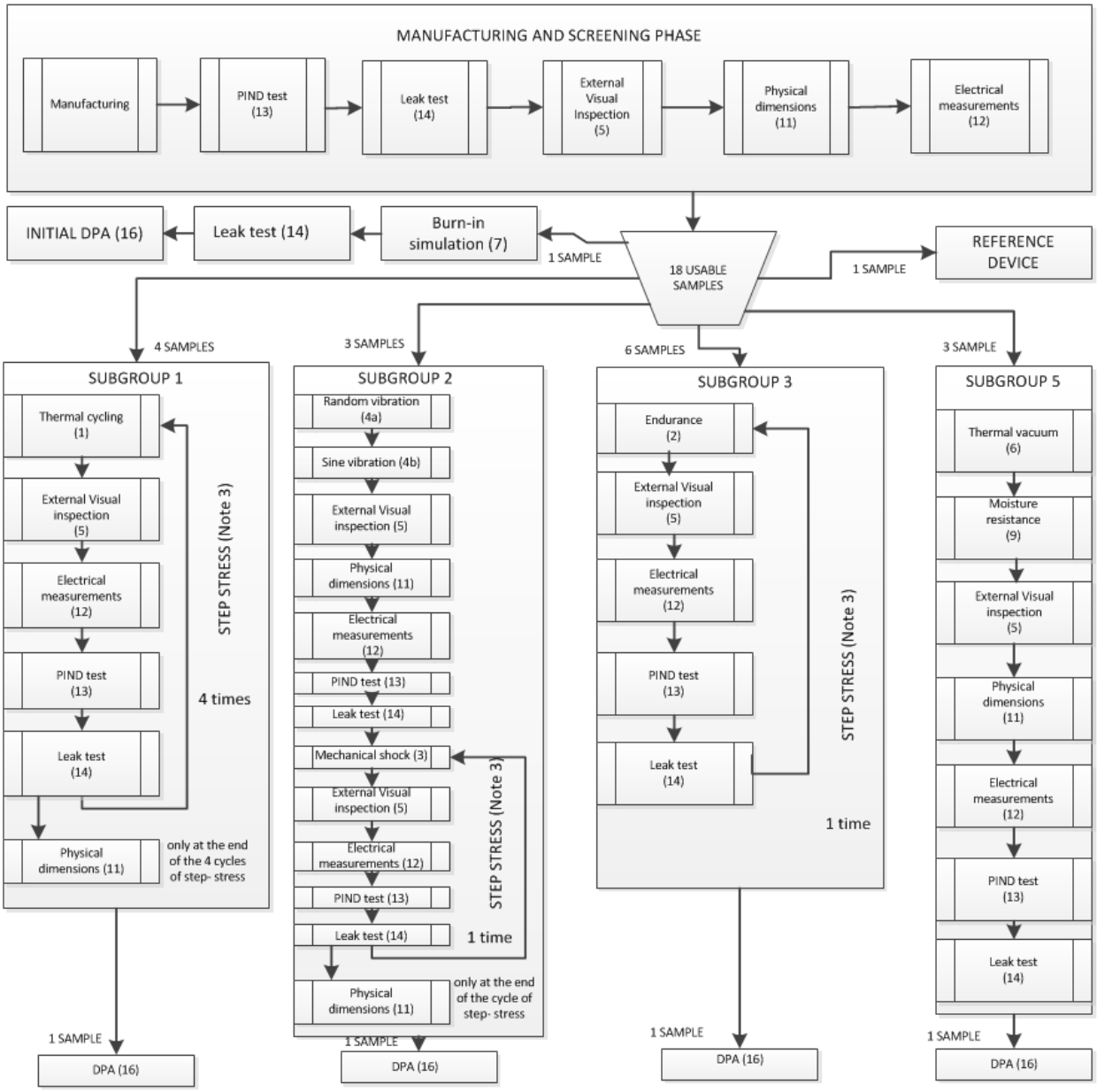


CHART 2.2. EVALUATION TEST PLAN FOR TEST STRUCTURES TVE2.



Note 0: The TVE1 technology/configuration drives the specific Evaluation Plan. The tailoring has to analyze the applicability (e.g. seal test is not applicable for just a substrate), and eventual replacement of a test (e.g. if solderability is not applicable, then it has to be replaced by other test e.g. bondability).

Note 1 : The hybrid manufacturer shall fabricate additional TVE1/TVE2 vehicles or define and fabricate specific test vehicles for evaluation of specific application (on/off or power cycling, high voltage, high current,…) and perform related specific tests including DPA.

Note 2: RGA is also used to verify hybrid hermeticity after ageing tests (O, Ar, He levels). For DPA in SG3 test 16e Internal Water Vapor Content requirement (max 5000ppm moisture) is not

applicable. The hybrids manufacturer can use the RGA measurements together with other observations (e.g. a current drift) to define its own requirements (e.g. hydrogen<300ppm) for later specifications (including TVCA in Chart 3).

Note 3: Step stressing requires the performance of each test in the loop for each step

7.4.4 Test methods and conditions

The test methods and conditions pertinent to TVE1 and TVE2 test plans are listed in following Table 2 together with the reference of the applicable specifications and each detail specification. The number of each test corresponds to that shown in brackets for each test in the evaluation test plans.

TABLE 2

N°	Test	MIL-STD	Method	Test conditions and remarks
1	Thermal cycling	883	1010	Condition B, 100 cycles per step up to 500 or failure
2a	Endurance	883	1005	Duration 1000h + 1000h. Ambient temperature will be defined to achieve 125°C≤T_j≤150°C (or maximum ratings). If the Tj of the most stressed part is lower than 125°C, the time shall be increased according to MIL-STD-883 Method 1005.
2b	High Temperature Storage	883	1008	Condition B: +125°C; 2000 hours
3	Mechanical shock	883	2002	Step1 : Condition B (1500g) for packages up to 1" x 2" and 1000 g 0,5 ms for packages above. Step 2 : Condition C (3000g) for packages up to 1" x 2" and Condition B (1500g) for packages above. Shocks performed on Y1, Y2, X and Z axes
4a	Random vibration	883	2026	Condition I K, Random Vibration 44.8 g RMS, 3 axis
4b	Sinusoidal vibration	883	2007	Condition B, 50 g
5	External Visual Inspection	883	2009	
6	Thermal vacuum			20 cycles -30 + 70 °C at ≤ 1mPa, dwell time : 2 hours, slope 2°C/minute
7	Burn-in simulation			Bake during 240 h at 125 °C, no voltage
8	Resistance to solvents	883	2015	ESCC 24800 may be used instead of the MIL Method
9	Moisture resistance	883	1004	10 V DC between all terminals connected together and package (+ on terminals)
10	Internal Visual inspection	883	2017	Class K requirements

N°	Test	MIL-STD	Method	Test conditions and remarks
11	Physical dimensions	883	2016	According to test vehicle detail specification. e.g. for TVE1 : line width, space, vias diameter, substrate camber,… e.g. for TVE2 : external dimensions, lid and package deformation,…
12	Electrical measurements			As per TVE2 specification
13	PIND test	883	2020	Condition A. Only applicable to cavity type devices
14	Leak test	883	1014	Fine leak : condition A Gross leak : condition C Only applicable to hermetically sealed, cavity type, devices
15	- None-			
16	DPA (initial or final)			Note 1, Note 2
16a	External Visual inspection	883	2009	
16b c	Radiography	883	2012	When soldered items or gold wires are present
16c	SAM inspection	883	2030	May be used in substitution of radiography
16d	Residual gas analysis	883	1018	
16e	Delidding	883	5009	Micromilling is allowed
16f	Internal visual inspection	883	2017	Class K
		883	2010	Condition A. Or ESCC equivalent for monolithic devices
		750	2072	
		750	2073	
		750	2074	
		883	2032	
16g	Dielectric strength	202	301	100 V DC between conductive layers in a multilayer system, between conductors on same layer in a monolayer system
16h	SEM Inspection	883	2018	Provide photos of typical assemblies, non conformances and anomalies
16i	Bond pull test	883	2011	On TVE2 only. Pull all wires and ribbons

N°	Test	MIL-STD	Method	Test conditions and remarks
16j	Die shear test	883	2019	On TVE2 only. Shear all chips and small substrates
16l	Substrate attach strength	883	2027	When shear test cannot be performed in case of substrates or large chips
16m	Adhesion test	-		Peeling test on metallization according to the hybrid manufacturer specification and agreed by ESCC executive
16n	Micro-sections	-		Micro-sectioning shall be performed to evaluate : multilayer substrates (conductors, dielectric, vias), assembly of added-on parts, cross-overs, local encapsulations, hermetic sealing (seal joint and feed-through).
17	Solderability	202	208	Three terminals per test item
18	Soldering heat	883	2036	Visual inspection (x 30 minimum) to verify that terminals, glass seals, connections or substrate are not damaged. Conditions as per test method to be defined according to application.
19	Terminal strength	883	2004	Flexible leads : condition A, F (N) = 30 x S (mm^2) (F : strength, S : lead section) Rigid feed-throughs in packages : • Diameter ≤ 1mm as above • Diameter > 1mm, condition C1, torque :1,5 N.cm

Note 1: the DPA (test number 16 in the table above) shall be performed by a laboratory mutually approved by the hybrid manufacturer and by the ESCC Executive.

Note 2: Initial DPA shall also contain Soldering Heat (test No. 18) prior to RGA (test No. 16e).

7.4.5 Evaluation Test Report

On completion of the evaluation testing, the manufacturer shall prepare an evaluation report. This report shall include:

- Description of the process capability domain technology tested: processes, materials and sub-techniques and how these were implemented in the devices tested.
- The Detail Specification for each Test Vehicle or circuit
- Production data for the test structures including details of any failures during production
- The evaluation test programme (ETP) giving details of all test methods and conditions and the number of test structures tested
- ETP detailed test results including: all electrical measurements and statistical analysis of the results, DPA reports, Failure Analysis reports (as applicable)
- Reference to the Manufacturer's alternative test data accepted as satisfying part or all of the ETP (as applicable)
- ETP summary and conclusions

The Evaluation report shall be sent to the ESCC Executive for review and acceptance.

8 PROCESS CAPABILITY APPROVAL (PCA) PHASE

8.1 GENERAL

The PCA phase of Hybrid Manufacturing Lines shall be as specified in ESCC Basic Specification 25600 with additional requirements set in the rest of this paragraph.

The objective of the Process Capability Approval Phase is to demonstrate, on the operational manufacturing line, the ability of the manufacturer to produce high reliability hybrids for space applications.

To this end the following prerequisites shall be satisfied:

- The Evaluation Phase has been completed successfully and the Capability Domain with its boundaries has been agreed between the Manufacturer and the ESCC Executive.
- The materials and processes and related specifications have been frozen in a PID agreed by the ESCC Executive
- The facilities and equipment and tools are operational and under control
- The training and certification of personnel is completed and surveyed
- All corrective actions derived from the manufacturer audit and line survey shall have been correctly and completely implemented
- An ESD control plan, meeting the minimum requirements of ESCC 24900, is frozen. Such control plan shall include provisions for the handling of Class 0 devices as per MIL-STD-883, Method 3015.

The ESCC Executive shall verify the completion of the prerequisites listed above at the time of the PCA readiness review.

8.2 PROCESS CAPABILITY APPROVAL TESTING

Process capability approval testing to be performed on test vehicles in accordance with the PID shall conform to ESCC 25600 and the rest of this paragraph.

This phase shall consist in the fabrication and testing of either test structures or actual circuit types covering the full technology domain defined in the PID.

The test vehicles used for PCA testing are called Test vehicles (TVCAs) in the rest of this document.

8.2.1 Definition and requirements for test vehicles for PCA testing

The capability approval test vehicles (TVCAs) shall be one or several functional products and additional test structures, if necessary, able to cover the capability domain boundaries defined in the PID.

For each TVCA:

- The Hybrid Technology Identification Form (HTIF) shall be established according to the format defined in Annex A of ECSS-Q-ST-60-05. The HTIF shall be checked against the Technology Domain boundaries defined in the PID.

- The Detail Specification has been written according to Annex B of ECSS-Q-ST-60-05 and agreed by the ESCC Executive.
- The capability approval test vehicles shall be manufactured in accordance with the PID and screened to Level 1 of ECSS-Q-ST-60-05.

In order to validate rework and repair procedures and limits, some of the TVCAs shall be intentionally reworked and repaired according to the methods described in the PID. At least one device per PCA test subgroup shall be reworked and/or repaired for that purpose.

The ESCC Executive shall be notified 3 weeks in advance of the following key points: Pre-cap Inspection and End of screening (for a review of screening results).

8.2.2 Hermetic Hybrids PCA test plans

8.2.2.1 General

The PCA programme of tests shall be reviewed and approved by the ESCC Executive prior to the start of the PCA testing.

The PCA test programme shall generally consist of the tests and subgroups given in Chart 3 of this specification. Samples to be submitted to Chart 3 shall be test structures as defined in Para. 8.2.1 of this specification and the PID. These test structures shall be randomly divided into the various test subgroups. Unless otherwise agreed with the ESCC Executive, when different types of test structure are being tested, each type shall be represented in each subgroup. In Chart 3, the numbers in brackets for each test correspond to the test number of Table 4 herein.

All TVCAs shall be serialized prior to testing. For each measurements or inspection performed, the results shall be recorded and summarized in terms of serial numbers and quantity tested, quantity passed and quantity rejected.

A reference device of each type of TVCA shall be kept for comparison purposes. Whenever electrical measurements are performed on any TVCA during PCA testing the reference device of the same type shall also be measured.

The manufacturer shall prepare and submit to the ESCC Executive a test plan specifying:

- The tests sub-groups (sequences, conditions, limits)
- The electrical measurement steps as per Detail Specification
- The inspection steps with related accept / reject criteria
- The sample size and the accept and reject criteria per sub-group
- The distribution of repaired hybrids per sub-group

8.2.2.2 Sample size

The following table defines the sample size and the accept/reject criteria per Subgroup (to be read together with Chart 3 under Para 8.2.2.3):

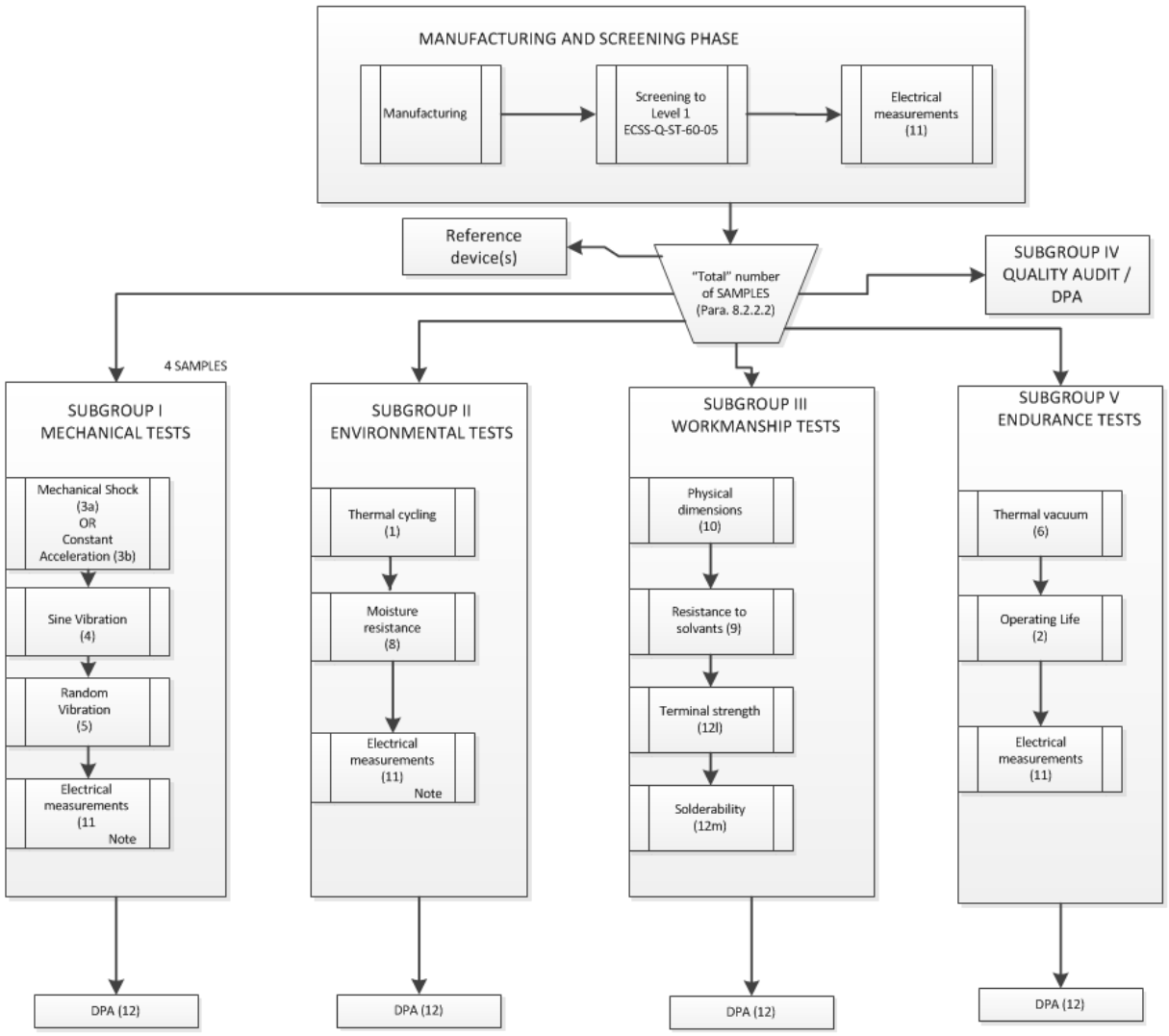
TABLE 3

No of TVCA *type*	***"N" TVCA's required per subgroup (Note 1)***					***Additional Samples***	***Total per type***	**TOTAL No**	***Accept/ reject criteria***
	SG I	SG II	SG III	SG IV	SG V				
	Mecha-nical tests	Thermal cycling	Workman-ship	QA/ DPA	Life Test	Reference device			
1	6	6	2	1	10	1	32	**32**	a=0, r≥1
2	3	3	1	1	5	1	17	**34**	a=0, r≥1
3	2	2	1	1	3	1	12	**36**	a=0, r≥1

NOTE 1: For large MCMs or complex hybrids, the sample size may be reduced provided that the design of TVCA include in them a statistically meaningful number of each subtechniques. A proposal of sample size shall be introduced in the PCA test plan to be submitted to ESCC Executive approval.

8.2.2.3 PCA test plan

CHART 3. PROCESS CAPABILITY APPROVAL TESTING OF TVCA TEST VEHICLES



NOTE: ONLY in the case of RF multi-cavity hybrids, the electrical measurements to be performed at the end of SUBGROUPS I and II shall be made in Thermal Vacuum (6)

8.2.3 Hermetic Hybrids PCA test methods and conditions

The test methods and conditions applicable to Chart 3 are listed in the following Table 4 together with the reference of the applicable specifications and each detail specification. The number of each test corresponds to that shown in brackets for each test in Chart 3.

The manufacturer's test procedures derived from the following table shall be submitted to the ESCC Executive for approval.

TABLE 4

N°	Test	MIL-STD	Method	Test conditions and remarks
1	Thermal cycling	883	1010	Condition B minimum, 100 cycles
2a	Operating life test	883	1005	Duration 1000h + 1000h. Ambient temperature will be defined to achieve 125°C≤T_j≤150°C (or maximum ratings). If the T_j of the most stressed part is lower than 125°C, the time shall be increased according to MIL-STD-883 Method 1005
2b	High Temperature Storage	883	1008	Condition B: +125°C; 2000 hours
3a	Mechanical shock	883	2002	Condition B for packages up to 1” x 2” 1000 g 0,5 ms for packages above. Shocks on Y1, plus shocks on Y2, Xand Z axes if required by the configuration.
3b	Constant acceleration	883	2001	Condition B for packages up to 1” x 1”. Y1 axis Condition A for packages above. Y1 axis, Y2 axis as needed Note : Constant acceleration is not applicable for packages > 1”x 2”
4	Sinusoidal Vibration	883	2007	Condition A, 20g
5	Random vibration	883	2026	Condition I F, Random Vibration 20 g RMS, 3 axes
6	Thermal vacuum			10 cycles -30 + 70 °C at ≤ 1mPa, dwell time : 2 hours, slope 2°C/mn The performance of this test under actual vacuum conditions may be waived by the ESCC Executive in cases where the approval domain includes only small hybrids.
7	Not used			
8	Moisture resistance	883	1004	Bias conditions shall be as agreed with the ESCC Executive in order to safeguard the integrity of the device.
9	Resistance to solvents	883	2015	ESCC may be used instead of the MIL Method
10	Physical dimensions			According to hybrid detail specification.
11	Electrical measurements			According to the hybrid detail specification. Note : Initial electrical measurements can be the final measurements performed after screening

N°	Test	MIL-STD	Method	Test conditions and remarks
12	DPA (initial or final)			DPA on 1 sample per SG Note 1
12a	External visual inspection	883	2009	
12b	Radiography	883	2012	If soldered items or gold wires are present
12c	SAM inspection	883	2030	May be used in substitution of radiography
12d	Seal test	883	1014	Fine leak : condition A Gross leak : condition C
12e	PIND test	883	2020	Condition A
12f	IResidual Gas Analysis	883	1018	The internal water vapour content requirement (maximum limit) is only for information after the Subgroup V “Endurance test” and Subgroup VI (HTS); in this case the RGA test is used as a verification of the hermeticity.
12g	Internal visual	883 883 750 750 750 883	2017 2010 2072 2073 2074 2032	Class K Condition A. Or ESCC equivalent for monolithic devices
12h	SEM Inspection	883	2018	Provide photos of typical assemblies, non conformances and anomalies
12i	Bond pull test	883	2011	Pull all wires and ribbons
12j	Die shear test	883	2019	Shear all chips and small substrates
12k	Substrate attach strength	883	2027	When shear test cannot be achieved for substrates or large chips
12l	Terminal strength	883	2004	Only for Subgroup III “Workmanship tests” Flexible leads : condition A, F (N) = 30 x S (mm^2) (F : strength, S : lead section) Rigid feed-throughs in packages :

N°	Test	MIL-STD	Method	Test conditions and remarks
				• Diameter ≤ 1mm as above • Diameter > 1mm, condition C1, torque :1,5 N.cm
12m	Solderability	202	208	Only for Subgroup III "Workmanship tests" Three terminals per test item.

Note 1: the DPA (test number 12 in the table above) shall be performed by a laboratory mutually approved by the hybrid manufacturer and by the ESCC Executive

8.2.4 PCA test report

On completion of the PCA testing, the manufacturer shall collect all test data and documentation in the form of a report. This report shall be sent to the ESCC Executive for review and acceptance.

The report shall contain the following information:

- Description of the process capability domain tested, including processes (including the associated equipment), materials and subtechniques and how these were implemented in the devices tested.
- The Specification for each test structure. The Detail Specification for each Test Vehicle or hybrid circuit type written according to Annex B of ECSS-Q-ST-60-05
- A description of the test vehicle(s) or actual hybrid type(s) used for approval testing in the form of the HTIF(s) according to Annex A of ECSS-Q-ST-60-05
- Production data for the test structures including details of any failures during production
- The PCA test programme giving details of all test methods and conditions and the number of test structures tested
- The Test Plans carried out for Capability Approval Testing with indication of the allowable number of failed devices per test file. The Test Methods and conditions used
- Detailed test results including: all electrical measurements and statistical analysis of the results, DPA reports, and any non-conformance reports
- Reference to the Manufacturer's alternative test data accepted as satisfying part or all of the PCA test programme (as applicable)
- PCA testing summary and conclusions

8.3 PROCEDURES SPECIFIC TO THE PCA OF HYBRID MANUFACTURING LINES

The following provisions, see Annex 2 for an overview, are specific to PCA of Hybrid Lines and supplement related requirements in ESCC 25600.

8.3.1 Manufacturing Line under TRB management

A manufacturing hybrid line can be under TRB management and SPC (Category 1 Option 2 of ECSS-Q-ST-60-05) only after having first achieved the PCA per this specification.

The migration to Category 1 Option 2 status shall be approved by the ESCC executive once a proper system is in place based on IPC-9191 and verified by ESCC executive or his expert delegate against IPC-9199.

8.3.2 Extension or change of the Process Capability Approval Domain

By a change of the Capability Approval Domain, it is intended to make an addition of, or change to, materials and/or processes and/or boundaries that were included in the previous PID.

The Extension of Capability Domain is a particular case of change.

Changes of the Capability Approval domain are categorized into two classifications:

- Major change (new materials, new processes, new production equipment, move of line location, new or modified inspection criteria, change of process parameters beyond PID limits)
- Minor change (addition of already-existing production equipment to the line, addition of a second supplier for an already-used material)

Upon application for change of the Capability Approval Domain by the manufacturer concerned, the ESCC Executive will decide whether the change is major or minor.

Changes shall be validated by test programmes according to the test plan reviewed and approved by the ESCC Executive.

As a minimum, major changes in the PID, as listed in Table 5, will be the object of Evaluation of test as defined in the table. A reduced testing may be used in case of minor changes. Inspection tests after environmental tests shall be adapted in accordance with the changes.

TABLE 5. TESTING REQUIREMENTS FOR MAJOR CHANGES

Major changes	Environmental tests Chart 2.1 and/or 2.2 and Table 2					
1. Change of substrate material	SG1	SG2	SG3			
2. Change of a) conductor b) resistor c) dielectric material deposite don substrate and/or change of deposit method	 SG1 SG1 SG1		 SG3 SG3 SG3			
3. Changes to substrate mask design that reduce nominal design dimensions, spacing or isolation or changes to electrical parameters of the deposited elements beyond the design limits	SG1		SG3			
4. Change of trimming method	SG1		SG3			
5. Increase in substrate fabrication multi-layer conductor levels, more than one level	SG1	SG2	SG3			
6. Change of attach material or of attachment method	SG1	SG2	SG3			
7. Increase in element attach area	SG1	SG2				
8. Change of wire bond method and or material	SG1	SG2	SG3			
9. Increase in substrate attach perimeter	SG1	SG2			SG5	
10. Change of package base material	SG1	SG2	SG3		SG5	
11. Change of seal method, seal material, lid base material	SG1	SG2			SG5	
12. Increase in package seal perimeter	SG1	SG2			SG5	
13. Increase in lead count per package type	SG1	SG2			SG5	
14. Change of element backside or topside finish material	SG1		SG3			
15. Change in package/lead finish	SG1	SG2		SG4	SG5	

NOTE 1: The test content and specification for each subgroup (SG) in Table 5 shall be consistent with Charts 2.1 and 2.2 as applicable:

SG1 = Thermal cycling

SG2 = Vibration / mechanical shock

SG3 = Life test

SG4 = Workmanship

SG5 = Thermal vacuum / moisture resistance

NOTE 2: SG3 test to be performed in the case of changes in package base material (Major change No. 10 in Table 5) when thermal performance differences may be expected due to changes in the thermal resistance of the materials.

8.3.3 Maintenance, suspension and withdrawal of the Process Capability Approval

8.3.3.1 Maintenance of process capability approval.

The maintenance of PCA can be achieved in two ways.

On one hand, the certification of PCA of hybrid manufacturing lines may be maintained by the successful repetition of the PCA test programme after a lapse period of 2 years.

On the other hand, Process Capability Approval may also be maintained by:

- The continuous production of devices according to the capability domain defined in the PID.
  At least two months prior to the expiry date of line approval, the manufacturer shall send a letter to the ESCC executive with the details of lots processed to ECSS-Q-ST-60-05.
  The letter will identify: lot numbers, delivered hybrids and numbers and a synthesis of failures during burn-in, environmental and life testing (LAT).
  If considered necessary, the ESCC executive may require further details or a repetition of some tests on suitable test vehicles.
- Or, if Hybrids have been manufactured and tested within the capability domain (including SEC, LAT, CTA, User LAT), and have a complexity covering the domain boundaries or part of them, these tests may suffice for the maintenance of PCA.

Modifications, additions or changes to the PID (domain), shall be submitted at the time of maintenance. Inclusion in the PID will be justified and supported by relevant Delta Qualifications.

The minimum requirement for capability approval is that, during the last 12-month lapse period, one lot of hybrids has been manufactured, screened and tested for lot acceptance in accordance with ECSS-Q-ST-60-05.

The ESCC Executive shall be provided with documented evidence that the lot in question has successfully passed the specified tests and inspections. The ESCC Executive shall be provided with DPA test reports on three hybrids successfully screened as part of the lot proposed to sustain the maintenance of PCA.This DPA exercise shall be consistent with requirements for DPA found at the end of PCA test as defined in this document.

Renewal of capability approval shall be valid either from the date on which:

1. The previous approval expired or,
2. The date on which lot acceptance testing was completed successfully if this date occurred more than 6 months prior to 1.

8.3.3.2 Suspension of process capability approval.

The ESCC executive reserves its right to suspend the approval status of a production line, or any part thereof, for the following reasons:

1. failure(s) which cannot be remedied within a period of 6 months
2. failures of more than two consecutive lots.
3. a complete stop in production at the space hybrid line for a period longer than 6 months

NOTE: Failures due to causes external to the PCA domain are not considered (e.g. Hybrid containing an ASIC failing due to its design).

In the event of 1. and / or 2. or 3., the manufacturer shall initiate any corrective action considered appropriate and, in order to achieve reinstatement of approval status, supply the ESCC Executive with evidence that the cause of failure has been eliminated.

During the suspension period, the line shall not be considered as approved and not be used for the production of high reliability circuits unless they serve for approval purposes.

8.3.3.3 Withdrawal of process capability approval

Process Capability Approval status shall be withdrawn by the ESCC Executive:

1. at the request of the manufacturer
2. in case of persistent non-conformances to the PID requirements

8.3.3.4 Renewal after lapse of process capability approval

Following the lapse of capability approval, a renewal of approval can be started within a period of 6 months. Provided the Manufacturer can demonstrate that the original evaluation of the capability domain is still valid, this renewal procedure shall comprise a destructive physical analysis of sample hybrids, a manufacturer audit and a survey of test records generated in the lapse period. If this survey shows that the Manufacturer's data, equivalent to either PCA testing or Lot Acceptance Testing are available and acceptable, the ESCC Executive may take such data into consideration for renewal of the process capability approval. Where such data is not available or not acceptable, the testing of a number of components to the requirements of ECSS-Q-ST-60-05 will be required for the renewal.

Failure to satisfy the requirements regarding the validity of the original evaluation of a capability domain will necessitate a completely new process capability approval.

9 ANNEX 1 REQUIREMENTS GUIDELINES FOR THE MATERIALS AND PROCESSES DESCRIPTION

The manufacturer shall describe the type of functions / products which are planned to be developed and manufactured within the perimeter of the process capability domain under approval. Such description shall include basic electrical characteristics as pertinent. For the purpose of fabricating these types of products, the manufacturer shall define the extent of his capability domain for which approval is sought in terms of construction technologies also called sub-techniques (type of substrates, components mounting and interconnection techniques, encapsulation,…) and their associated boundaries.

The manufacturer shall describe the procedures for selection, procurement and control of materials used for production of structures within the process capability domain.

The manufacturer shall describe the processes within the process capability domain. He shall also give reference to the documents specifying the processes. At least the following areas shall be covered including a statement on the equipment used:

- Substrate and carrier preparation
- Conductor, termination and wire bonding process
- Thick film, thin film circuit processes
- Package assembly and encapsulation processes
- Rework procedures

9.1 DEFINITION OF PROPOSED SUB-TECHNIQUES IN THE PCA DOMAIN

The different sub-techniques are defined by:

- The materials (composition, designation, manufacturer)
- The processes (process owner- if subcontracted)
- The associated limits in terms of Dimensions and density of integration

The definition of the sub-techniques within a process capability domain depends on the substrate technology involved (e.g. thick film) and the related needs for assembly and encapsulation. It is specified in the following paragraphs.

9.1.1 Definition of sub-techniques depending on the substrate technology

This paragraph lists some substrate technologies and the applicable requirements, in each case, for the appropriate definition of the related necessary sub-techniques.

9.1.1.1 Screen Printed Thick film

Substrate(s)

- Composition, designation, manufacturer
- Surface characteristics (as fired…)
- Minimum/maximum size, thicknesses, shape…
- Cutting method
- Holes drilling method, dimensions and number per square unit

Conductive ink(s)

- Composition, designation, manufacturer, application (conductive layer, via filling, holes/edges metallization, …)
- Minimum track width/space for different layers (if applicable), thickness
- Resistivity, current density
- Maximum number of layers
- Minimum vias/holes dimensions

Dielectric ink(s)

- Composition, designation, manufacturer, application (multi layer, cross over, overglaze, capacitor dielectric, …)
- Thickness
- Maximum number of layers
- Number of printings per layer
- Withstanding voltage, insulation resistance

Resistive ink(s)

- Composition, designation, manufacturer, application (printed on dielectric or directly on the bare substrate, …)
- Associated specific conductive ink used as resistor terminations (if applicable)
- Resistivity range (ohm/square), TCR, long term stability, power rating
- Blending of resistor inks (if applicable)
- Minimum dimensions
- Minimum/maximum number of squares
- Trimming methods

9.1.1.2 Thin film deposition

Substrates

- Composition, designation, manufacturer
- Surface characteristics (as fired, lapped and polished…)
- Minimum/maximum size, thicknesses, shape…
- Cutting method
- Holes drilling method, dimensions and number per square unit

Metallization(s): resistive, barrier, conductive layer

- Deposition and etching method
- Composition, target designation and manufacturer
- Minimum track width/space, thicknesses
- Resistivity, current density for conductive layer
- Resistivity range (ohm/square), TCR, long term stability, power rating for resistive layer
- Conductive layer over-plating (if any)
- Resistor trimming methods
- Holes metallization method (if any)

Dielectric layer

- Composition, designation, manufacturer, application (multi layer, cross over, overglaze, capacitor dielectric, …)
- Deposition and etching method
- Thickness
- Maximum number of layers
- Withstanding voltage, insulation resistance

9.1.1.3 HTCC (High Temperature Cofired Ceramic)

- Manufacturer
- Ceramic type (Al2O3, AlN), composition
- Minimum/maximum size and thickness, shape, …
- Minimum dimensions of punched via holes
- Maximum number of layers
- Maximum numbers of green tapes per layer
- Typical shrinkage (after firing)
- Minimum dielectric thickness as fired
- Withstanding voltage, insulation resistance
- Conductor (internal and external)
  - Composition
  - Minimum track width/space, thickness
  - Resistivity, current density
- External conductor plating
  - Plating method
  - Composition
  - Different layers and thicknesses
- Brazed elements (carrier, frame, leadframe,…)
  - Element function (thermal dissipation, hermetic cavity, interconnection, mechanical carrier, …)
  - Element composition (raw material and plating)
  - Maximum dimensions, thickness
  - Attachment medium composition

9.1.1.4 LTCC (Low Temperature Co-fired Ceramic)

- Tape material, designation, manufacturer
- Minimum/maximum size, thicknesses after firing
- Minimum dimensions of punched via holes
- Maximum number of layers
- Typical shrinkage (after firing)
- Minimum dielectric thickness as fired
- Withstanding voltage, insulation resistance
- Conductive ink(s) (internal and external)
  - Composition, designation, manufacturer, application (conductive layer, via filling, holes/edges metallization, …)
  - Minimum track width/space, thickness
  - Resistivity, current density
- Resistive ink(s)
  - Composition, designation, manufacturer

- Resistivity range (ohm/square), TCR, long term stability, power rating
- Blending of resistor inks (if applicable)
- Minimum dimensions
- Minimum/maximum number of squares
- Trimming methods

- Substrate cutting method
- Holes drilling method, dimensions and number per square unit
- Brazed elements (carrier, frame, leadframe,…)
  - Element function (thermal dissipation, hermetic cavity, interconnection, mechanical carrier, …)
  - Element composition (raw material and plating)
  - Maximum dimensions, thickness
  - Attachment medium composition

9.1.1.5 Organic substrate(s)

- Substrate manufacturer
- Raw material: designation, manufacturer
- External maximum dimensions, total thickness
- Maximum number of layers
- Conductors (internal and external)
  - Composition
  - Minimum track width/space and thickness for internal and external layers
  - Minimum dimensions of via holes
  - Resistivity, current density
  - External conductor plating
    - Types
    - Thicknesses
- Embedded passives

9.1.1.6 DBC (Direct Bonded Copper)

- Manufacturer
- Ceramic type (Al2O3, AlN), composition
  - Minimum/maximum size and thickness, shape, …
  - Minimum/maximum dimensions of via holes
  - Minimum/maximum dimensions of plaggged holes
  - Minimum track width/space, thickness
  - Minimum width and maximum length of flying leads
- Withstanding voltage, insulation resistance
- Conductor plating
  - Plating method
  - Composition
  - Different layers and thicknesses
- Brazed elements (carrier, frame, leadframe,…)
  - Element function (thermal dissipation, hermetic cavity, interconnection, mechanical carrier, …)
  - Element composition (raw material and plating)
  - Maximum dimensions, thickness
  - Attachment medium composition

9.1.2 Assembly of added-on components, substrates and carriers

9.1.2.1 Passive components assembly

- Type (resistor, capacitor, inductance, …)
  - Packaging (chip, package type, …)
    - Materials
      - Substrate (silicon, ceramic,…)
      - passive part material (NiCr, Ta2N, …)
      - Interconnecting metallization (Ni/Au, Ag/Pd, …)
    - Minimum/maximum dimensions

- Attachment medium
  - Mechanical
    - Material
      - Type (non conductive adhesive, solder, …)
      - Thickness
    - Process (dispensing, preform reflow,…)
  - Electrical
    - Material
      - Type (conductive adhesive, solder, wires, ribbons, …)
      - Dimensions (diameter, thickness, width)
    - Process (dispensing, preform reflow, wire bonding, …)

- Attachment substrate
  - Composition (thick film main substrate or carrier, package base, …)
  - Material
    - Raw material (alumina, Kovar, …)
    - Metallization (thick film gold pad, Ni/Au, …)

9.1.2.2 Active components assembly

- Type of active components
  - Type (diode, transistor, integrated circuit, …)
  - Packaging (bare chip, beam lead, flip chip, package type, …)
    - Materials
      - Silicon, Gallium Arsenide,…
      - Interconnecting metallization (Al, Au…)
    - Minimum/maximum dimensions
  - Attachment medium
    - Mechanical
      - Material
        - Type (non conductive adhesive, solder, …)
        - Thickness
      - Process (dispensing, preform reflow,…)
    - Electrical
      - Material
        - Type (conductive adhesive, solder, wires, ribbons, …)
        - Dimensions (diameter, thickness, width)
      - Process (dispensing, preform reflow, wire bonding, …)

- Attachment substrate
  - Composition (Thick film main substrate or carrier, package base, …)
  - Material
    - Raw material (alumina, Kovar, Cu/W, …)
    - Metallization (thick film gold pad, Ni/Au, …)

- Wire/ribbon bonding
  - Material
    - Composition
    - Dimensions
  - Process (Thermocompression, thermosonic, ultrasonic, parallel gap,…)

9.1.2.3 Substrate and carrier assembly

- Substrate assembly
  - Material (adhesive, solder, …)
  - Process (preform curing, reflow,…)
  - Details of package base to which the substrate is attached
    - Composition
    - Metallization

  - Interconnection substrate/package
    - Material
    - Process

- Carrier assembly
  - Material (adhesive, solder,…)
  - Process (preform curing, reflow,…)
  - Details of main substrate or package base
    - Composition
    - Metallization

  - Interconnection carrier/main substrate or carrier/package base
    - Material
    - Process

9.1.3 Encapsulation

9.1.3.1 Hermetic packaging

- Package technology (metallic with glass or ceramic feed-throughs, HTCC or LTCC without or with interconnection in the package base (ISP), …)
- Application (low power, high power, LF, RF, …)
- Package manufacturer
- Body
  - Base
    - Material
    - Minimum/maximum dimensions
    - Plating (composition, thicknesses,…)

  - Wall/frame
    - Material
    - Minimum/maximum dimensions
    - Plating (composition, thicknesses, …)

- Base/frame attachment
  - Attachment medium
  - Process

- Feedthroughs
  - Material

    - Dielectric (glass, ceramic, …)
    - Conductor (metal, ink, …)
  - Dimensions
  - Sealing technology (matched seal, …)

- Leads
  - Material
  - Dimensions
  - Plating (composition, process, thicknesses, …)
  - Number and pitch
  - Leads to package attachment
  - Attachment medium (Au/Sn, Ag/Cu,…)
  - Process

- Lid
  - Material
  - Lid manufacturer
  - Minimum/maximum dimensions
  - Thickness and design
  - Plating (composition, process, thicknesses,…)

- Sealing
  - Process (parallel seam welding, laser,…)
  - Sealing atmosphere
  - Getter/absorber

10 ANNEX 2 - OVERVIEW OF THE PCA EXTENSION APPLICATION