INTEGRATED CIRCUITS:
MONOLITHIC AND MULTICHIP MICROCIRCUITS,
WIRE-BONDED, HERMETICALLY SEALED
AND
FLIP-CHIP MONOLITHIC MICROCIRCUITS,
SOLDER BALL BONDED, HERMETICALLY AND
NON-HERMETICALLY SEALED
AND
DIE

ESCC Generic Specification No. 9000

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DCR No.	CHANGE DESCRIPTION
1134	Specification upissued to incorporate changes per DCR.

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1 INTRODUCTION

1.1 SCOPE

This specification defines the general requirements for the qualification, qualification maintenance, procurement, and delivery of Integrated Circuits for space applications as follows:

- Monolithic and Multichip Microcircuits, wire-bonded, hermetically sealed packaged components
- Flip-chip Monolithic Microcircuits, solder ball bonded, hermetically and non-hermetically sealed packaged components with and without passive (i.e. capacitors and resistors) Add-on Components
- Monolithic Microcircuit die components

This specification contains the appropriate inspection and test schedules and also specifies the data documentation requirements.

1.2 APPLICABILITY

This specification is primarily applicable to the granting of qualification approval to components qualified in accordance with one of the following ESCC methods:

(a) Qualification of Standard Components per this ESCC Generic Specification and ESCC Basic Specification No. 20100.

(b) Qualification of a component within an approved capability domain per ESCC Basic Specification No. 24300.

(c) Technology Flow Qualification per ESCC Basic Specification No. 25400.

It is also primarily applicable to the procurement of components so qualified.

This specification may also be applied to the procurement of unqualified components, recommendations for which are given in ESCC Basic Specification No. 23100.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect on the date of starting qualification or placing the Purchase Order.

2.1 ESCC SPECIFICATIONS

- No. 20100, Requirements for the Qualification of Standard Electronic Components for Space Application.
- No. 20200, Component Manufacturer Evaluation.
- No. 2029000, Checklist for Monolithic Microcircuit Manufacturer and Line Survey.
- No. 20400, Internal Visual Inspection.
- No. 20500, External Visual Inspection.
- No. 20600, Preservation, Packaging and Dispatch of ESCC Components.
- No. 21001, Destructive Physical Analysis of EEE Components.
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 21400, Scanning Electron Microscope Inspection of Semiconductor Dice.
- No. 21700, General Requirements for the Marking of ESCC Components.

- No. 22600, Requirements for the Evaluation of Standard Electronic Components for Space Application.
- No. 2269000, Evaluation Test Programme for Integrated Circuits: Monolithic and Multichip Microcircuits, Wire-Bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits, Solder Ball Bonded, Hermetically and Non-Hermetically Sealed.
- No. 22800, ESCC Non-Conformance Control System.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23100, Recommendations on the use of the ESCC Specification System for the Evaluation and Procurement of Unqualified Components.
- No. 23500, Lead Materials and Finishes for Components for Space Application.
- No. 23800, Electrostatic Discharge Sensitivity Test Method.
- No. 24300, Requirements for the Capability Approval of Electronic Component Technologies for Space Application.
- No. 24600, Minimum Quality System Requirements.
- No. 24800, Resistance to Solvents of Marking, Materials and Finishes.
- No. 25100, Single Event Effects Test Method and Guidelines
- No. 25400, Requirements for the Technology Flow Qualification of Electronic Components for Space Application.
- REP005, Qualified Parts List.
- REP006, Qualified Manufacturers List

For qualification and qualification maintenance or procurement of qualified components, with the exception of ESCC Basic Specifications Nos. 20100, 21700, 22800, 24300, 24600 and 25400, where Manufacturers' specifications are equivalent to, or more stringent than, the ESCC Basic Specifications listed above, they may be used in place of the latter, subject to the approval of the ESCC Executive. Such replacements shall be clearly identified in the applicable Process Identification Document (PID).

For procurement of unqualified components, where Manufacturers' specifications are equivalent to or more stringent than the ESCC Basic Specifications listed above, they may be used in place of the latter subject to the approval of the Orderer.

Such replacements may be listed in an appendix to the appropriate Detail Specification at the request of the Manufacturer or Orderer, subject to the approval of the ESCC Executive.

Unless otherwise stated herein, references within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

- ECSS-Q-ST-70-08, Space Product Assurance: Manual soldering of high-reliability electrical connections
- ECSS-Q-ST-70-38, Space Product Assurance: High-Reliability Soldering for Surface-Mount and Mixed Technology
- J-STD-020, IPC/Jedec Standard for Moisture/Reflow Sensitivity Classification for Non-Hermetic Surface-Mount Devices.
- JESD22-A118, EIA/Jedec Standard Test Method: Accelerated Moisture Resistance - Unbiased HAST.

- JESD22-B117, EIA/Jedec Standard Test Method: Solder Ball Shear.
- JEP001, Jedec Publication for Foundry Process Qualification Guidelines
- MIL-STD-883, Test Methods and Procedures for Micro-electronics.

2.3 ORDER OF PRECEDENCE

For the purpose of interpretation and in case of conflict with regard to documentation, the following order of precedence shall apply:

(a) ESCC Detail Specification.
(b) ESCC Generic Specification.
(c) ESCC Basic Specification.
(d) Other documents, if referenced herein.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following shall apply:

- Integrated Circuit (Microcircuit): A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function. Monolithic Microcircuits and Multichip Microcircuits are considered as Integrated Circuits.
- Monolithic Microcircuit: A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate (with a single semiconductor die).
- Multichip Microcircuit: A microcircuit consisting of two or more semiconductor dice coming from the same manufacturer, from one or more foundries, individually attached to a single package cavity.
- Wire-bonded Integrated Circuit: A monolithic or multichip microcircuit with the die (dice) backside(s) bonded to the package cavity or substrate, and wire-bonded to the package leads.
- Flip-chip Integrated Circuit: A monolithic microcircuit with solder balls attached to the active side of the die, connected top side down to a substrate, with or without underfill.
- Hermetic Package: A component encapsulation which by design and construction is able to pass a seal test.
- Non-Hermetic Package: A component encapsulation which by design or construction is unable to pass a seal test.
- Add-on Components: Capacitors and/or resistors mounted in and electrically connected to a Flip-chip Integrated Circuit assembly. Other component types are not permitted.
- Packaged Component: A monolithic or multichip microcircuit designed to be delivered after encapsulation (for Wire-bonded Integrated Circuits) or connected to a substrate (for Flip-chip Integrated Circuits).
- Die Component: A monolithic microcircuit designed to be delivered without encapsulation

4 REQUIREMENTS

4.1 GENERAL

Unless otherwise specified, the requirements for the qualification of a component shall be in accordance with ESCC Basic Specification No. 20100. Specifically for Wire-bonded Integrated Circuits, the requirements of Para. 4.2.1 shall also apply.

The requirements for approval of a capability domain and the qualification of a component (type approval testing) within an approved domain shall be in accordance with ESCC Basic Specification No. 24300.

The requirements for Technology Flow Qualification and the listing of qualified component types shall be in accordance with ESCC Basic Specification No. 25400.

The test requirements for procurement of both qualified and unqualified Packaged Components (see Chart F1A) shall comprise:

- Wafer Lot Acceptance with, if stipulated in the Purchase Order, total dose radiation testing.
- Special In-Process Controls.
- Screening Tests.
- Periodic Testing (for qualified components only).
- Lot Validation Testing if stipulated in the Purchase Order.

The test requirements for procurement of both qualified and unqualified Die Components (See Chart F1B) shall comprise:

- Wafer Lot Acceptance with, if stipulated in the Purchase Order, total dose radiation testing.
- Special In-Process Controls (on Packaged Test Sublot samples).
- Screening Tests (on Packaged Test Sublot samples).
- Periodic Testing (for qualified components only; on Packaged Test Sublot samples).
- Lot Validation Testing if stipulated in the Purchase Order (on Packaged Test Sublot samples).

4.1.1 Specifications

For qualification, qualification maintenance, procurement and delivery of components in conformity with this specification, the applicable specifications listed in Section 2 of this document shall apply in total unless otherwise specified herein or in the Detail Specification.

4.1.2 Conditions and Methods of Test

The conditions and methods of test shall be in accordance with this specification, the ESCC Basic Specifications referenced herein and the Detail Specification.

4.1.3 Manufacturer's Responsibility for Performance of Tests and Inspections

The Manufacturer shall be responsible for the performance of tests and inspections required by the applicable specifications. These tests and inspections shall be performed at the plant of the Manufacturer of the components unless it is agreed by the ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified components), to use an approved external facility.

4.1.4 Inspection Rights

The ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified components if stipulated in the Purchase Order) reserves the right to monitor any of the tests and inspections scheduled in the applicable specifications.

4.1.5 Customer Source Inspections

4.1.5.1 Pre-Encapsulation Customer Source Inspection

If stipulated in the Purchase Order, the Orderer may perform a source inspection at the Manufacturer's facility prior to encapsulation (e.g. perform Internal Visual Inspection, witness of Bond Pull and Die Shear). Details of the inspections to be performed or witnessed and the required period of notification shall be as stipulated in the Purchase Order.

For Flip-Chip Integrated Circuit components, the inspection may be performed on piece parts prior to or after die to substrate attachment unless otherwise stated in the Detail Specification.

4.1.5.2 Final Customer Source Inspection

If stipulated in the Purchase Order, the Orderer may perform a source inspection at the Manufacturer's facility prior to delivery at an appropriate point during testing that has been agreed with the Manufacturer (e.g. perform Die Visual Inspection for Die Components; witness of final Room Temperature Electrical Measurements; performance of External Visual Inspection and Dimension Check; review of the data documentation package). Details of the inspections to be performed or witnessed and the required period of notification shall be as stipulated in the Purchase Order.

4.2 QUALIFICATION AND QUALIFICATION MAINTENANCE REQUIREMENTS ON A MANUFACTURER

To obtain and maintain the qualification of a component, or family of components, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 20100, except as amended in Para. 4.2.1.

To obtain and maintain the qualification of a component in a capability approved domain, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 24300.

To obtain and maintain the qualification of a component produced using a qualified Technology Flow, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 25400.

4.2.1 Single Phase Qualification (SPQ)

Exclusively for qualification of Wire-bonded Integrated Circuits, the separate, detailed evaluation phase of ESCC Basic Specification No. 20100 shall not be performed. Instead, additional assessment activities, to be performed by the Manufacturer, and supervised by and agreed with the ESCC Executive, shall be included as an initial stage in the process of achieving qualification. This approach is described in Chart F0 and detailed below:

(a) Manufacturer Assessment

The Manufacturer shall provide the following information for the component(s) being qualified, to the ESCC Executive for review:

- A detailed conformance matrix to the general requirements for qualification included in ESCC Basic Specification No. 20100.
- Information explicitly indicating full details on the compliance, or otherwise, of the Manufacturer's quality management system to the requirements of ESCC Basic Specification No. 24600.
- A completed ESCC Manufacturer Checklist in accordance with ESCC Basic Specification Nos. 20200 and 2029000
- The draft Process Identification Document (PID).
- A draft ESCC Detail Specification

(b) Component Assessment

The Manufacturer shall provide to the ESCC Executive sufficient information to enable the full assessment of the suitability of the component(s) being qualified under the following criteria:

- design margins
- constituent materials
- construction
- characterisation and performance over the full operating and storage temperature ranges
- radiation performance
- intrinsic reliability

Specific requirements, to be addressed for the component(s) being qualified, shall include the following (the relevant requirements specified in ESCC Basic Specification Nos. 22600 and 2269000 may be used for guidance):

i. Wafer Level Reliability Assessment

This assessment shall address potential failure mechanisms and mitigation strategies, calculation/evaluation of activation energy and acceleration factors for voltage and temperature, and the establishment of long term reliability failure rates.

The information gained during the determination of failure mechanisms and activation energy shall be used to determine appropriate life test conditions that would verify the goal of 18 years satisfactory operating life at $T_j \leq +110°C$ (see MIL-STD-883, Test Method 1016 for guidance). The Manufacturer shall determine worst case characteristics for the component (JEP001 may be used as a guideline).

ii. Component Reliability Assessment

Suitable information shall be provided to demonstrate that the goal of 18 years satisfactory operating life at $T_j \leq +110°C$ is also met at the component level.

If no suitable data are available, the 2000 hours Operating Life test to be performed during qualification testing, in accordance with Chart F4A, shall be extended to a minimum of 4000 hours at $T_{amb} = +125°C$. The remaining Operating Life test conditions shall be in accordance with Para. 8.25.

iii. Construction Analysis

Construction analysis shall be performed on a minimum of 3 samples. The content and extent of the construction analysis shall be agreed with the ESCC Executive. ESCC Basic Specification No. 21001 may be used as a guideline.

iv. Electrical Characterisation

Suitable information on the following specific electrical characterisation details for the component(s) over the full operating temperature shall be provided (as applicable):

- Electrostatic Discharge Sensitivity
- Safe Operating Area
- Current Limits
- Breakdown Voltage, Input or Output
- Input Interaction
- Thermal resistance
- Verification of Functionality

v. Radiation Assessment
Suitable information on the ability of the component(s) to withstand the space radiation environment in line with the requirements of ESCC Basic Specification Nos. 22900 and 25100 (as applicable) shall be provided.

vi. Package Assessment
Suitable information on the following specific package assessment details for the component(s) shall be provided (as applicable):

- Assessment of the component(s) capability to withstand typical mounting in accordance with ECSS-Q-ST-70-08 and/or ECSS-Q-ST-70-38
- Lid Torque or Lid Pull
- Resistance to Soldering Heat
- Pin-to-Pin Isolation
- Thermal Resistance Characterisation
- The ability to withstand thermal cycling and thermal shock
- The ability to withstand environmental loads as vibration and mechanical shock

NOTE:
For SPQ, the number of components selected for component assessment testing will depend on whether a single component type or a family of components is being assessed, the number of component types chosen to represent the family, and the availability of appropriate, suitable information. The component types chosen to represent a family shall cover the range of components to be qualified and shall be representative of the different package and pin configurations. They shall also be the most suitable for highlighting those characteristics and parameters that are pertinent to an investigation into failure modes and weaknesses. These test samples shall be as specified by or agreed with the ESCC Executive.

The verification of the completeness and adequacy of data related to the preliminary additional assessment, will be performed by the ESCC Executive as part of a Manufacturer Data Review, to be conducted in accordance with ESCC Basic Specification Nos. 20200 and 2029000, and this specification.

Subject to the ESCC Executive verifying the adequacy and completeness of the additional assessment information in (a) and (b) above, as presented by the Manufacturer during the Manufacturer Data Review, this initial stage of SPQ will be considered completed. The draft ESCC Detail Specification and PID shall be revised as necessary and frozen pending completion of qualification testing. SPQ shall continue in line with the requirements of the Qualification Testing Phase as detailed in ESCC Basic Specification No. 20100 and Chart F4A of this specification.

4.3 DELIVERABLE COMPONENTS

4.3.1 ESCC Qualified Components

Components delivered to this specification shall be processed and inspected in accordance with the relevant Process Identification Document (PID).

4.3.2 ESCC Components

Each component, irrespective of qualification status, identified with an ESCC component number and delivered to this specification shall:

- be traceable. Each Packaged Component shall be traceable to its production lot. Each Die Component shall be traceable to its wafer lot.
- have satisfactorily completed all the tests required by the relevant issues of the applicable specifications.
- be produced from lots that are considered by the Manufacturer to be capable of passing all applicable tests, and sequences of tests, that are defined in Chart F4A or F4B (as applicable). The Manufacturer shall not knowingly supply components that cannot meet this requirement. In the event that, subsequent to delivery and prior to operational use, a component is found to be in a condition such that, demonstrably, it could not have passed these tests at the time of manufacture, this shall be grounds for rejection of the delivered lot.

4.3.3 Lot Failure

Lot failure may occur during Wafer Lot Acceptance (Charts F2A and F2B), Special In-Process Controls (Charts F2A and F2B), Screening Tests (Charts F3A and F3B), or Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B).

Should such failure occur during qualification, qualification maintenance or procurement of qualified components the Manufacturer shall initiate the non-conformance procedure in accordance with ESCC Basic Specification No. 22800. The Manufacturer shall notify the Orderer and the ESCC Executive by any appropriate written means, within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing or analysis shall be performed on the failed components until so instructed by the ESCC Executive.

Should such failure occur during procurement of unqualified components the Manufacturer shall notify the Orderer by any appropriate written means within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing or analysis shall be performed on the failed components until so instructed by the Orderer. The Orderer shall inform the Manufacturer within 5 working days of receipt of notification what action shall be taken.

4.4 MARKING

All components procured and delivered to this specification shall be marked in accordance with ESCC Basic Specification No. 21700.

For Die Components, the specified marking shall not be marked on the component but shall accompany the component, in full, in its primary package. For Die Components, lot identification shall also include wafer lot numbers.

4.5 CONSTRUCTION, MATERIALS AND FINISHES

Specific requirements for materials and finishes are specified in the Detail Specification. Where a definite material or finish is not specified a material or finish shall be used so as to ensure that the component meets the performance requirements of this specification and the Detail Specification. Acceptance or approval of any constituent material or finish does not guarantee acceptance of the finished product.

For Wire-bonded Integrated Circuit components, unless otherwise specified in the Detail Specification, the component shall be hermetically sealed and shall have a metal body with hard glass seal or a ceramic body. The component case lid shall be welded, brazed, preform soldered or glass frit sealed.

For Flip-chip Integrated Circuit components, the component shall have a ceramic body with either a Hermetic or Non-Hermetic Package as specified in the Detail Specification. For Flip-chip Integrated Circuit components with Hermetic Packages, the case lid shall be welded, brazed, preform soldered or glass frit sealed. For Flip-chip Integrated Circuit components with Non-Hermetic Packages, the encapsulation shall be without cavity.

For Die Components, see Para. 4.8 for the minimum material requirements that shall be specified in the Detail Specification.

All materials and finishes of the components specified in the Detail Specification shall comply with the restrictions on materials specified in ESCC Basic Specification No. 22600.

4.6 ADD-ON COMPONENTS AND MATERIALS REQUIREMENTS

Only applicable to Flip-chip Integrated Circuit components.

All Add-on Components (capacitors and resistors only) and materials incorporated into deliverable components shall be procured as traceable homogeneous lots.

For qualified Flip-chip Integrated Circuit components, the PID shall include a list of Add-on Components and materials which have been successfully tested according to the requirements of this specification and approved for their inclusion in the PID by the ESCC Executive.

For qualified Flip-chip Integrated Circuit components, Add-on Components shall either have been successfully evaluated per ESCC Basic Specification No. 2269000 as approved in the PID, or be ESCC Qualified as evidenced by a listing in the current ESCC Qualified Parts List REP005 or ESCC Qualified Manufacturers List REP006.

Documentation requirements for Add-on Components shall be as specified in Para. 9.7.

4.7 RADIATION TESTING

For qualification or qualification maintenance total dose radiation testing shall be performed when specified in the Detail Specification to the specified total dose level.

For procurement, as stipulated in the Purchase Order, total dose radiation testing shall be performed to the total dose level specified in the Detail Specification or to an alternate level if so stipulated in the Purchase Order.

The qualification status of the procured components shall not be impacted by any change to the total dose level applied.

For procurement, any lot of components that fails the specified total dose radiation test level may be accepted to a lower level of radiation subject to satisfactory test results at the lower level. In this case the total dose radiation level letter for the lot shall be modified accordingly.

4.8 DIE COMPONENTS

For Die Components, the Detail Specification shall, as a minimum, specify the following:

(a) Materials:
- Die substrate material
- Glassivation material
- Top metallisation material
- Backside metallisation material (if applicable)

(b) Terminal Identification and the applicable bias details for:
- All bonding pads
- Die substrate/backside contact

(c) Dimensions:
- Die length, width and thickness
- Glassivation thickness
- Top metallisation thickness
- Backside metallisation thickness (if applicable)
- Die topography details including all bonding pad dimensions

5 PRODUCTION CONTROL

5.1 GENERAL

Unless otherwise specified herein or in the Detail Specification, all lots of components used for qualification and qualification maintenance, Lot Validation Testing and for delivery shall be subject to tests and inspections in accordance with Chart F2A for Packaged Components and Chart F2B for Die Components, in the sequence shown. Any components which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The test requirements for Packaged Components are detailed in the paragraphs referenced in Chart F2A, as applicable and as indicated.

The test requirements for Die Components are detailed in the paragraphs referenced in Chart F2B, as applicable and as indicated.

For qualified components, the full production control provisions are defined in the PID.

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.3.

5.1.1 Rework and Repair

Any rework or repair procedures shall be agreed with the ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified components).

For qualified components, all rework and repair processes shall have been fully specified, documented and qualified by the manufacturer, and shall be listed in the PID.

Unless otherwise specified, the following specific rework and repair requirements shall apply:

(a) For Wire-bonded Integrated Circuit components: The rebonding of wires during assembly is not permitted.

(b) For components with column grid array packages: The entire column may be replaced only once.

(c) For Flip-chip Integrated Circuit components:

- Any polymer attached Add-on Component may be replaced twice at a given location.
- Any solder attached Add-on Component may be replaced once at a given location.
- The total number of replacements shall be limited to a maximum of 10% of the total number of Add-on Components.
- There shall be a maximum of 4 heating cycles for Add-on Component removal.
- It shall be demonstrated that the reliability of the remaining Add-on Components is not impacted.
- Neither rework nor repair of flip-chip attachment to the substrate (including underfill) is allowed.
- No thermal interface material rework is allowed after cure.
- For the purposes of rework or repair, no delidding is allowed where there is a physical link between die and lid (thermal interface material or other). If there is no physical link between die and lid, the components may be delidded and relidded provided that:
  - No more than one delid-relid cycle is performed.
  - Suitable screening tests shall be performed on the delidded-relidded components. These screening tests shall be defined at the stage when the delidding-relidding takes place and depend on the type of repair performed.

5.2 WAFER LOT ACCEPTANCE

5.2.1 Process Monitoring Review

For both Monolithic and Multichip Microcircuits, process monitoring review shall be done in compliance with the Manufacturer's SPC rules described in the PID (for qualification, qualification maintenance or procurement of qualified components).

A wafer shall be rejected if one or more process control data parameters exceed the allowed distribution as specified in the PID (for qualification, qualification maintenance or procurement of qualified components).

5.2.2 Wafer Lot Screening

Wafer Lot Screening of Die Components shall consist of the following tests and inspections:

(a) Go-no-go Room Temperature Electrical Measurements in accordance with Para. 8.14.3.1, either as an on-wafer measurement or after dice separation.

(b) Die Visual Inspection in accordance with Para. 8.1, after dice separation.

NOTE:
Die Visual Inspection may be performed on a selected sublot basis. The selected sublot shall consist of a minimum of the Die Components necessary for delivery, testing and allowable failures.

5.2.3 Die Dimensions

See Para. 4.8 for the minimum dimension requirements for Die Components that shall be specified in the Detail Specification. The dimensions of the Die Components as specified in the Detail Specification shall be guaranteed but not tested.

5.2.4 Scanning Electron Microscope (SEM) Inspection

For both Monolithic and Multichip Microcircuits, semiconductor dice incorporated into components supplied to this specification shall originate from a wafer lot that has been subjected to, and successfully met, the Scanning Electron Microscope Inspection requirements in accordance with Para. 8.5.

5.2.5 Total Dose Radiation Testing

For qualification or qualification maintenance of both Monolithic and Multichip Microcircuits:

- If specified in the Detail Specification, semiconductor dice incorporated into components shall originate from a wafer lot which has been subjected to and successfully completed Total Dose Radiation Testing in accordance with Para. 8.6 to the specified total dose level.

During procurement of both Monolithic and Multichip Microcircuits:

- If specified in the Detail Specification and stipulated in the Purchase Order, semiconductor dice incorporated into components shall originate from a wafer lot which has been subjected to and successfully completed Total Dose Radiation Testing in accordance with Para. 8.6 to the stipulated total dose level.

5.2.6 Documentation

Documentation of Wafer Lot Acceptance shall be in accordance with Para. 9.5.

5.3 SPECIAL IN-PROCESS CONTROLS

For Monolithic Microcircuits, tests and inspections shall be performed at Monolithic Microcircuit level. For Multichip Microcircuits, tests and inspections shall be performed at Multichip Microcircuit level.

5.3.1 Assembly of the Packaged Test Sublot for Die Components

For Die Components, sample dice shall be selected at random from each wafer lot and assembled into suitable packages. These samples make up the Packaged Test Sublot. For procurement of Die Components, the quantity of dice to be assembled, n, shall be selected from one of the following sampling plans. Unless otherwise specified, the selection shall be at the Manufacturer's discretion:

(a) n = 11 assembled dice from each wafer lot with 0 total Chart F3B failures allowed (see Para. 6.4.2.2)

(b) n = 18 assembled dice from each wafer lot with 1 total Chart F3B failures allowed (see Para. 6.4.2.2)

(c) n = 25 assembled dice from each wafer lot with 2 total Chart F3B failures allowed (see Para. 6.4.2.2)

(d) n = 38 assembled dice from each wafer lot with 3 total Chart F3B failures allowed (see Para. 6.4.2.2)

NOTE:

For qualification and maintenance of qualification of a single part type (ref. Para. 7.1.2.1), only sampling plans (c) and (d) shall apply.

In addition to the above quantities, 4 dice from each wafer lot shall also be selected and assembled for use in Bond Strength, Die Shear, Substrate Attach Strength and/or Flip-chip Pull-Off tests (as applicable) during Special In-Process Controls.

5.3.2 Internal Visual Inspection

(a) For Wire-bonded Integrated Circuit components: Internal Visual Inspection shall be performed in accordance with Para. 8.1.

(b) For Flip-chip Integrated Circuit components prior die attach, as follows:
- All packages/substrates shall be inspected to ensure the reliable soldering of balls on lands. Any non-conforming material shall be removed.

(c) For Flip-chip Integrated Circuit components after die attach, as follows:
- Internal Visual Inspection in accordance with Para. 8.1.
- Visual inspection of mounted Add-on Components in accordance with Para. 8.2.

(d) For Die Components: Internal Visual Inspection of the Packaged Test Sublot shall be performed in accordance with Para. 8.1.

Visual inspection of mounted Add-on Components shall be performed in accordance with Para. 8.2 if they are applicable to the package.

5.3.3 Bond Strength

Bond Strength shall be performed on test samples in accordance with Para. 8.3. A single failure shall be cause for lot failure. This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

For Multichip Microcircuits, testing shall be performed on each semiconductor die incorporated into the component.

5.3.4 Die Shear or Substrate Attach Strength (Non-Flip-Chip)

Either Die Shear or Substrate Attach Strength, as applicable, shall be performed on test samples in accordance with Para. 8.4(a) for Packaged Components, or 8.4(d) for Die Components.

For Multichip Microcircuits, testing shall be performed on each semiconductor die incorporated into the component.

A single failure shall be cause for lot failure. These tests are considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.5 Flip-Chip Pull-Off
Flip-chip Pull-Off shall be performed on test samples in accordance with Para. 8.4(b) for Packaged Components, or Para. 8.4(e) for Die Components.

A single failure shall be cause for lot failure. This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.6 Scanning Acoustic Microscopy (SAM)
SAM shall be performed in accordance with Para. 8.7.

5.3.7 Add-on Components Shear or Substrate Attach Strength
Either Shear or Substrate Attach Strength, as applicable, shall be performed on all Add-on Components mounted in test samples in accordance with Para. 8.4(c).

A single failure shall be cause for lot failure. This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.8 Lid Pull
Lid Pull shall be performed in accordance with Para. 8.8 on 2 samples. A single failure shall be cause for lot failure.

5.3.9 Lid Torque
Lid Torque shall be performed in accordance with Para. 8.9 on 2 samples. A single failure shall be cause for lot failure.

5.3.10 Dimension Check
Dimension Check shall be performed in accordance with Para. 8.18 on 3 samples only. In the event of any failure a 100% Dimension Check shall be performed.

5.3.11 Weight
The maximum weight of the component specified in the Detail Specification shall be guaranteed but not tested.

5.3.12 Documentation
Documentation of Special In-Process Controls shall be in accordance with Para. 9.6.

6 SCREENING TESTS

6.1 GENERAL

Unless otherwise specified herein or in the Detail Specification, all lots of components used for qualification and qualification maintenance, Lot Validation Testing, and for delivery, shall be subjected to tests and inspections in accordance with Chart F3A for Packaged Components and Chart F3B for Die Components, in the sequence shown.

For Monolithic Microcircuits, tests and inspections shall be performed at Monolithic Microcircuit level. For Multichip Microcircuits, tests and inspections shall be performed at Multichip Microcircuit level.

For Die Components, testing shall be performed on the Packaged Test Sublot.

All components shall be serialised prior to the tests and inspections.

Any components which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The applicable test methods and conditions are specified in the paragraphs referenced in Charts F3A and F3B.

6.2 FAILURE CRITERIA

6.2.1 Environmental and Mechanical Test Failure

The following shall be counted as component failures:

- Components which fail during tests for which the pass/fail criteria are inherent in the test method, i.e. PIND, Solderability, Seal and External Visual Inspection.

6.2.2 Parameter Drift Failure

The acceptable change limits are shown in Parameter Drift Values in the Detail Specification. A component shall be counted as a parameter drift failure if the changes during High Temperature Reverse Bias Burn-in or during Power Burn-in are larger than the drift values (Δ) specified.

6.2.3 Parameter Limit Failure

A component shall be counted as a limit failure if one or more parameters exceed the limits shown in Room Temperature Electrical Measurements or High and Low Temperatures Electrical Measurements in the Detail Specification.

For Packaged Components, any component which exhibits a limit failure prior to the submission to HTRB Burn-in shall be rejected and not counted when determining lot rejection.

6.2.4 Other Failures

A component shall be counted as a failure in any of the following cases:

- Visual failure.
- Mechanical failure.
- Handling failure.
- Lost component.

6.3 FAILED COMPONENTS

A component shall be considered as a failed component if it exhibits one or more of the failure modes described in Para. 6.2.

6.4 LOT FAILURE

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.3.

6.4.1 Lot Failure for Packaged Components

6.4.1.1 Lot Failure during 100% Testing

If the number of components failed on the basis of the failure criteria specified in Paras. 6.2.2 and 6.2.3 exceeds 5% (rounded upwards to the nearest whole number) of the components submitted to High Temperature Reverse Bias Burn-in (or Power Burn-in if HTRB Burn-in is not being performed) of Chart F3A, the lot of Packaged Components shall be considered as failed.

If a lot is composed of groups of components of one family defined in one ESCC Detail Specification, but separately identifiable for any reason, then the lot failure criteria shall apply separately to each identifiable group.

6.4.1.2 Lot Failure during Sample Testing

A lot shall be considered as failed if the number of allowable failures during sample testing as specified herein or in the Detail Specification, is exceeded.

Unless otherwise specified, if a lot failure occurs, a 100% testing may be performed but the cumulative percent defective shall not exceed that specified in Para. 6.4.1.1.

No failures are allowed for the Solderability test.

6.4.2 Lot Failure for Die Components

6.4.2.1 Lot Failure Prior to Burn-in Testing of the Packaged Test Sublot

If the number of components failed during Room Temperature Electrical Measurements, and High and Low Temperatures Electrical Measurements (if performed) prior to HTRB Burn-in in Chart F3B, on the basis of the failure criteria specified in Para. 6.2.3, exceeds the following allowed failures, the wafer lot shall be considered as failed:

Packaged Test Sublot Sample Size n	Total Number of Allowed Failures per Paras. 8.14.2 & 8.14.3.2 (prior to HTRB Burn-in)
11	0
18	1
25	2
38	3

6.4.2.2 Lot Failure After Burn-in Testing of the Packaged Test Sublot

If the number of components failed during Parameter Drift Values, Room Temperature Electrical Measurements, and High and Low Temperatures Electrical Measurements subsequent to HTRB Burn-in in Chart F3B, on the basis of the failure criteria specified in Paras. 6.2.2 and 6.2.3, exceeds the following allowed failures, the wafer lot shall be considered as failed.

In addition, if the total number of failures at any point during Chart F3B, on the basis of the failure criteria specified in Paras. 6.2.2 and 6.2.3, exceeds the following allowed failures, the wafer lot shall be considered as failed:

Packaged Test Sublot Sample Size n	Total Number of Allowed Failures per Paras. 8.14.1, 8.14.2, & 8.14.3.2 (subsequent to HTRB Burn-in)	Total Number of Allowed Failures per Paras. 8.14.1, 8.14.2, & 8.14.3.2 (at any time during Chart F3B)
11	0	0
18	1	1
25	1	2
38	2	3

6.5 DOCUMENTATION

Documentation of Screening Tests shall be in accordance with Para. 9.8.

7 QUALIFICATION, QUALIFICATION MAINTENANCE AND LOT VALIDATION TESTING

The requirements of this paragraph are applicable to the tests performed on components or test structures as part of qualification or qualification maintenance in accordance with either ESCC Basic Specification No. 20100, 24300 or 25400 as applicable. They are also applicable to Lot Validation Testing as part of the procurement of qualified or unqualified components.

7.1 QUALIFICATION TESTING

7.1.1 General

Qualification testing shall be in accordance with the requirements specified in Chart F4A for Packaged Components or Chart F4B for Die Components.

For Packaged Components, the tests of Chart F4A shall be performed on the specified sample, chosen at random from the components which have successfully passed the tests in Chart F3A.

For Die Components, the tests of Chart F4B shall be performed on the specified sample chosen at random from the components of the Packaged Test Sublot which have successfully passed the tests in Chart F3B.

This sample constitutes the Qualification Test Lot. The Qualification Test Lot is divided into subgroups of tests and, unless otherwise specified, all components assigned to a subgroup shall be subjected to all of the tests in that subgroup, in the sequence shown. The applicable test requirements are detailed in the paragraphs referenced in Charts F4A and F4B.

For Monolithic Microcircuits, tests and inspections shall be performed at Monolithic Microcircuit level. For Multichip Microcircuits, tests and inspections shall be performed at Multichip Microcircuit level.

The conditions governing qualification testing are specified in ESCC Basic Specification No. 20100.

7.1.2 Distribution within the Qualification Test Lot

The Qualification Test Lot shall be comprised in accordance with the following provisions, depending on whether it is required to obtain qualification for a single component type or for a family of component types.

7.1.2.1 Single Component Type

When it is proposed to submit a single component type for qualification testing, the sample quantity shall be as specified in Charts F4A and F4B, Note 1. However, for Packaged Components, when such a single component type is to be qualified in more than one type of package, each package variation must be equally represented in, the Environmental/Mechanical, Endurance and Assembly Capability Subgroups of Chart F4A. For this purpose, unless otherwise specified, the applicable sample distribution shall be the same as for the qualification of a family of component types as specified in Chart F4A, Note 2 or Note 3.

7.1.2.2 Family of Component Types

A family of component types is a series of components produced by the same manufacturing techniques, using the same types of machines and apparatus. Such components will be designed for the same supply, bias and signal voltages and for an input/output compatibility with each other under an established set of loading rules. They shall be produced using the same technology (e.g. the same diffusion schedules, method of metallisation, etc.) and identical design rules.

Qualification may be granted to a family of components subject to the successful outcome of the qualification testing of certain specified component types to represent the family.

Structurally similar components from such a family may be grouped together for the purpose of selecting samples for qualification testing. The component types selected must adequately represent all of the various mechanical, structural and electrical elements encountered within the family.

The component types chosen must be those that employ the extremes of design rules and tolerances and contain the maximum of internal sub-circuitry complexity, i.e. usually those that give the greatest risk of rejection.

For Packaged Components, when qualification is required for component types in more than one type of package, each package must be adequately represented in the Environmental/Mechanical, Endurance and Assembly Capability subgroups.

The component types may be specified by, but in any case shall be agreed with the ESCC Executive prior to the commencement of qualification testing and the justification for the selection shall be declared in the qualification test report.

The number of component types selected as representative of the family will therefore determine the total number of components comprising the qualification test lot. Unless otherwise specified, depending on the number of types selected, the sample sizes shall be as specified in Charts F4A and F4B, Note 2 or Note 3.

In the case of four or more component types selected, different pass/fail criteria from those shown in Charts F4A and F4B may be applicable. When appropriate, these shall be agreed with the ESCC Executive prior to the commencement of qualification testing.

7.2 QUALIFICATION WITHIN A CAPABILITY APPROVED DOMAIN

The qualification of a component within a capability approved domain shall be in accordance with ESCC Basic Specification No. 24300.

7.3 QUALIFICATION WITHIN A TECHNOLOGY FLOW

The qualification of a component produced using a qualified Technology Flow shall be in accordance with ESCC Basic Specification No. 25400.

7.4 QUALIFICATION MAINTENANCE (PERIODIC TESTING)

Qualification is maintained through periodic testing and the test requirements of Para. 7.1 shall apply. For each subgroup, the sample size, the test requirements and the period between successive subgroup testing shall be as specified in Chart F4A for Packaged Components and Chart F4B for Die Components.

The conditions governing qualification maintenance are specified in ESCC Basic Specification No. 20100.

Qualification of a component within a capability approved domain is maintained by maintenance of the approval of the capability domain itself in accordance with ESCC Basic Specification No. 24300.

Qualification of a component, produced using a qualified Technology Flow, is maintained by the maintenance of the Technology Flow Qualification itself in accordance with ESCC Basic Specification No. 25400.

7.5 LOT VALIDATION TESTING

For procurement of qualified Packaged Components or qualified Die Components, Lot Validation Testing is not required and shall only be performed if specifically stipulated in the Purchase Order.

For procurement of unqualified Packaged Components or unqualified Die Components, the need for Lot Validation Testing shall be determined by the Orderer (ref. ESCC Basic Specification No. 23100).

When Lot Validation Testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of Chart F4A or F4B (as applicable). The testing to be performed and the sample size shall be as stipulated in the Purchase Order.

When procurement of more than one component type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the Purchase Order.

7.6 FAILURE CRITERIA

The following criteria shall apply to qualification, qualification maintenance and Lot Validation Testing.

7.6.1 Environmental and Mechanical Test Failure

The following shall be counted as component failures:

- Components which fail during tests for which the pass/fail criteria are inherent in the test method, e.g. Seal, Terminal Strength, etc.

7.6.2 Electrical Failure

The following shall be counted as component failures:

- Components which fail one or more of the applicable limits at each of the relevant data points specified for environmental, mechanical and endurance testing in Intermediate and End-Point Electrical Measurements in the Detail Specification.

7.6.3 Other Failures

A component shall be counted as a failure in any of the following cases:

- Visual failure
- Mechanical failure
- Handling failure
- Lost component

7.7 FAILED COMPONENTS

A component shall be considered as failed if it exhibits one or more of the failure modes detailed in Para. 7.6.

When requested by the ESCC Executive (for qualification, qualification maintenance or procurement of qualified components) or the Orderer (for procurement of qualified or unqualified components), failure analysis of failed components shall be performed under the responsibility of the Manufacturer and the results provided.

Failed components shall be retained at the Manufacturer's plant until the final disposition has been agreed and certified.

7.8 LOT FAILURE

For qualification and qualification maintenance, the lot shall be considered as failed if one component in any subgroup of Chart F4A or F4B (as applicable) is a failed component based on the criteria specified in Para. 7.6.

For procurement, the lot shall be considered as failed if one component in any test specified for Lot Validation Testing is a failed component based on the criteria specified in Para. 7.6.

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.3.

7.9 QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING SAMPLES

All tests of Charts F4A and F4B are considered to be destructive and therefore components so tested shall not form part of the delivery lot.

7.10 DOCUMENTATION

Documentation of Qualification, Periodic Testing and Lot Validation Testing shall be in accordance with Para. 9.9.

8 TEST METHODS AND PROCEDURES

If a Manufacturer elects to eliminate or modify a test method or procedure, the Manufacturer is still responsible for delivering components that meet all of the performance, quality and reliability requirements defined in this specification and the Detail Specification.

For a qualified component, documentation supporting the change shall be approved by the ESCC Executive and retained by the Manufacturer. It shall be copied, when requested, to the ESCC Executive. The change shall be specified in an appendix to the Detail Specification and in the PID.

For an unqualified component, the change shall be approved by the Orderer. The change may be specified in an appendix to the Detail Specification at the request of the Manufacturer or Orderer, subject to the approval of the ESCC Executive.

8.1 INTERNAL VISUAL INSPECTION AND DIE VISUAL INSPECTION

ESCC Basic Specification No. 20400.

8.2 INSPECTION OF ADD-ON COMPONENTS

All mounted Add-on Components shall be visually inspected in accordance with MIL-STD-883, Test Method 2032.

8.3 BOND STRENGTH

MIL-STD-883, Test Method 2011.

- Test Conditions:
  - Test condition C or D for thermo-compression, ultrasonic or wedge bonding.
  - Test condition G or H for beam lead bonding.
- Test Samples:
  - Quantity of internal bond wires 8 or less; Test samples = 3, Test all bonds
  - Quantity of internal bond wires 9 to 24; Test samples = 2, Test all bonds
  - Quantity of internal bond wires 25 or more; Test samples = 2, Test 50% of bonds

  For Multichip Microcircuits, the above internal bond wire sampling shall apply to each semiconductor die incorporated into the component.

  For Packaged Components during Special In-Process Controls (Chart F2A), the required test samples shall be selected at random from the lot of components accepted after Internal Visual Inspection.

  For Packaged Components during Qualification, Periodic Testing and Lot Validation Testing (Chart F4A), the required test samples shall be selected from the components in the Assembly Capability Subgroup.

  For Die Components during Special In-Process Controls (Chart F2B), 4 test samples shall be selected at random from the components of the Packaged Test Sublot accepted after Die Attach and Internal Visual Inspection.

  For Die Components during Qualification, Periodic Testing and Lot Validation Testing (Chart F4B), the required test samples shall be selected from the components of the Packaged Test Sublot in the De-encapsulation Subgroup.

If agreed by the ESCC Executive (for qualification or qualification maintenance) or the Orderer (for procurement) the test samples for Special In-Process Controls may have only passed the low magnification phase of the Internal Visual Inspection.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

8.4 DIE SHEAR, SUBSTRATE ATTACH STRENGTH OR FLIP-CHIP PULL-OFF

(a) For Wire-bonded Integrated Circuit components:
Die Shear, or Substrate Attach Strength (as applicable): MIL-STD-883, Test Method 2019 or 2027.

- Test Samples:
  The same test samples submitted to Bond Strength shall be tested.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.
For Multichip Microcircuits, testing shall be performed on each semiconductor die incorporated into the component.

(b) For Flip-chip Integrated Circuit components:
Flip-chip Pull-Off: MIL-STD-883, Test Method 2031.

- Test Samples:
  - For Special In-Process Controls (Chart F2A): 1 sample selected at random from the lot shall be tested.
  - For Qualification, Periodic Testing and Lot Validation Testing (Chart F4A): 3 samples selected from the components in the Assembly Capability Subgroup shall be tested.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

(c) For Add-on Components mounted in Flip-chip Integrated Circuit components:
Die Shear or Substrate Attach Strength (as applicable): MIL-STD-883, Test Method 2019 or 2027.

- Test Samples:
  - For Special In-Process Controls (Chart F2A): all Add-on Components mounted in 1 sample selected at random from the lot shall be tested.
  - For Qualification, Periodic Testing and Lot Validation Testing (Chart F4A): all Add-on Components mounted in 1 sample from the components in the Assembly Capability Subgroup shall be tested.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

(d) For Die Components designed for assembly into Wire-bonded Integrated Circuit components:
Die Shear, or Substrate Attach Strength (as applicable): MIL-STD-883, Test Method 2019 or 2027.

- Test Samples:
  The same Packaged Test Sublot samples submitted to Bond Strength shall be tested.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

(e) For Die Components designed for assembly into Flip-chip Integrated Circuit components:
Flip-chip Pull-Off: MIL-STD-883, Test Method 2031.

- Test Samples:
  - For Special In-Process Controls (Chart F2B): 1 sample selected at random from the components of the Packaged Test Sublot accepted after Die Attach shall be tested.
  - For Qualification, Periodic Testing and Lot Validation Testing (Chart F4B): 3 samples selected from the components of the Packaged Test Sublot in the De-encapsulation Subgroup shall be tested.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

8.5 SCANNING ELECTRON MICROSCOPE INSPECTION
ESCC Basic Specification No. 21400.

NOTE:
For components manufactured with semiconductor processes that defeat the objectives of the above specification, the deviations from the specified requirements shall be identified in the PID and the Detail Specification.

8.6 TOTAL DOSE RADIATION TESTING
ESCC Basic Specification No. 22900 to the total dose level specified in the Detail Specification or as stipulated in the Purchase Order.

For both Monolithic and Multichip Microcircuits, testing shall be performed on each semiconductor die type incorporated into the component, in accordance with the Detail Specification.

8.7 SCANNING ACOUSTIC MICROSCOPY
MIL-STD-883, Test Method 2030. SAM shall be performed to detect defects at die/underfill and underfill/package interfaces, and at lid/thermal interface material and thermal interface material/die interfaces (as applicable).

8.8 LID PULL
MIL-STD-883, Test Method 2027.

8.9 LID TORQUE
MIL-STD-883, Test Method 2024.

8.10 HIGH TEMPERATURE STABILISATION BAKE
MIL-STD-883, Test Method 1008. Duration: 24 hours at maximum storage temperature rating specified in the Detail Specification.

8.11 CONSTANT ACCELERATION

8.11.1 Screening Tests (Chart F3A)
Unless otherwise specified in the Detail Specification:

(a) For packages ≤ 25.4mm × 25.4mm: MIL-STD-883, Test Method 2001, Test Condition B.
(b) For packages > 25.4mm × 25.4mm and ≤ 25.4mm × 50.8mm: MIL-STD-883, Test Method 2001, Test Condition A.
(c) For packages > 25.4mm × 50.8mm: Shall not be performed.

8.11.2 Qualification, Periodic Testing and Lot Validation Testing (Chart F4A)
MIL-STD-883, Test Method 2001, Test Condition E (resultant centrifugal acceleration to be in the Y1 axis only). For components which have a package weight of 5 grammes or more, or whose inner seal or cavity perimeter is more than 5 cm, Condition D shall be used.

8.12 TEMPERATURE CYCLING

8.12.1 Screening Tests (Chart F3A)
MIL-STD-883, Test Method 1010. Test Condition C (10 cycles).

8.12.2 Qualification, Periodic Testing and Lot Validation Testing (Chart F4A)

(a) For Wire-bonded Integrated Circuit components:
MIL-STD-883, Test Method 1010. Test Condition C, except the number of cycles shall be 100 minimum.

(b) For Flip-chip Integrated Circuit components:
MIL-STD-883, Test Method 1010. Test Condition B, except the number of cycles shall be 100 minimum.

8.13 PARTICLE IMPACT NOISE DETECTION (PIND)
MIL-STD-883, Test Method 2020, Test Condition A.

8.14 ELECTRICAL MEASUREMENTS

8.14.1 Parameter Drift Values
At each of the relevant data points during Screening Tests (Charts F3A and F3B), Parameter Drift Values shall be measured as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated.

8.14.2 High and Low Temperatures Electrical Measurements
High and Low Temperatures Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.14.3 Room Temperature Electrical Measurements

8.14.3.1 Room Temperature Electrical Measurements during Wafer Lot Acceptance (Chart F2B)
Unless otherwise specified, go-no-go Room Temperature Electrical Measurements shall be performed as specified in the Detail Specifications. All failed dice shall be clearly identified.

8.14.3.2 Room Temperature Electrical Measurements during Screening Tests (Charts F3A and F3B)
Room Temperature Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.14.4 Intermediate and End-Point Electrical Measurements
At each of the relevant data points during Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B), Intermediate and End-Point Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated, if specified.

8.15 HIGH TEMPERATURE REVERSE BIAS BURN-IN
MIL-STD-883, Test Method 1015, Test Condition A.

- Duration and Test Conditions: As specified, where applicable, in High Temperature Reverse Bias Burn-in in the Detail Specification.
- Data Points:
  As specified in the Parameter Drift Values in the Detail Specification at 0 hour (initial) and T (+24 -0) hours (where T is the specified duration). Drift shall be related to the initial measurement.

8.16 POWER BURN-IN
MIL-STD-883, Test Method 1015, Test Condition B, D or E.

- Duration: Unless otherwise specified in the Detail Specification, components shall be subjected to a total Power Burn-in period of 240 (+24 -0) hours.
- Test Conditions: As specified in Power Burn-in in the Detail Specification.
  The alternative temperature and time combinations per MIL-STD-883 Test Method 1015 are permissible provided that the maximum operating ratings for a component are not exceeded.
- Data Points:
  As specified in Parameter Drift Values in the Detail Specification at T (+24 -0) hours (where T is the specified duration).

  If High Temperature Reverse Bias Burn-in is not being performed, the 0 hour (initial) measurement is also required. Drift shall be related to the initial measurement for Power Burn-in.

8.17 SEAL

8.17.1 Seal, Fine Leak
MIL-STD-883, Test Method 1014, Condition A or B.

8.17.2 Seal, Gross Leak
MIL-STD-883, Test Method 1014, Condition C.

8.18 EXTERNAL VISUAL INSPECTION AND DIMENSION CHECK
External Visual Inspection shall be performed in accordance with ESCC Basic Specification No. 20500.

Dimension Check (during Special In-Process Controls only) shall be performed in accordance with ESCC Basic Specification No. 20500 and the Detail Specification on a sample of 3 components. In the event of any failure a 100% Dimension Check shall be performed.

8.19 SOLDERABILITY

For procurement lots: 5 samples. A single failure shall be cause for lot failure.

MIL-STD-883, Test Method 2003, to be performed on all terminals.

Solderability testing may be performed on empty packages or electrical rejects. The test samples used must be of the same package type and must have been manufactured using the same process, at the same time and have been subjected to the same screening as the packages of the delivery lot with which they are associated.

For components with gold plated lead finish, activated fluxes (RMA, RA and OA) may be used but shall be immediately cleaned off after dipping, using an acceptable solvent.

Solderability testing is classed as destructive and therefore components so tested shall not form part of the delivery lot.

8.20 MECHANICAL SHOCK

Unless otherwise specified in the Detail Specification:

(a) For packages ≤ 25.4mm × 50.8mm: MIL-STD-883, Test Method 2002, Test Condition B.
(b) For packages > 25.4mm × 50.8mm: MIL-STD-883, Test Method 2002, Test Condition B, except the peak level shall be 1000g.

8.21 VIBRATION

MIL-STD-883, Test Method 2007, Test Condition A.

8.22 THERMAL SHOCK

MIL-STD-883. Test Method 1011, Test Condition B.

8.23 MOISTURE RESISTANCE

(a) For components with Hermetic Packages: MIL-STD-883, Test Method 1004.
(b) For Flip-chip Integrated Circuit components with Non-Hermetic Packages: JESD22-A118, Condition B

8.24 PRECONDITIONING

J-STD-020. Conditions as specified in the Detail Specification.

8.25 OPERATING LIFE

MIL-STD-883, Test Method 1005.

- Duration: 2000 hours (or 4000 hours if applicable; see Para. 4.2.1(b)).
- Conditions: As specified in Operating Life in the Detail Specification.
- Data Points:
  As specified in Intermediate and End-Point Electrical Measurements in the Detail Specification at 0 hour, 1000 ±48 hours and 2000 ±48 hours (and 4000 ±48 hours if applicable). If drift values are specified, the drift shall always be related to the 0 hour measurement.

8.26 PERMANENCE OF MARKING

ESCC Basic Specification No. 24800.

8.27 TERMINAL STRENGTH

(a) For chip carrier packages: MIL-STD-883, Test Method 2004, Test Condition D.

(b) For ball grid array packages: JESD22-B117; 45 balls from 2 devices minimum.

(c) For column grid array packages: MIL-STD-883, Test Method 2038; 45 columns from 2 devices minimum.

(d) For other packages: MIL-STD-883, Test Method 2004, Test Condition B2; 3 leads (excluding corner leads) or 10% of the leads (whichever is greater) randomly selected on each component.

8.28 INTERNAL GAS ANALYSIS

MIL-STD-883, Test Method 1018.

9 DATA DOCUMENTATION

9.1 GENERAL

For the qualification, qualification maintenance and procurement for each lot a data documentation package shall exist in a printed or electronic form.

This package shall be compiled from:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Wafer Lot Acceptance data (Charts F2A and F2B).
(e) Special In-Process Controls data (Charts F2A and F2B).
(f) Add-on Components procurement and testing data.
(g) Screening Tests data (Charts F3A and F3B).
(h) Qualification, Periodic Testing and Lot Validation Testing (when applicable) data (Charts F4A and F4B).
(i) Failed components list and failure analysis report (when applicable).
(j) Certificate of Conformity.

Items (a) to (j) inclusive shall be grouped, preferably as subpackages and, for identification purposes, each page shall include the following information:

- ESCC Component Number.
- Manufacturer's name.
- Lot identification.
- Date of establishment of the document.
- Page number.

Whenever possible, documentation should preferably be available in electronic format suitable for reading using a compatible PC. The format supplied shall be legible, durable and indexed. The preferred storage medium is CD-ROM and the preferred file format is PDF.

9.1.1 Qualification and Qualification Maintenance

In the case of qualification or qualification maintenance, the items listed in Para. 9.1(a) to (j) are required.

9.1.2 Component Procurement and Delivery

For all deliveries of components procured to this specification, the following documentation shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity).
(b) Certificate of Conformity (including range of delivered serial numbers for Packaged Components or the wafer lot number for Die Components).

9.1.3 Additional Documentation

The Manufacturer shall deliver additional documentation containing data and reports to the Orderer, if stipulated in the Purchase Order.

9.1.4 Data Retention/Data Access

If not delivered, all data shall be retained by the Manufacturer for a minimum of 5 years during which time it shall be available for review, if requested, by the Orderer or the ESCC Executive (for qualified components).

9.2 COVER SHEET(S)

The cover sheet(s) of the data documentation package shall include as a minimum:

(a) Reference to the Detail Specification, including issue and date.
(b) Reference to the applicable ESCC Generic Specification, including issue and date.
(c) ESCC Component Number and the Manufacturer's part type number.
(d) Lot identification (including wafer lot number for Die Components).
(e) Range of delivered serial numbers (for Packaged Components).
(f) Number of the Purchase Order.
(g) Total dose radiation test level (if applicable).
(h) Information relative to any additions to this specification and/or the Detail Specification.
(i) Manufacturer's name and address.
(j) Location of the manufacturing plant (specify place of diffusion, assembly and test).
(k) Signature on behalf of Manufacturer.
(l) Total number of pages of the data package.

9.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be prepared. Where applicable, this list shall contain inventory number, Manufacturer's type number, serial number, etc. This list shall indicate for which tests such equipment was used.

9.4 LIST OF TEST REFERENCES

This list shall include all Manufacturer's references or codes which are necessary to correlate the test data provided with the applicable tests specified in the tables of the Detail Specification.

9.5 WAFER LOT ACCEPTANCE DATA (CHARTS F2A AND F2B)

For Die Components, a test result summary shall be compiled giving the total number of dice submitted to and the total number of dice rejected after each of the tests. For each test requiring electrical measurements, the results shall be traceable to wafer lot.

Data of SEM Inspection shall be prepared in accordance with the requirements of ESCC Basic Specification No. 21400.

A total dose radiation test report shall be prepared in accordance with the requirements of ESCC Basic Specification No. 22900 (if specified).

9.6 SPECIAL IN-PROCESS CONTROLS DATA (CHARTS F2A AND F2B)

A test result summary shall be compiled showing the total number of components submitted to, and the total number rejected after each of the tests. For all Bond Strength, Die Shear, Substrate Attach Strength and Flip-chip Pull-Off tests, the separation forces and categories shall be recorded.

9.7 ADD-ON COMPONENTS PROCUREMENT AND TESTING DATA (PARA. 4.6)

A summary of the procurement details applicable to all Add-on Components shall be complied including:

- Procurement specification(s) number and quality level
- Manufacturer's name and location
- Lot identification
- Certificate of Conformity
- Traceability information against component serial number

For Add-on Component testing in accordance with Para. 5.3.7, a test result summary shall be compiled. For Shear or Substrate Attach Strength tests, the separation forces and categories shall be recorded.

9.8 SCREENING TESTS DATA (CHARTS F3A AND F3B)

A test result summary shall be compiled showing the total number of components submitted to and the total number rejected after each of the tests. For each test requiring electrical measurements, the results shall be recorded against component serial number. Component drift calculations shall be recorded for each specified test against component serial number.

9.9 QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING DATA (CHARTS F4A AND F4B)

9.9.1 Qualification Testing

A test result summary shall be compiled showing the components submitted to, and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

9.9.2 Periodic Testing for Qualification Maintenance

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

In addition to the full test data a report shall be compiled for each subgroup of Chart F4A or F4B (as applicable) to act as the most recent Periodic Testing summary. These reports shall include a list of all tests performed in each subgroup, the ESCC Component Numbers and quantities of components tested, a statement confirming all the results were satisfactory, the date the tests were performed and a reference to the full test data.

9.9.3 Lot Validation Testing

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup (as applicable). Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

9.10 FAILED COMPONENTS LIST AND FAILURE ANALYSIS REPORT

The failed components list and failure analysis report shall provide full details of:

(a) The reference and description of the test or measurement performed as defined in this specification and/or the Detail Specification during Wafer Lot Acceptance, Special In-Process Controls, Screening Tests and Qualification, Periodic Testing and Lot Validation Testing.
(b) Traceability information including wafer lot and serial number (if applicable) of the failed component.
(c) The failed parameter and the failure mode of the component.
(d) Detailed failure analysis (if requested by the ESCC Executive or Orderer).

9.11 CERTIFICATE OF CONFORMITY

A Certificate of Conformity shall be established in accordance with the requirements of ESCC Basic Specification Nos. 20100, 24300 or 25400.

10 DELIVERY

For procurement, for each order, the items forming the delivery are:

(a) The delivery lot.
(b) The components used for Lot Validation Testing (as applicable), but not forming part of the delivery lot, if stipulated in the Purchase Order.
(c) The relevant documentation in accordance with the requirements of Paras. 9.1.2 and 9.1.3.

NOTE: Except for qualification or qualification maintenance of Die Components, the Packaged Test Sublot samples may be delivered if so stipulated in the Purchase Order.

In the case of a component for which a valid qualification is in force, all data of all components submitted to Lot Validation Testing shall also be copied, when requested, to the ESCC Executive.

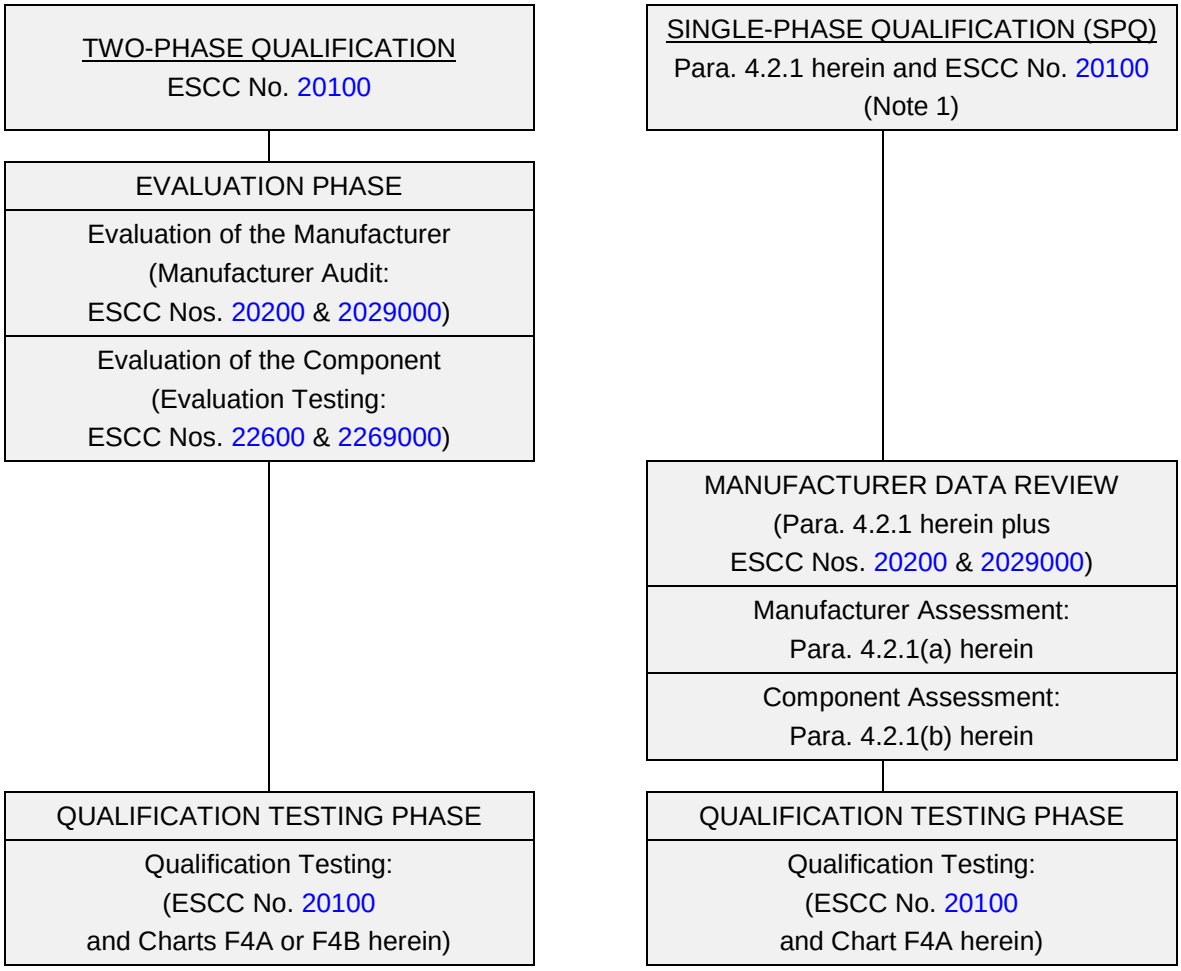
For qualification or qualification maintenance, the disposition of the Qualification Test Lot and its related documentation shall be as specified in ESCC Basic Specification Nos. 20100, 24300 or 25400 and the relevant paragraphs of Section 9 of this specification.

11 PACKAGING AND DISPATCH

The packaging and dispatch of components to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 20600.

12 CHARTS

12.1 CHART F0 (INFORMATIVE) – INITIAL (PRODUCT) QUALIFICATION

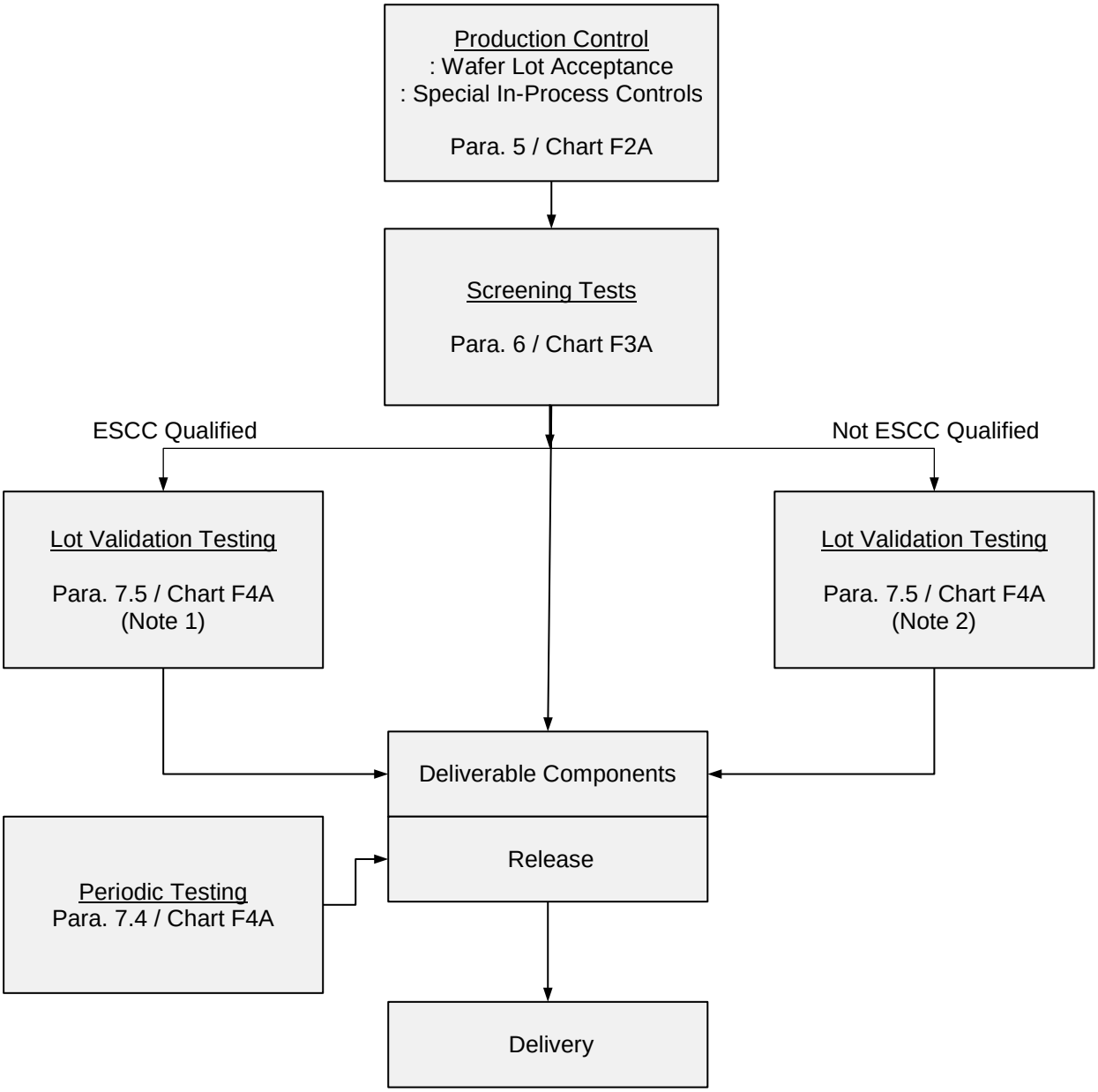


NOTES:

1. SPQ is exclusively for qualification of Wire-bonded Integrated Circuits.

12.2 CHART F1 - GENERAL FLOW FOR PROCUREMENT

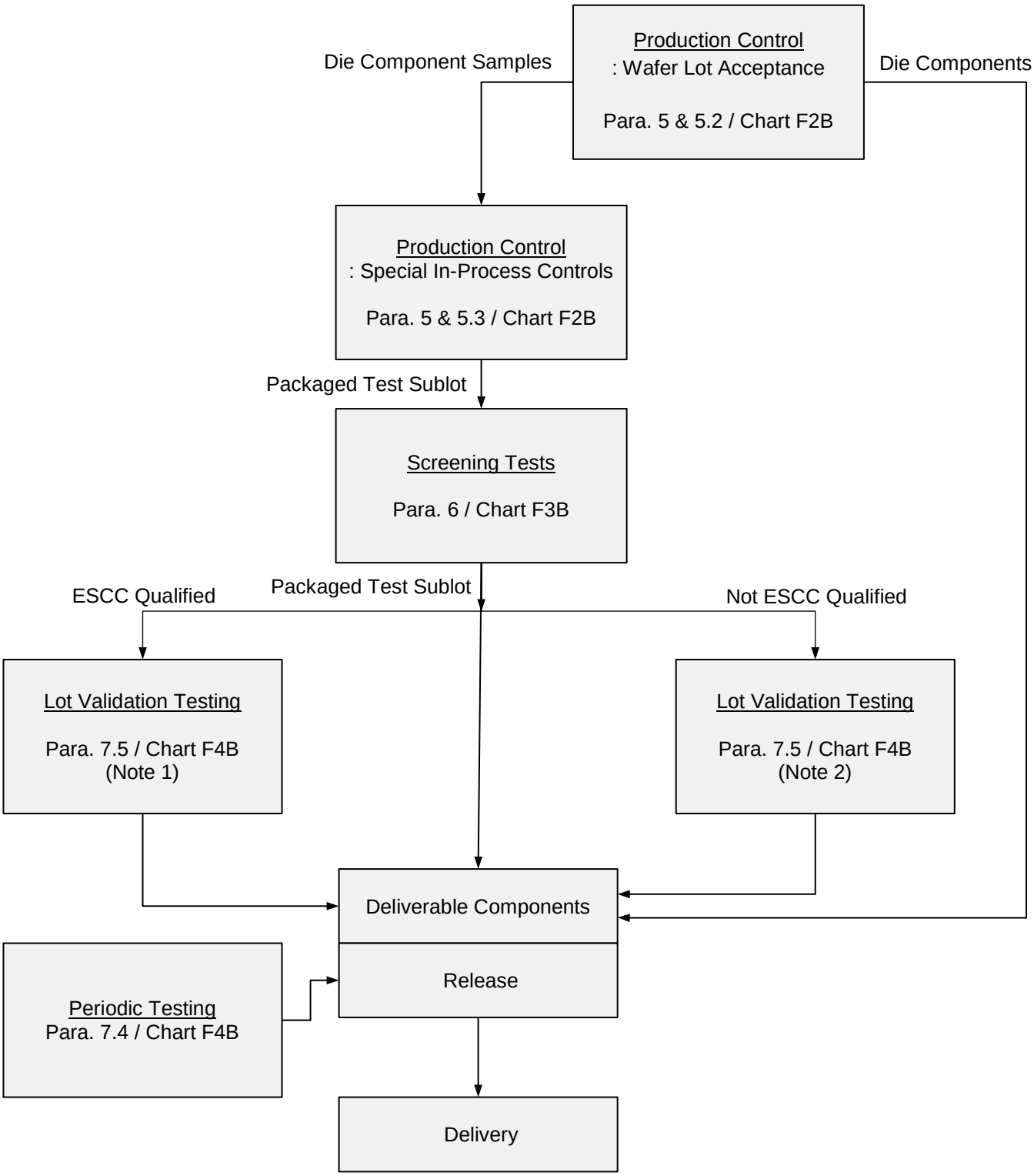
12.2.1 Chart F1A - General Flow for Procurement of Packaged Components



NOTES:

1. Lot Validation Testing is not required for qualified Packaged Components unless specifically stipulated in the Purchase Order.
2. For unqualified Packaged Components, the need for Lot Validation Testing shall be determined by the Orderer and the required testing shall be as stipulated in the Purchase Order (ref. ESCC Basic Specification No. 23100).

12.2.2 Chart F1B - General Flow for Procurement of Die Components



NOTES:

1. Lot Validation Testing is not required for qualified Die Components unless specifically stipulated in the Purchase Order.
2. For unqualified Die Components, the need for Lot Validation Testing shall be determined by the Orderer and the required testing shall be as stipulated in the Purchase Order (Ref. ESCC Basic Specification No. 23100).

12.3 CHART F2 - PRODUCTION CONTROL

12.3.1 Chart F2A – Production Control for Packaged Components

COMPONENT LOT MANUFACTURING	

WAFER LOT ACCEPTANCE	
Para. 5.2.1	Process Monitoring Review
Para. 5.2.4	SEM Inspection (1)
Para. 5.2.5	Total Dose Radiation Testing (1) (2)

SPECIAL IN-PROCESS CONTROLS			
WIRE-BONDED INTEGRATED CIRCUIT COMPONENTS		FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS	
Para. 5.3.2(a)	Internal Visual Inspection	Para. 5.3.2(b)	Package/Substrate Visual Inspection
Para. 5.3.3	Bond Strength (1)	-	Die Attach
Para. 5.3.4	Die Shear or Substrate Attach Strength (1)	Para. 5.3.5	Flip-Chip Pull-Off (1)
-	Encapsulation	-	Underfill
		Para. 5.3.6	SAM
		-	Add-on Components Attach (3)
		Para. 5.3.2(c)	Internal Visual Inspection & Visual Inspection of Add-on Components
		Para. 5.3.7	Add-on Components Shear or Substrate Attach Strength (1)
		-	Encapsulation or Heat-spreader Attach
		Para. 5.3.6	SAM (4)
		Para. 5.3.8	Lid Pull (1) (5)
		Para. 5.3.9	Lid Torque (1) (6)

Para. 5.3.10	Dimension Check (1)
Para. 5.3.11	Weight (7)

TO CHART F3A – SCREENING TESTS

NOTES:

1. Performed on a sample basis.
2. Only required if specified in the Detail Specification and stipulated in the Purchase Order.
3. May be performed at any point prior to Internal Visual inspection.
4. Only applicable to Flip-chip Integrated Circuit components with thermal interface material between die and lid/heat-spreader.
5. Only applicable to Flip-chip Integrated Circuit components with Non-Hermetic Packages.
6. Only applicable to Flip-chip Integrated Circuit components with glass frit sealed Hermetic Packages.
7. Guaranteed but not tested.

12.3.2 Chart F2B – Production Control for Die Components

WAFER LOT MANUFACTURING	
WAFER LOT ACCEPTANCE	
Para. 5.2.1	Process Monitoring Review
Para. 5.2.2(a)	Room Temperature Electrical Measurements (Wafer Lot Screening) (1)
-	Wafer Dicing
Para. 5.2.2(b)	Die Visual Inspection (Wafer Lot Screening)
Para. 5.2.3	Die Dimensions (2)
Para. 5.2.4	SEM Inspection (3)
Para. 5.2.5	Total Dose Radiation Testing (3) (4)

SPECIAL IN-PROCESS CONTROLS			
DIE COMPONENTS DESIGNED FOR ASSEMBLY INTO WIRE-BONDED INTEGRATED CIRCUIT COMPONENTS		DIE COMPONENTS DESIGNED FOR ASSEMBLY INTO FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS	
-	Die Attach (5)	Para. 5.3.2(b)	Package/Substrate Visual Inspection
Para. 5.3.2(d)	Internal Visual Inspection	-	Die Attach (5)
Para. 5.3.3	Bond Strength (3)	Para. 5.3.5	Flip-Chip Pull-Off (3)
Para. 5.3.4	Die Shear or Substrate Attach Strength (3)	-	Underfill (6)
-	Encapsulation	Para. 5.3.6	SAM
		Para. 5.3.2(d)	Internal Visual Inspection & Visual Inspection of Add-on Components (6)
		-	Encapsulation or Heat-spreader Attach (6)
		Para. 5.3.6	SAM (7)

TO CHART F3B – SCREENING TESTS

NOTES:

1. May be performed either as an on-wafer measurement or after dice separation.
2. Guaranteed but not tested.
3. Performed on a sample basis.
4. Only required if specified in the Detail Specification and stipulated in the Purchase Order.
5. Assembly of the Packaged Test Sublot samples for Die Components (see Para. 5.3.1).
6. If applicable to the component and/or the package selected by the Manufacturer for assembly of the Packaged Test Sublot.
7. Only applicable to Packaged Test Sublot samples which are equivalent to Flip-chip Integrated Circuit components with thermal interface material between die and lid/heat-spreader.

12.4 CHART F3 - SCREENING TESTS

12.4.1 Chart F3A - Screening Tests for Packaged Components

PACKAGED COMPONENTS FROM PRODUCTION CONTROL	
Para. 6.1	Serialisation
Para. 8.10	High Temperature Stabilisation Bake
Para. 8.11.1	Constant Acceleration (1)
Para. 8.12.1	Temperature Cycling
Para. 8.13	Particle Impact Noise Detection (PIND) (2)
Para. 8.14.1	Parameter Drift Values (Initial Measurements)
Para. 8.15	High Temperature Reverse Bias Burn-in
Para. 8.14.1	Parameter Drift Values (Final Measurements for HTRB Burn-in; Initial Measurements for Power Burn-in) (3)
Para. 8.16	Power Burn-in
Para. 8.14.1	Parameter Drift Values (Final Measurements) (3)
Para. 8.14.2	High and Low Temperatures Electrical Measurements (3)
-	Hot Solder Dip / Ball Attach / Column Attach (as applicable)
Para. 8.14.3.2	Room Temperature Electrical Measurements (3) (5)
Para. 6.4.1	Check for Lot Failure (6)
Para. 8.17	Seal (Fine and Gross Leak)
Para. 8.18	External Visual Inspection
Para. 8.19	Solderability (3) (8)
TO CHART F4A WHEN APPLICABLE	

NOTES:

1. Only applicable to Flip-chip Integrated Circuit components with Add-on Components.
2. Only applicable to components with cavities.
3. The lot failure criteria of Para. 6.4.1 apply to this test.
4. For components with hot solder dip final lead finish or ball attach or column attach, the hot solder dip, ball attach or column attach processing shall be performed at any time prior to Room Temperature Electrical Measurements during Screening Tests. The requirements for hot solder dip are specified in ESCC Basic Specification No. 23500.
5. Measurements of Parameter Drift Values need not be repeated in Room Temperature Electrical Measurements.
6. Check for Lot Failure shall take into account all electrical parameter failures that may occur during Screening Tests in accordance with Paras. 8.14.1, 8.14.2, 8.14.3.2 subsequent to HTRB Burn-in.
7. Only applicable to components with Hermetic Packages.
8. Performed on a sample basis.

12.4.2 Chart F3B - Screening Tests for Die Components

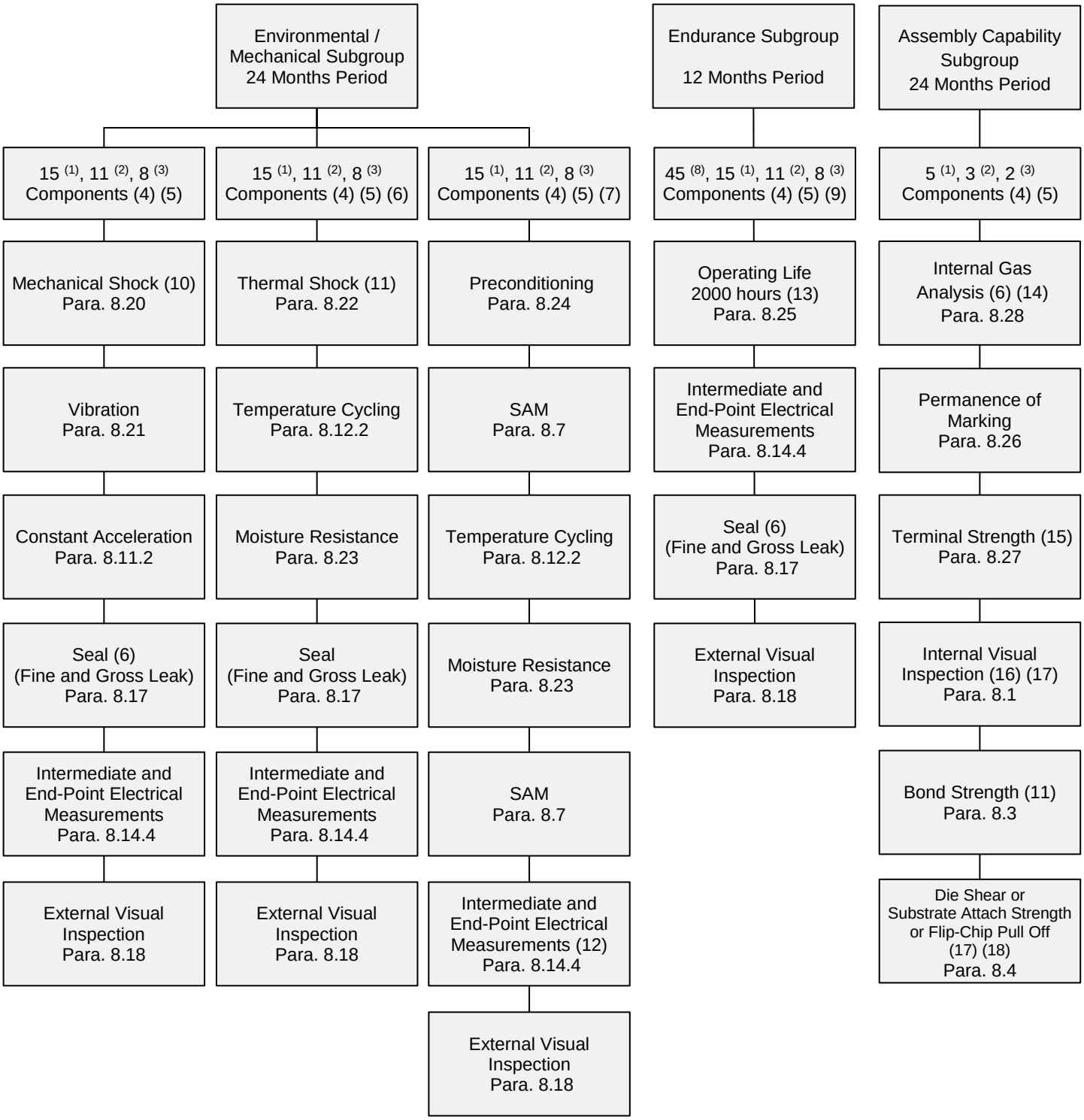
PACKAGED TEST SUBLOT FROM PRODUCTION CONTROL	
Para. 6.1	Serialisation
Para. 8.14.3.2	Room Temperature Electrical Measurements (1) (2)
Para. 8.14.2	High and Low Temperatures Electrical Measurements (1) (2) (3)
Para. 6.4.2.1	Check for Lot Failure (4)
Para. 8.14.1	Parameter Drift Values (Initial Measurements) (2) (5)
Para. 8.15	High Temperature Reverse Bias Burn-in
Para. 8.14.1	Parameter Drift Values (Final Measurements for HTRB Burn-in; Initial Measurements for Power Burn-in) (2)
Para. 8.16	Power Burn-in
Para. 8.14.1	Parameter Drift Values (Final Measurements) (2)
Para. 8.14.2	High and Low Temperatures Electrical Measurements (2)
Para. 8.14.3.2	Room Temperature Electrical Measurements (2) (6)
Para. 6.4.2.2	Check for Lot Failure (7)
TO CHART F4B WHEN APPLICABLE	

NOTES:

1. The lot failure criteria of Para. 6.4.2.1 apply to this test.
2. The lot failure criteria of Para. 6.4.2.2 apply to this test.
3. Optional at the Manufacturer's discretion.
4. Check for Lot Failure shall take into account all electrical parameter failures that may occur during Screening Tests in accordance with Paras. 8.14.2 and 8.14.3.2 prior to HTRB Burn-in.
5. Measurements of Parameter Drift Values need not be repeated if data is available from the previous Room Temperature Electrical Measurements.
6. Measurements of Parameter Drift Values need not be repeated in Room Temperature Electrical Measurements.
7. Check for Lot Failure shall take into account all electrical parameter failures that may occur at any point during Screening Tests in accordance with Paras. 8.14.1, 8.14.2 and 8.14.3.2.

12.5 CHART F4 - QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING

12.5.1 Chart F4A – Qualification, Periodic Testing and Lot Validation Testing for Packaged Components

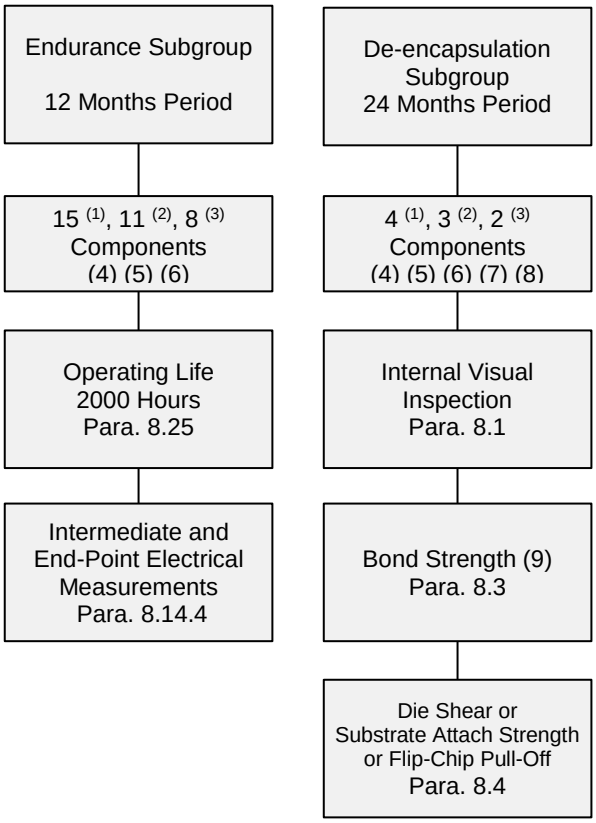


NOTES:

1. The quantity for qualification and qualification maintenance of a single type (see Para. 7.1.2.1) (Note: does not apply to Qualification Testing for single phase qualification of Wire-bonded Integrated Circuits; see note 8).

2. The quantity per type for qualification and qualification maintenance of two types selected (see Para. 7.1.2.2) (Note: does not apply to Qualification Testing for single phase qualification of Wire-bonded Integrated Circuits; see note 8).
3. The quantity per type for qualification and qualification maintenance of three or more types selected (see Para. 7.1.2.2) (Note: does not apply to Qualification Testing for single phase qualification of Wire-bonded Integrated Circuits; see note 8).
4. For distribution within the subgroups, see Para. 7.1.2 for qualification and qualification maintenance, and Para. 7.5 for Lot Validation Testing.
5. No failures are permitted.
6. Only applicable to components with Hermetic Packages.
7. Only applicable to Flip-chip Integrated Circuit components with Non-Hermetic Packages.
8. Only applicable to Qualification Testing for single phase qualification of a single type of Wire-bonded Integrated Circuit. For Qualification Testing of a family of such components, the sample sizes shall be agreed with the ESCC Executive prior to the commencement of Qualification Testing.
9. For components which have balls or columns, the tests of this subgroup may be performed without balls or columns provided preconditioning equivalent to the ball or column attach thermal profile has been applied on the samples.
10. Not applicable to Flip-chip Integrated Circuit components without Add-on Components.
11. Not applicable to Flip-chip Integrated Circuit components.
12. Unless otherwise specified in the Detail Specification, electrical measurements shall be performed at room, high and low temperatures.
13. For single phase qualification of Wire-bonded Integrated Circuits only, a 4000 hour life test may be performed; see Para. 8.25.
14. Only applicable to single phase qualification of Wire-bonded Integrated Circuits.
15. May be done at the beginning or the end of the subgroup, depending on package configuration.
16. The components shall be de-encapsulated using suitable means to facilitate Internal Visual Inspection, Bond Strength and either Die Shear or Substrate Attach Strength.
17. Not applicable to Flip-chip Integrated Circuit components with thermal interface material between die and lid/heat-spreader.
18. For Flip-chip Integrated Circuit components with Add-on Components, Shear or Substrate Attach Strength tests shall also be performed on all Add-on Components mounted in 1 sample, as specified in Para. 8.4(c).

12.5.2 Chart F4B – Qualification, Periodic Testing and Lot Validation Testing for Die Components



NOTES:

1. Single type (see Para. 7.1.2.1)
2. Per type for two types selected (see Para. 7.1.2.2)
3. Per type for three or more types selected (see Para. 7.1.2.2)
4. For distribution within the subgroups, see Para. 7.1.2 for qualification and qualification maintenance, and Para. 7.5 for Lot Validation Testing.
5. The tests of Chart F4B shall be performed on components selected from the Packaged Test Sublot, which have successfully passed the tests in Chart F3B.
6. No Failures are allowed.
7. The components shall be de-encapsulated using suitable means to facilitate Internal Visual Inspection, and Bond Strength, Die Shear, Substrate Attach Strength or Flip-chip Pull-Off, as applicable.
8. Not applicable to Packaged Test Sublot samples which are equivalent to Flip-chip Integrated Circuit components with thermal interface material between die and lid/heat-spreader.
9. Not applicable to Packaged Test Sublot samples which are equivalent to Flip-chip Integrated Circuit components.