TRANSISTORS, LOW POWER, COMPLEMENTARY NPN/PNP

BASED ON TYPE 2ST3360

ESCC Detail Specification No. 5207/009

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000
(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520700901R

- Detail Specification Reference: 5207009
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case (Note 1)	Lead/Terminal Material and Finish (Note 2)	Weight max g	Total Dose Radiation Level Letter (Note 3)
01	2ST3360	FP	G2	0.7	R [100kRAD(Si)]
02	2ST3360	FP	G4	0.7	R [100kRAD(Si)]

NOTES:

1. See Para. 1.6.
2. The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
3. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order, the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

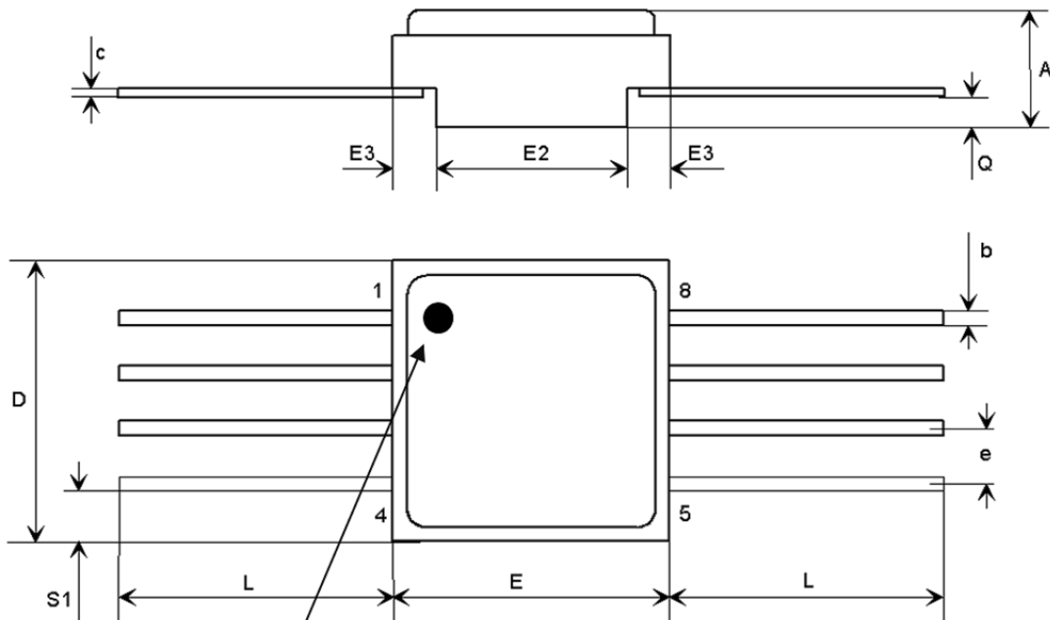
Characteristics	Symbols	Maximum Ratings		Units	Remarks
		NPN	PNP		
Collector-Base Voltage	V_{CBO}	60	-60	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	60	-60	V	
Emitter-Base Voltage	V_{EBO}	6	-6	V	
Collector Current	I_C	800	-800	mA	Continuous
Collector Peak Current	I_{CM}	4	-4	A	$t_p < 5$ms
Base Current	I_B	200	-200	mA	Continuous
Base Peak Current	I_{BM}	400	-400	mA	$t_p < 5$ms
Power Dissipation					
Single Transistor only:	P_{tot1}	0.8	0.8	W	At $T_{amb} \leq +25°C$, Note 1
Single Transistor only:	P_{tot2}	5	5		At $T_{case} \leq +25°C$, Note 1
Both Transistors:	P_{tot3}	1.4		W	At $T_{amb} \leq +25°C$, Note 1
Both Transistors:	P_{tot4}	7			At $T_{case} \leq +25°C$, Note 1
Thermal Resistance, Junction-to-Ambient	$R_{th(j-a)}$			°C/W	
Single Transistor only:		180	180		
Both Transistors:		125			
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$			°C/W	
Single Transistor only:		35	35		
Both Transistors:		25			
Junction Temperature	T_j	+200		°C	
Operating Temperature Range	T_{op}	-65 to +200		°C	
Storage Temperature Range	T_{stg}	-65 to +200		°C	
Soldering Temperature	T_{sol}	+265		°C	Note 2

NOTES:

1. For T_{amb} or T_{case} > +25ºC, derate linearly to 0W at +200ºC.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body, and the same lead shall not be resoldered until 3 minutes have elapsed.

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

FLAT PACKAGE (8 LEAD) - FP

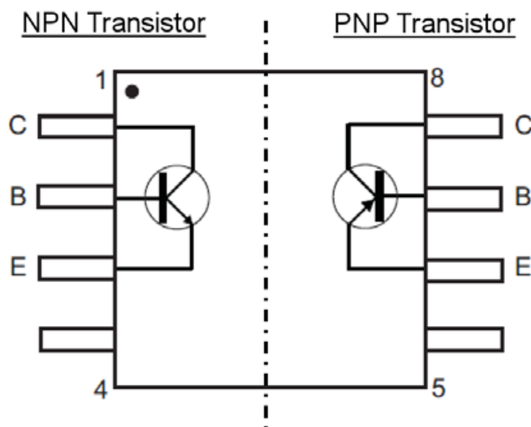


Symbols	Dimensions mm		Remarks
	Min	Max	
A	2.24	2.64	
b	0.38	0.48	All leads
c	0.1	0.16	All leads
D	6.35	6.61	
E	6.35	6.61	
E2	4.32	4.58	
E3	0.88	1.14	
e	1.27 BSC		All leads
L	6.51	7.38	All leads
Q	0.66	0.92	All leads
S1	0.92	1.32	4 places

NOTES:

1. Terminal identification is specified by reference to the black dot marked on top of the body that indicates terminal 1 (NPN Collector); see Para. 1.7.

1.7 FUNCTIONAL DIAGRAM



NOTES:

1. C = Collector; B = Base; E = Emitter.
2. The lid is connected to leads 4 and 5.

1.8 MATERIALS AND FINISHES

Materials and finishes shall be as follows:

(a) Case
The case shall be hermetically sealed and have a ceramic body with a Kovar lid.

(b) Leads/Terminals
As specified in Para. 1.4.2 Component Type Variants.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification (see Para. 1.6).
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 TERMINAL STRENGTH

The test conditions for terminal strength, tested as specified in the ESCC Generic Specification, shall be in accordance with MIL-STD-750, Test Method 2036, Test Condition E. The following details shall apply:

- Attached weight: 85gms
- Number of arcs: 3 arcs of 15°

2.4 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the Tables.

2.4.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3°C.

2.4.1.1 NPN Transistor Room Temperature Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	3001	I_C = 100µA Bias condition D Note 1	60	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	3011	I_C = 1mA Bias condition D Note 1	60	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	3026	I_E = 10µA Bias condition D Note 1	6	-	V
Collector-Base Cut-off Current	I_{CBO}	3036	V_{CB} = 60V Bias condition D Note 1	-	100	nA
Emitter-Base Cut-off Current	I_{EBO}	3061	V_{EB} = 6V Bias condition D Note 1	-	100	nA
Collector-Emitter Saturation Voltage 1	$V_{CE(sat)1}$	3071	I_C = 800mA I_B = 40mA Note 1	-	160	mV
Collector-Emitter Saturation Voltage 2	$V_{CE(sat)2}$	3071	I_C = 2A I_B = 100mA Note 1	-	380	mV
Base-Emitter Voltage (non-saturated)	$V_{BE(ON)}$	3066	V_{CE} = 2V I_C = 100mA Test condition B Note 1	600	720	mV
Forward-Current Transfer Ratio	h_{FE1}	3076	V_{CE} = 2V; I_C = 100mA Note 1	100	-	-
	h_{FE2}	3076	V_{CE} = 2V; I_C = 1A Note 1	160	400	-

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Output Capacitance	C_{obo}	3236	V_{CB} = 10V I_E = 0A f = 1MHz Note 2	-	45	pF
Switching Times			V_{CC} = 10V I_C = 800mA $I_{B(on)}$ = $-I_{B(off)}$ = 80mA Notes 2, 3			
Delay Time + Rise Time:	$t_d + t_r$	-		-	175	ns
Storage Time + Fall Time:	$t_s + t_f$	-		-	2.5	µs

2.4.1.2 PNP Transistor Room Temperature Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	3001	I_C = -100µA Bias condition D Note 1	-60	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	3011	I_C = -1mA Bias condition D Note 1	-60	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	3026	I_E = -10µA Bias condition D Note 1	-6	-	V
Collector-Base Cut-off Current	I_{CBO}	3036	V_{CB} = -60V Bias condition D Note 1	-	-100	nA
Emitter-Base Cut-off Current	I_{EBO}	3061	V_{EB} = -6V Bias condition D Note 1	-	-100	nA
Collector-Emitter Saturation Voltage 1	$V_{CE(sat)1}$	3071	I_C = -800mA I_B = -40mA Note 1	-	-180	mV
Collector-Emitter Saturation Voltage 2	$V_{CE(sat)2}$	3071	I_C = -2A I_B = -100mA Note 1	-	-440	mV
Base-Emitter Voltage (non-saturated)	$V_{BE(ON)}$	3066	V_{CE} = -2V I_C = -100mA Test condition B Note 1	-600	-720	mV
Forward-Current Transfer Ratio	h_{FE1}	3076	V_{CE} = -2V; I_C = -100mA Note 1	100	-	-
	h_{FE2}	3076	V_{CE} = -2V; I_C = -1A Note 1	160	400	-

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Output Capacitance	C_{obo}	3236	V_{CB} = -10V I_E = 0A f = 1MHz Note 2	-	45	pF
Switching Times			V_{CC} = -10V I_C = -800mA $I_{B(on)}$ = $-I_{B(off)}$ = -80mA Notes 2, 3			
Delay Time + Rise Time:	$t_d + t_r$	-		-	150	ns
Storage Time + Fall Time:	$t_s + t_f$	-		-	1	μs

2.4.2 High and Low Temperatures Electrical Measurements

2.4.2.1 NPN Transistor High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions (Note 4)	Limits		Units
				Min	Max	
Collector-Base Cut-off Current	I_{CBO}	3036	T_{amb} = +150 (+0 -5)°C V_{CB} = 60V Bias condition D	-	10	μA
Forward-Current Transfer Ratio 1	h_{FE1}	3076	T_{amb} = -55 (+5 -0)°C V_{CE} = 2V; I_C = 100mA	40	-	-

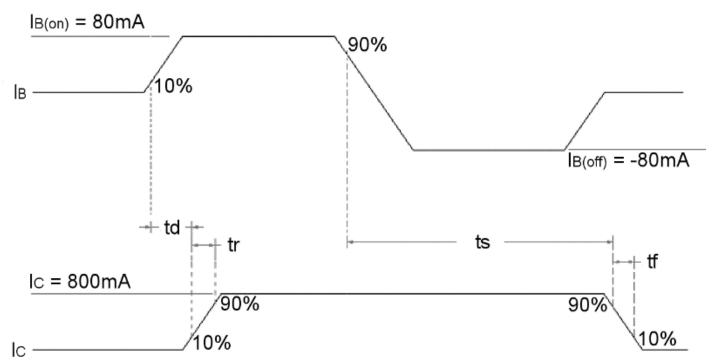
2.4.2.2 PNP Transistor High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions (Note 4)	Limits		Units
				Min	Max	
Collector-Base Cut-off Current	I_{CBO}	3036	T_{amb} = +150 (+0 -5)°C V_{CB} = -60V Bias condition D	-	-10	μA
Forward-Current Transfer Ratio 1	h_{FE1}	3076	T_{amb} = -55 (+5 -0)°C V_{CE} = -2V; I_C = -100mA	40	-	-

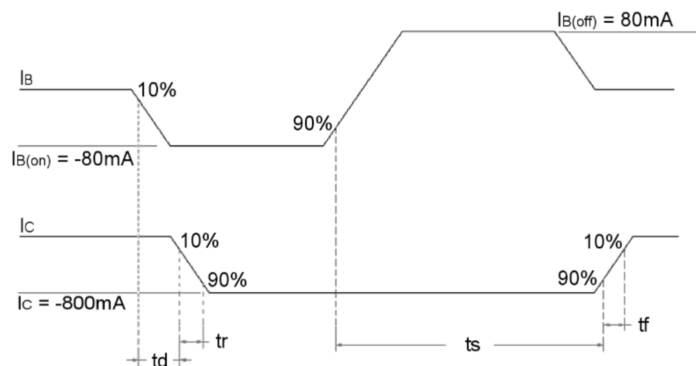
2.4.3 Notes to Electrical Measurements Tables

1. Pulse measurement: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2. For these characteristics, read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively a 100% inspection may be performed.
3. Switching Times shall be measured as follows:
    - Input waveform: see below, using pulse generator: t_r ≤ 20ns, Pulse Width = 10μs, Duty Cycle = 1%
    - Output waveform: see below, measured using sampling oscilloscope: Z_{IN} ≥ 100kΩ, C_{IN} ≤ 12pF, t_r ≤ 5ns
    - Test conditions: input voltage shall be adjusted to achieve $I_{B(on)}$ and $I_{B(off)}$, where $I_{B(on)}$ is the on-state base current and $I_{B(off)}$ is the post off-state base current.
    - Switching time waveforms:

NPN TRANSISTOR



PNP TRANSISTOR



4. Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Collector-Base Cut-off Current	I_{CBO}	±5 or (1) ±100%	-	100 (2) or -100 (3)	nA
Forward-Current Transfer Ratio 2 (4)	h_{FE2}	±15%	160	400	-

NOTES:
1. Whichever is the greater referred to initial value.
2. For the NPN transistor.
3. For the PNP transistor
4. For both NPN and PNP transistors.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	I_{CBO}	-	100 (1) or -100 (2)	nA
Forward-Current Transfer Ratio 2 (4)	h_{FE1}	160	400	-

NOTES:
1. For the NPN transistor.
2. For the PNP transistor.
3. For both NPN and PNP transistors.

2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+150 (+0 -5)	°C
Collector-Base Voltage	V_{CB}	48 (1) or -48 (2)	V
Duration	t	48 minimum	Hours

NOTES:
1. For the NPN transistor.
2. For the PNP transistor

2.8 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+20 to +50	°C
Power Dissipation	P_{tot}	As per Maximum Ratings. Derate P_{tot3} at the chosen T_{amb} using the specified $R_{th(j-a)}$.	W
Collector-Base Voltage	V_{CB}	25 (1) or -25 (2)	V

NOTES:
1. For the NPN transistor.
2. For the PNP transistor

2.9 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.8 Power Burn-in Conditions.

2.10 TOTAL DOSE RADIATION TESTING

All lots shall be irradiated in accordance with ESCC Basic Specification No. 22900, low dose rate (window 2: 36 to 360 RAD/h).

2.10.1 Bias Conditions and Total Dose Level for Total dose Radiation Testing

The following bias conditions shall be used for Total Dose Radiation Testing:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+20 ±5	°C
Bias Condition 1: Collector-Emitter Voltage	V_{CES}	≥ 80% $V_{(BR)CEO}$	V
Bias Condition 2: Collector-Emitter Voltage	V_{CES}	0	V

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

2.10.2 Electrical Measurements for Radiation Testing

Prior to irradiation testing, the devices shall have successfully met Para. 2.4.1 Room Temperature Electrical Measurements.

Unless otherwise stated, the measurements shall be performed at T_{amb} = +22 ±3°C.

Unless otherwise specified, the test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1 Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below.

(a) NPN Transistor:

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	Para. 2.4.1	Para. 2.4.1	60	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	Para. 2.4.1	Para. 2.4.1	60	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	Para. 2.4.1	Para. 2.4.1	6	-	V
Collector-Base Cut-off Current	I_{CBO}	Para. 2.4.1	Para. 2.4.1	-	200	nA
Emitter-Base Cut-off Current	I_{EBO}	Para. 2.4.1	Para. 2.4.1	-	200	nA
Collector-Emitter Saturation Voltage 1	$V_{CE(sat)1}$	Para. 2.4.1	Para. 2.4.1	-	184	mV
Collector-Emitter Saturation Voltage 2	$V_{CE(sat)2}$	Para. 2.4.1	Para. 2.4.1	-	437	mV
Base-Emitter Voltage (non-saturated)	$V_{BE(ON)}$	Para. 2.4.1	Para. 2.4.1	600	828	mV
Forward-Current Transfer Ratio (post irradiation gain calculation) (Note 1)	[h_{FE1}]	Para. 2.4.1	Para. 2.4.1	[50]	-	-
	[h_{FE2}]	Para. 2.4.1	Para. 2.4.1	[80]	400	-

(b) PNP Transistor:

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	Para. 2.4.1	Para. 2.4.1	-60	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	Para. 2.4.1	Para. 2.4.1	-60	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	Para. 2.4.1	Para. 2.4.1	-6	-	V
Collector-Base Cut-off Current	I_{CBO}	Para. 2.4.1	Para. 2.4.1	-	-200	nA
Emitter-Base Cut-off Current	I_{EBO}	Para. 2.4.1	Para. 2.4.1	-	-200	nA
Collector-Emitter Saturation Voltage 1	$V_{CE(sat)1}$	Para. 2.4.1	Para. 2.4.1	-	-207	mV
Collector-Emitter Saturation Voltage 2	$V_{CE(sat)2}$	Para. 2.4.1	Para. 2.4.1	-	-506	mV
Base-Emitter Voltage (non-saturated)	$V_{BE(ON)}$	Para. 2.4.1	Para. 2.4.1	-600	-828	mV
Forward-Current Transfer Ratio (post irradiation gain calculation) (Note 1)	$[h_{FE1}]$	Para. 2.4.1	Para. 2.4.1	[50]	-	-
	$[h_{FE2}]$	Para. 2.4.1	Para. 2.4.1	[80]	400	-

NOTES:

1. The post-irradiation gain calculation of $[h_{FE}]$, made using h_{FE} measurements from prior to and on completion of irradiation testing and after each annealing step if any, shall be as specified in MIL-STD-750 Method 1019.

APPENDIX A

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.1.1 Deviations from the Generic Specification: Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.
Para. 2.4.2 High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.