



**INTEGRATED CIRCUITS, SILICON MONOLITHIC, HCMOS  
OCTAL D-TYPE EDGE TRIGGERED FLIP-FLOP WITH  
CLEAR AND FULLY BUFFERED OUTPUTS**

**BASED ON TYPE 54HC273**

**ESCC Detail Specification No. 9203/053**

|         |          |
|---------|----------|
| Issue 5 | May 2019 |
|---------|----------|



### **LEGAL DISCLAIMER AND COPYRIGHT**

European Space Agency, Copyright © 2019. All rights reserved.

The European Space Agency disclaims any liability or responsibility, to any person or entity, with respect to any loss or damage caused, or alleged to be caused, directly or indirectly by the use and application of this ESCC publication.

This publication, without the prior permission of the European Space Agency and provided that it is not used for a commercial purpose, may be:

- copied in whole, in any medium, without alteration or modification.
- copied in part, in any medium, provided that the ESCC document identification, comprising the ESCC symbol, document number and document issue, is removed.

**DOCUMENTATION CHANGE NOTICE**

(Refer to <https://escies.org> for ESCC DCR content)

| DCR No.                        | CHANGE DESCRIPTION                                     |
|--------------------------------|--|
| <a href="#">1184 1200 1258</a> | Specification upissued to incorporate changes per DCR. |

**TABLE OF CONTENTS**

|       |   |    |
|-------|---|----|
| 1     | GENERAL   | 5  |
| 1.1   | SCOPE   | 5  |
| 1.2   | APPLICABLE DOCUMENTS  | 5  |
| 1.3   | TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS                  | 5  |
| 1.4   | THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS                 | 5  |
| 1.4.1 | The ESCC Component Number   | 5  |
| 1.4.2 | Component Type Variants   | 5  |
| 1.5   | MAXIMUM RATINGS   | 6  |
| 1.6   | HANDLING PRECAUTIONS  | 6  |
| 1.7   | PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION                       | 7  |
| 1.7.1 | Flat Package (FP) - 20 Pin  | 7  |
| 1.7.2 | Dual-in-line Package (DIP) - 20 Pin                                   | 8  |
| 1.7.3 | Notes to Para. 1.7 Physical Dimensions and Terminal Identification    | 9  |
| 1.8   | FUNCTIONAL DIAGRAM  | 9  |
| 1.9   | PIN ASSIGNMENT  | 10 |
| 1.10  | TRUTH TABLE   | 10 |
| 1.11  | PROTECTION NETWORKS   | 11 |
| 2     | REQUIREMENTS  | 11 |
| 2.1   | GENERAL   | 11 |
| 2.1.1 | Deviations from the Generic Specification                             | 11 |
| 2.2   | MARKING   | 11 |
| 2.3   | ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES            | 12 |
| 2.3.1 | Room Temperature Electrical Measurements                              | 12 |
| 2.3.2 | High and Low Temperatures Electrical Measurements                     | 14 |
| 2.3.3 | Notes to Electrical Measurement Tables                                | 16 |
| 2.4   | PARAMETER DRIFT VALUES  | 17 |
| 2.5   | INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS                    | 17 |
| 2.6   | HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS                      | 18 |
| 2.6.1 | N-Channel HTRB  | 18 |
| 2.6.2 | P-Channel HTRB  | 18 |
| 2.7   | POWER BURN-IN CONDITIONS  | 19 |
| 2.8   | OPERATING LIFE CONDITIONS   | 19 |
| 2.9   | TOTAL DOSE RADIATION TESTING  | 19 |
| 2.9.1 | Bias Conditions and Total Dose Level for Total Dose Radiation Testing | 19 |
| 2.9.2 | Electrical Measurements for Total Dose Radiation Testing              | 20 |
|       | APPENDIX 'A'  | 21 |

## 1 GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

### 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. [9000](#).
- (b) [MIL-STD-883](#), Test Methods and Procedures for Microelectronics.

### 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. [21300](#) shall apply.

### 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

#### 1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920305301F

- Detail Specification Reference: 9203053
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: F (as required)

#### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

| Variant Number | Based on Type | Case | Terminal Material and Finish | Weight max g | Total Dose Radiation Level Letter |
|----------------|---------------|------|------------------------------|--------------|-----------------------------------|
| 01             | 54HC273       | FP   | G2                           | 0.9          | F [50kRAD(Si)]                    |
| 02             | 54HC273       | FP   | G4                           | 0.9          | F [50kRAD(Si)]                    |
| 03             | 54HC273       | DIP  | G2                           | 3.2          | F [50kRAD(Si)]                    |
| 04             | 54HC273       | DIP  | G4                           | 3.2          | F [50kRAD(Si)]                    |

The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. [23500](#).

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. [22900](#). If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

### 1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

| Characteristics                       | Symbols    | Maximum Ratings      | Units | Remarks    |
|---------------------------------------|------------|----------------------|-------|------------|
| Supply Voltage                        | $V_{DD}$   | -0.5 to 7            | V     | Note 1     |
| Input Voltage                         | $V_{IN}$   | -0.5 to $V_{DD}+0.5$ | V     | Notes 1, 2 |
| Output Voltage                        | $V_{OUT}$  | -0.5 to $V_{DD}+0.5$ | V     | Notes 1, 3 |
| Device Power Dissipation (Continuous) | $P_D$      | 300                  | mW    | Note 4     |
| Supply Current                        | $I_{DDop}$ | 50                   | mA    |            |
| Operating Temperature Range           | $T_{op}$   | -55 to +125          | °C    | $T_{amb}$  |
| Storage Temperature Range             | $T_{stg}$  | -65 to +150          | °C    |            |
| Soldering Temperature                 | $T_{sol}$  | +265                 | °C    | Note 5     |

#### **NOTES:**

1. Device is functional for  $2V \leq V_{DD} \leq 6V$ .
2. Input current limited to  $I_{IC} = \pm 20mA$ .
3. Output current limited to  $I_{OUT} = \pm 25mA$ .
4. The maximum device dissipation is determined by  $I_{DDop} \text{ max } (50mA) \times 6V$ .
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

### 1.6 HANDLING PRECAUTIONS

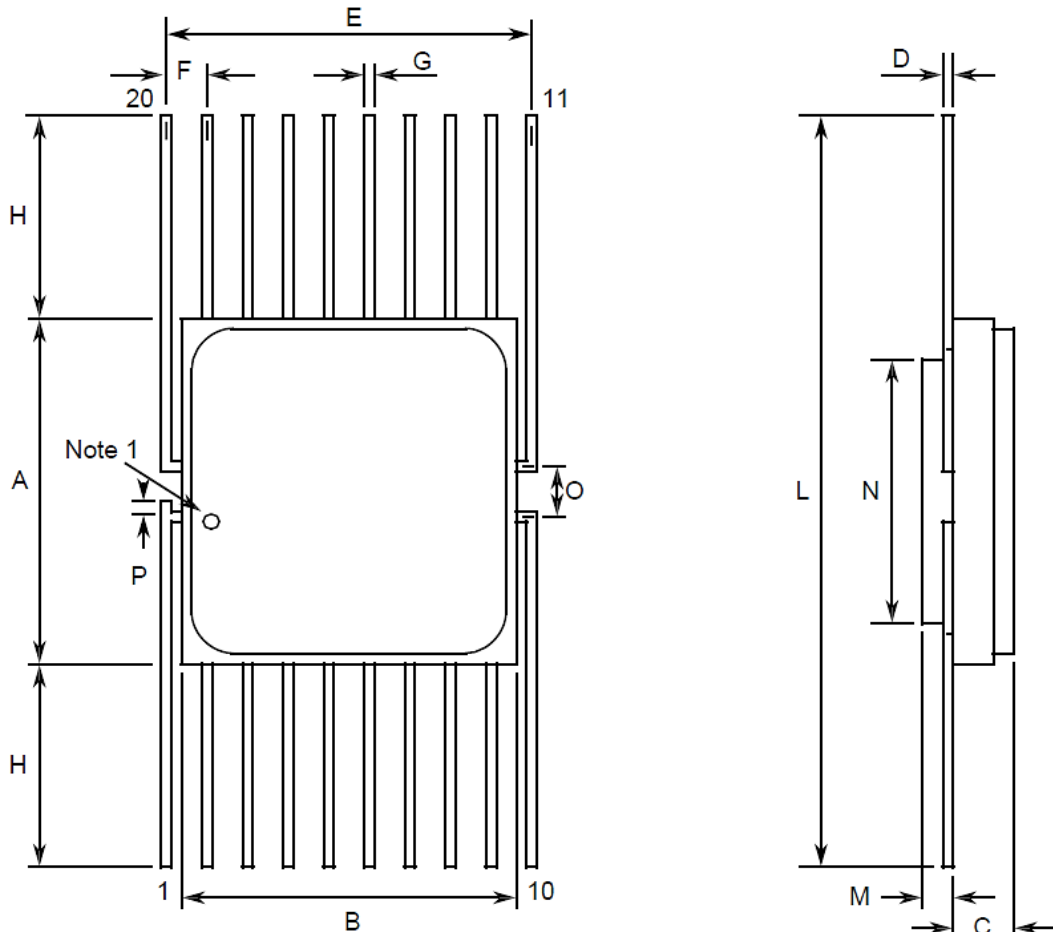
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. [23800](#) with a Minimum Critical Path Failure Voltage of 2500 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Consolidated Notes are given in Para. 1.7.3.

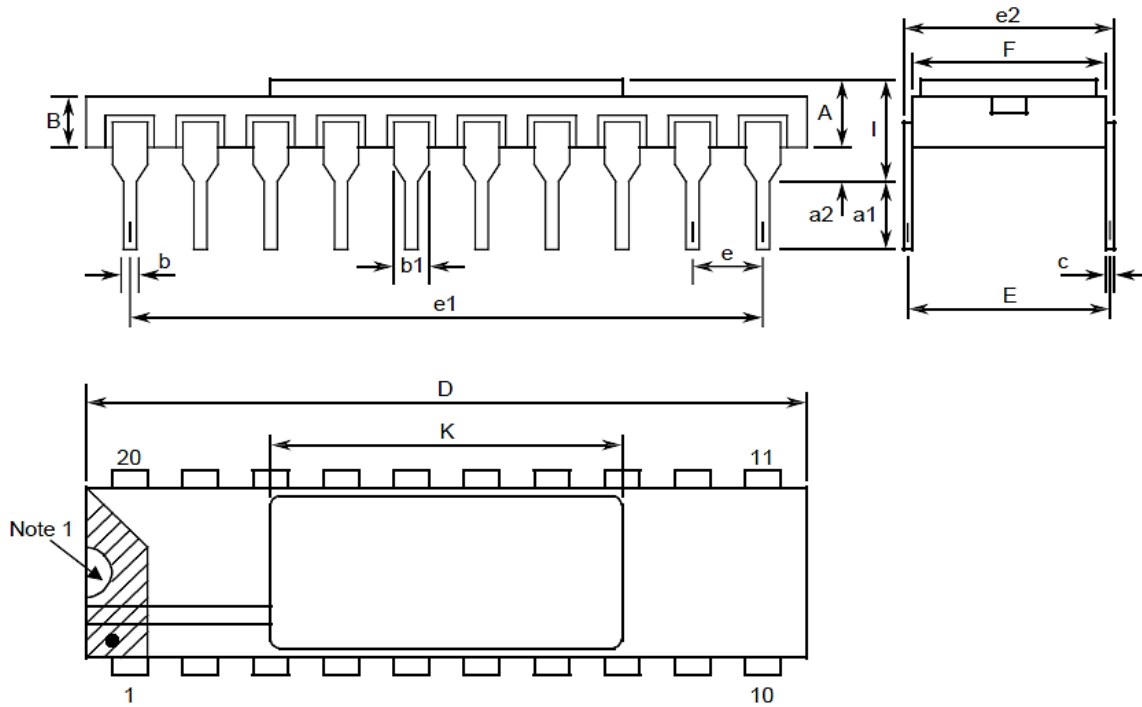
1.7.1 Flat Package (FP) - 20 Pin



| Symbols | Dimensions mm |       | Notes |
|---------|---------------|-------|-------|
|         | Min           | Max   |       |
| A       | 9.98          | 10.34 |       |
| B       | 9.98          | 10.34 |       |
| C       | 1.45          | 1.78  |       |
| D       | 0.1           | 0.18  | 5     |
| E       | 11.3          | 11.56 |       |
| F       | 1.27 BSC      |       | 3, 6  |
| G       | 0.38          | 0.48  | 5     |
| H       | 7.24          | 8.16  | 5     |
| L       | 24.46         | 26.67 |       |
| M       | 0.45          | 0.55  |       |

| Symbols | Dimensions mm |      | Notes |
|---------|---------------|------|-------|
|         | Min           | Max  |       |
| N       | 7.87 TYPICAL  |      |       |
| O       | 1.27 BSC      |      |       |
| P       | 0.1           | 0.25 |       |

1.7.2 Dual-in-line Package (DIP) - 20 Pin



| Symbols | Dimensions mm |       | Notes |
|---------|---------------|-------|-------|
|         | Min           | Max   |       |
| A       | 2.1           | 2.72  |       |
| a1      | 3             | 3.7   |       |
| a2      | 0.63          | 1.14  | 2     |
| B       | 1.93          | 2.39  |       |
| b       | 0.4           | 0.5   | 5     |
| b1      | 1.27 TYPICAL  |       | 5     |
| c       | 0.2           | 0.3   | 5     |
| D       | 25.14         | 25.65 |       |
| E       | 7.36          | 7.87  |       |
| e       | 2.54 BSC      |       | 4, 6  |
| e1      | 22.73         | 22.99 |       |

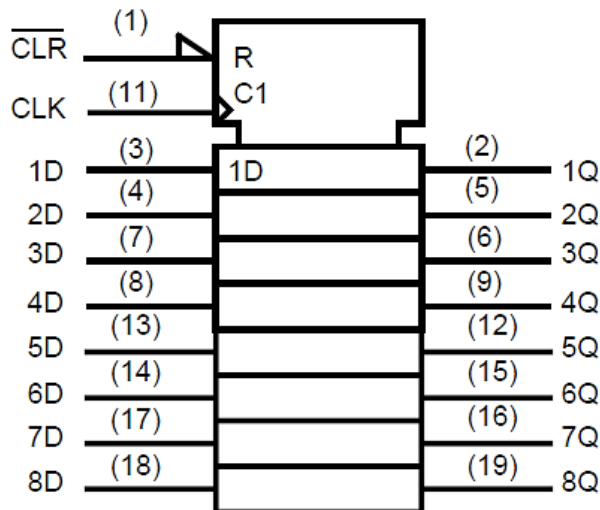


| Symbols | Dimensions mm |       | Notes |
|---------|---------------|-------|-------|
|         | Min           | Max   |       |
| e2      | 7.62          | 8.12  |       |
| F       | 7.11          | 7.62  |       |
| I       | -             | 3.86  |       |
| K       | 11.3          | 11.56 |       |

1.7.3 Notes to Para. 1.7 Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within  $\pm 0.13\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within  $\pm 0.25\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 18 spaces.

1.8 FUNCTIONAL DIAGRAM



**NOTES:**

1. The package lid for all packages is not connected to any terminal.

1.9 PIN ASSIGNMENT

| Pin | Function                              | Pin | Function          |
|-----|---------------------------------------|-----|-------------------|
| 1   | $\overline{\text{CLR}}$ Input (Clear) | 11  | CLK Input (Clock) |
| 2   | 1Q Output                             | 12  | 5Q Output         |
| 3   | 1D Input (Data)                       | 13  | 5D Input (Data)   |
| 4   | 2D Input (Data)                       | 14  | 6D Input (Data)   |
| 5   | 2Q Output                             | 15  | 6Q Output         |
| 6   | 3Q Output                             | 16  | 7Q Output         |
| 7   | 3D Input (Data)                       | 17  | 7D Input (Data)   |
| 8   | 4D Input (Data)                       | 18  | 8D Input (Data)   |
| 9   | 4Q Output                             | 19  | 8Q Output         |
| 10  | V <sub>SS</sub>                       | 20  | V <sub>DD</sub>   |

1.10 TRUTH TABLE

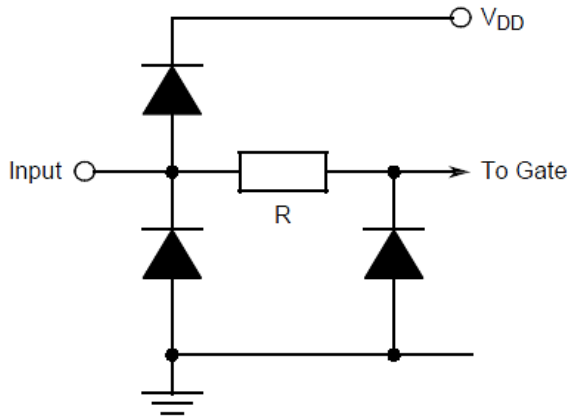
1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
2.  $\uparrow$  = Transition, Low to High.
3. Q<sub>n</sub> = The Level of Q before the indicated steady-state input conditions are established.

EACH FLIP-FLOP

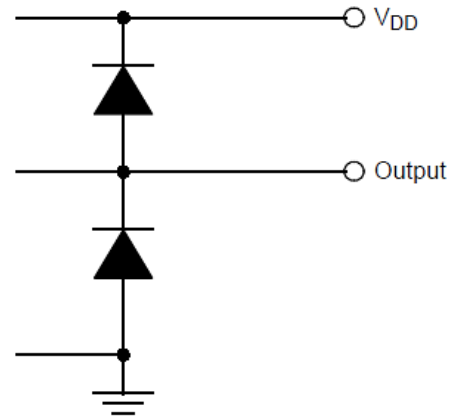
| INPUTS                  |   |            | OUTPUT<br>Q    | FUNCTION  |
|-------------------------|---|------------|----------------|-----------|
| $\overline{\text{CLR}}$ | D | CLK        |                |           |
| L                       | X | X          | L              | CLEAR     |
| H                       | L | $\uparrow$ | L              | -         |
| H                       | H | $\uparrow$ | H              | -         |
| H                       | X | L          | Q <sub>n</sub> | No Change |

## 1.11 PROTECTION NETWORKS

### INPUT PROTECTION



### OUTPUT PROTECTION



## 2 REQUIREMENTS

### 2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

#### 2.1.1 Deviations from the Generic Specification

None.

### 2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification (see Para. 1.7).
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number (see Para. 1.4.1).
- (d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given in Para. 2.3.3.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

| Characteristics               | Symbols   | MIL-STD-883<br>Test Method | Test Conditions<br>Note 1  | Limits |     | Units |
|-------------------------------|-----------|----------------------------|--|--------|-----|-------|
|                               |           |                            |  | Min    | Max |       |
| Functional Test 1             | -         | 3014                       | Verify Truth Table<br>without Load<br>$V_{IL} = 0.3V, V_{IH} = 1.5V$<br>$V_{DD} = 2V, V_{SS} = 0V$<br>$t_r < 1\mu s$ , Note 2          | -      | -   | -     |
| Functional Test 2             | -         | 3014                       | Verify Truth Table<br>without Load<br>$V_{IL} = 0.9V, V_{IH} = 3.15V$<br>$V_{DD} = 4.5V, V_{SS} = 0V$<br>$t_r = t_f < 500ns$<br>Note 2 | -      | -   | -     |
| Functional Test 3             | -         | 3014                       | Verify Truth Table<br>without Load<br>$V_{IL} = 1.2V, V_{IH} = 4.2V$<br>$V_{DD} = 6V, V_{SS} = 0V$<br>$t_r = t_f < 400ns$<br>Note 2    | -      | -   | -     |
| Quiescent Current             | $I_{DD}$  | 3005                       | $V_{IL} = 0V, V_{IH} = 6V$<br>$V_{DD} = 6V, V_{SS} = 0V$<br>All Outputs Open<br>Note 3   | -      | 400 | nA    |
| Low Level Input<br>Current    | $I_{IL}$  | 3009                       | $V_{IN}$ (Under Test) = 0V<br>$V_{IN}$ (Remaining Inputs)<br>= 6V<br>$V_{DD} = 6V, V_{SS} = 0V$  | -      | -50 | nA    |
| High Level Input<br>Current   | $I_{IH}$  | 3010                       | $V_{IN}$ (Under Test) = 6V<br>$V_{IN}$ (Remaining Inputs)<br>= 0V<br>$V_{DD} = 6V, V_{SS} = 0V$  | -      | 50  | nA    |
| Low Level Output<br>Voltage 1 | $V_{OL1}$ | 3007                       | $V_{IL} = 0.3V, V_{IH} = 1.5V,$<br>$I_{OL} = 20\mu A$<br>$V_{DD} = 2V, V_{SS} = 0V$  | -      | 100 | mV    |
| Low Level Output<br>Voltage 2 | $V_{OL2}$ | 3007                       | $V_{IL} = 0.9V, V_{IH} = 3.15V,$<br>$I_{OL} = 20\mu A$<br>$V_{DD} = 4.5V, V_{SS} = 0V$   | -      | 100 | mV    |
| Low Level Output<br>Voltage 3 | $V_{OL3}$ | 3007                       | $V_{IL} = 1.2V, V_{IH} = 4.2V,$<br>$I_{OL} = 20\mu A$<br>$V_{DD} = 6V, V_{SS} = 0V$  | -      | 100 | mV    |
| Low Level Output<br>Voltage 4 | $V_{OL4}$ | 3007                       | $V_{IL} = 0.9V, V_{IH} = 3.15V,$<br>$I_{OL} = 4mA$<br>$V_{DD} = 4.5V, V_{SS} = 0V$   | -      | 260 | mV    |

| Characteristics                           | Symbols          | MIL-STD-883<br>Test Method | Test Conditions<br>Note 1  | Limits |       | Units |
|---|------------------|----------------------------|--|--------|-------|-------|
|   |                  |                            |  | Min    | Max   |       |
| Low Level Output Voltage 5                | V <sub>OL5</sub> | 3007                       | V <sub>IL</sub> = 1.2V, V <sub>IH</sub> = 4.2V,<br>I <sub>OL</sub> = 5.2mA<br>V <sub>DD</sub> = 6V, V <sub>SS</sub> = 0V   | -      | 260   | mV    |
| High Level Output Voltage 1               | V <sub>OH1</sub> | 3006                       | V <sub>IL</sub> = 0.3V, V <sub>IH</sub> = 1.5V,<br>I <sub>OH</sub> = -20μA<br>V <sub>DD</sub> = 2V, V <sub>SS</sub> = 0V   | 1.9    | -     | V     |
| High Level Output Voltage 2               | V <sub>OH2</sub> | 3006                       | V <sub>IL</sub> = 0.9V, V <sub>IH</sub> = 3.15V,<br>I <sub>OH</sub> = -20μA<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V  | 4.4    | -     | V     |
| High Level Output Voltage 3               | V <sub>OH3</sub> | 3006                       | V <sub>IL</sub> = 1.2V, V <sub>IH</sub> = 4.2V,<br>I <sub>OH</sub> = -20μA<br>V <sub>DD</sub> = 6V, V <sub>SS</sub> = 0V   | 5.9    | -     | V     |
| High Level Output Voltage 4               | V <sub>OH4</sub> | 3006                       | V <sub>IL</sub> = 0.9V, V <sub>IH</sub> = 3.15V,<br>I <sub>OH</sub> = -4mA<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V   | 3.98   | -     | V     |
| High Level Output Voltage 5               | V <sub>OH5</sub> | 3006                       | V <sub>IL</sub> = 1.2V, V <sub>IH</sub> = 4.2V,<br>I <sub>OH</sub> = -5.2mA<br>V <sub>DD</sub> = 6V, V <sub>SS</sub> = 0V  | 5.48   | -     | V     |
| Threshold Voltage N-Channel               | V <sub>THN</sub> | -                          | CLK Input at Ground<br>All Other Inputs:<br>V <sub>IN</sub> = 5V<br>V <sub>DD</sub> = 5V, I <sub>SS</sub> = -10μA  | -0.45  | -1.45 | V     |
| Threshold Voltage P-Channel               | V <sub>THP</sub> | -                          | CLK Input at Ground<br>All Other Inputs:<br>V <sub>IN</sub> = -5V<br>V <sub>SS</sub> = -5V, I <sub>DD</sub> = 10μA   | 0.45   | 1.35  | V     |
| Input Clamp Voltage 1, to V <sub>SS</sub> | V <sub>IC1</sub> | -                          | I <sub>IN</sub> (Under Test) =<br>-100μA<br>V <sub>DD</sub> = Open, V <sub>SS</sub> = 0V<br>All Other Pins Open  | -400   | -900  | mV    |
| Input Clamp Voltage 2, to V <sub>DD</sub> | V <sub>IC2</sub> | -                          | I <sub>IN</sub> (Under Test) =<br>100μA<br>V <sub>DD</sub> = 0V, V <sub>SS</sub> = Open<br>All Other Pins Open   | 400    | 900   | mV    |
| Input Capacitance                         | C <sub>IN</sub>  | 3012                       | V <sub>IN</sub> (Not Under Test) =<br>0V<br>V <sub>DD</sub> = V <sub>SS</sub> = 0V<br>f = 100kHz to 1MHz<br>Note 4   | -      | 10    | pF    |
| Propagation Delay Low to High, CLK to 1Q  | t <sub>PLH</sub> | 3003                       | V <sub>IN</sub> (Under Test) = Pulse Generator<br>V <sub>IN</sub> (Remaining Inputs) = Truth Table<br>V <sub>IL</sub> = 0V, V <sub>IH</sub> = 4.5V<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V<br>Note 5 | -      | 36    | ns    |

| Characteristics                                  | Symbols           | MIL-STD-883<br>Test Method | Test Conditions<br>Note 1  | Limits |     | Units |
|--|-------------------|----------------------------|--|--------|-----|-------|
|  |                   |                            |  | Min    | Max |       |
| Propagation Delay<br>High to Low 1,<br>CLK to 1Q | t <sub>PHL1</sub> | 3003                       | V <sub>IN</sub> (Under Test) = Pulse<br>Generator<br>V <sub>IN</sub> (Remaining Inputs)<br>= Truth Table<br>V <sub>IL</sub> = 0V, V <sub>IH</sub> = 4.5V<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V<br>Note 5 | -      | 36  | ns    |
| Propagation Delay<br>High to Low 2,<br>CLR to 8Q | t <sub>PHL2</sub> | 3003                       | V <sub>IN</sub> (Under Test) = Pulse<br>Generator<br>V <sub>IN</sub> (Remaining Inputs)<br>= Truth Table<br>V <sub>IL</sub> = 0V, V <sub>IH</sub> = 4.5V<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V<br>Note 5 | -      | 36  | ns    |
| Transition Time<br>Low to High,<br>1Q            | t <sub>TLH</sub>  | 3004                       | V <sub>IN</sub> (Under Test) = Pulse<br>Generator<br>V <sub>IN</sub> (Remaining Inputs)<br>= Truth Table<br>V <sub>IL</sub> = 0V, V <sub>IH</sub> = 4.5V<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V<br>Note 5 | -      | 15  | ns    |
| Transition Time<br>High to Low,<br>1Q            | t <sub>THL</sub>  | 3004                       | V <sub>IN</sub> (Under Test) = Pulse<br>Generator<br>V <sub>IN</sub> (Remaining Inputs)<br>= Truth Table<br>V <sub>IL</sub> = 0V, V <sub>IH</sub> = 4.5V<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V<br>Note 5 | -      | 15  | ns    |
| Maximum Clock<br>Frequency                       | f <sub>CLK</sub>  | -                          | Clock = Pulse<br>Generator<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V<br>Notes 6, 7   | 27     | -   | MHZ   |

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T<sub>amb</sub> = +125 (+0 -5)°C and T<sub>amb</sub> = -55 (+5 -0)°C.

| Characteristics   | Symbols | MIL-STD-883<br>Test Method | Test Conditions<br>Note 1  | Limits |     | Units |
|-------------------|---------|----------------------------|--|--------|-----|-------|
|                   |         |                            |  | Min    | Max |       |
| Functional Test 1 | -       | 3014                       | Verify Truth Table<br>without Load<br>V <sub>IL</sub> = 0.3V, V <sub>IH</sub> = 1.5V<br>V <sub>DD</sub> = 2V, V <sub>SS</sub> = 0V<br>t <sub>r</sub> < 1μs, Note 2                         | -      | -   | -     |
| Functional Test 2 | -       | 3014                       | Verify Truth Table<br>without Load<br>V <sub>IL</sub> = 0.9V, V <sub>IH</sub> = 3.15V<br>V <sub>DD</sub> = 4.5V, V <sub>SS</sub> = 0V<br>t <sub>r</sub> = t <sub>f</sub> < 500ns<br>Note 2 | -      | -   | -     |

| Characteristics                | Symbols   | MIL-STD-883<br>Test Method | Test Conditions<br>Note 1   | Limits |     | Units   |
|--------------------------------|-----------|----------------------------|---|--------|-----|---------|
|                                |           |                            |   | Min    | Max |         |
| Functional Test 3              | -         | 3014                       | Verify Truth Table<br>without Load<br>$V_{IL} = 1.2V, V_{IH} = 4.2V$<br>$V_{DD} = 6V, V_{SS} = 0V$<br>$t_r = t_f < 400ns$<br>Note 2 | -      | -   | -       |
| Quiescent Current              | $I_{DD}$  | 3005                       | $V_{IL} = 0V, V_{IH} = 6V$<br>$V_{DD} = 6V, V_{SS} = 0V$<br>All Outputs Open<br>Note 3  | -      | 8   | $\mu A$ |
| Low Level Input<br>Current     | $I_{IL}$  | 3009                       | $V_{IN}$ (Under Test) = 0V<br>$V_{IN}$ (Remaining Inputs)<br>= 6V<br>$V_{DD} = 6V, V_{SS} = 0V$                                     | -      | -1  | $\mu A$ |
| High Level Input<br>Current    | $I_{IH}$  | 3010                       | $V_{IN}$ (Under Test) = 6V<br>$V_{IN}$ (Remaining Inputs)<br>= 0V<br>$V_{DD} = 6V, V_{SS} = 0V$                                     | -      | 1   | $\mu A$ |
| Low Level Output<br>Voltage 1  | $V_{OL1}$ | 3007                       | $V_{IL} = 0.3V, V_{IH} = 1.5V,$<br>$I_{OL} = 20\mu A$<br>$V_{DD} = 2V, V_{SS} = 0V$   | -      | 100 | mV      |
| Low Level Output<br>Voltage 2  | $V_{OL2}$ | 3007                       | $V_{IL} = 0.9V, V_{IH} = 3.15V,$<br>$I_{OL} = 20\mu A$<br>$V_{DD} = 4.5V, V_{SS} = 0V$  | -      | 100 | mV      |
| Low Level Output<br>Voltage 3  | $V_{OL3}$ | 3007                       | $V_{IL} = 1.2V, V_{IH} = 4.2V,$<br>$I_{OL} = 20\mu A$<br>$V_{DD} = 6V, V_{SS} = 0V$   | -      | 100 | mV      |
| Low Level Output<br>Voltage 4  | $V_{OL4}$ | 3007                       | $V_{IL} = 0.9V, V_{IH} = 3.15V,$<br>$I_{OL} = 4mA$<br>$V_{DD} = 4.5V, V_{SS} = 0V$  | -      | 400 | mV      |
| Low Level Output<br>Voltage 5  | $V_{OL5}$ | 3007                       | $V_{IL} = 1.2V, V_{IH} = 4.2V,$<br>$I_{OL} = 5.2mA$<br>$V_{DD} = 6V, V_{SS} = 0V$   | -      | 400 | mV      |
| High Level Output<br>Voltage 1 | $V_{OH1}$ | 3006                       | $V_{IL} = 0.3V, V_{IH} = 1.5V,$<br>$I_{OH} = -20\mu A$<br>$V_{DD} = 2V, V_{SS} = 0V$  | 1.9    | -   | V       |
| High Level Output<br>Voltage 2 | $V_{OH2}$ | 3006                       | $V_{IL} = 0.9V, V_{IH} = 3.15V,$<br>$I_{OH} = -20\mu A$<br>$V_{DD} = 4.5V, V_{SS} = 0V$   | 4.4    | -   | V       |
| High Level Output<br>Voltage 3 | $V_{OH3}$ | 3006                       | $V_{IL} = 1.2V, V_{IH} = 4.2V,$<br>$I_{OH} = -20\mu A$<br>$V_{DD} = 6V, V_{SS} = 0V$  | 5.9    | -   | V       |
| High Level Output<br>Voltage 4 | $V_{OH4}$ | 3006                       | $V_{IL} = 0.9V, V_{IH} = 3.15V,$<br>$I_{OH} = -4mA$<br>$V_{DD} = 4.5V, V_{SS} = 0V$   | 3.7    | -   | V       |
| High Level Output<br>Voltage 5 | $V_{OH5}$ | 3006                       | $V_{IL} = 1.2V, V_{IH} = 4.2V,$<br>$I_{OH} = -5.2mA$<br>$V_{DD} = 6V, V_{SS} = 0V$  | 5.2    | -   | V       |

| Characteristics                    | Symbols   | MIL-STD-883<br>Test Method | Test Conditions<br>Note 1  | Limits |      | Units |
|------------------------------------|-----------|----------------------------|--|--------|------|-------|
|                                    |           |                            |  | Min    | Max  |       |
| Input Clamp Voltage 1, to $V_{SS}$ | $V_{IC1}$ | -                          | $I_{IN}$ (Under Test) =<br>-100 $\mu$ A<br>$V_{DD}$ = Open, $V_{SS}$ = 0V<br>All Other Pins Open | -0.1   | -1.2 | V     |
| Input Clamp Voltage 2, to $V_{DD}$ | $V_{IC2}$ | -                          | $I_{IN}$ (Under Test) =<br>100 $\mu$ A<br>$V_{DD}$ = 0V, $V_{SS}$ = Open<br>All Other Pins Open  | 0.1    | 1.2  | V     |

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be  $V_{IN} = V_{SS}$  or  $V_{DD}$  and outputs not under test shall be open.
2. Functional tests shall be performed with  $f = 10\text{kHz}$  (min). The maximum time to output comparator strobe = 30 $\mu$ s.
3. Quiescent Current shall be tested using the following input conditions:
  - (a) CLK = Low to High transition; all other inputs =  $V_{IH}$
  - (b) CLK = Low to High transition; all other inputs =  $V_{IL}$
4. Guaranteed but not tested.
5. Measurements shall be performed as a go-no-go test on a 100% basis. Read and record measurements shall be performed on a sample of 5 components.  
 The pulse generator shall have the following characteristics:  
 $V_{GEN} = 0$  to  $V_{DD}$ ;  $f_{GEN} = 1\text{MHz}$  minimum;  $t_r$  and  $t_f \leq 6\text{ns}$  (10% to 90%); duty cycle = 50%;  $Z_{out} = 50\Omega$ . Output load capacitance  $C_L = 50\text{pF} \pm 5\%$  including scope probe, wiring and stray capacitance without component in the test fixture and output load resistance  $R_L = 1\text{k}\Omega \pm 5\%$ .  
 Propagation delay shall be measured referenced to the 50% input and output voltages.  
 Transition time shall be measured referenced to the 10% and 90% output voltage.
6. Read and record measurements shall be performed on a sample of 5 components with 0 failures permitted.
7. A pulse, having the following conditions, shall be applied to clock input:  $V_P = 0\text{V}$  to  $V_{DD}$ . Maximum clock frequency  $f_{CLK}$  requirement shall be considered as met if proper output state changes occur with the pulse repetition rate set to that given in the Limits column.



2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics             | Symbols   | Limits               |          |       | Units |
|-----------------------------|-----------|----------------------|----------|-------|-------|
|                             |           | Drift Value $\Delta$ | Absolute |       |       |
|                             |           |                      | Min      | Max   |       |
| Quiescent Current           | $I_{DD}$  | $\pm 120$            | -        | 400   | nA    |
| Low Level Input Current     | $I_{IL}$  | $\pm 20$             | -        | -50   | nA    |
| High Level Input Current    | $I_{IH}$  | $\pm 20$             | -        | 50    | nA    |
| Low Level Output Voltage 4  | $V_{OL4}$ | $\pm 26$             | -        | 260   | mV    |
| High Level Output Voltage 4 | $V_{OH4}$ | $\pm 0.2$            | 3.98     | -     | V     |
| Threshold Voltage N-Channel | $V_{THN}$ | $\pm 0.3$            | -0.45    | -1.45 | V     |
| Threshold Voltage P-Channel | $V_{THP}$ | $\pm 0.3$            | 0.45     | 1.35  | V     |

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics          | Symbols  | Limits               |          |     | Units |
|--------------------------|----------|----------------------|----------|-----|-------|
|                          |          | Drift Value $\Delta$ | Absolute |     |       |
|                          |          |                      | Min      | Max |       |
| Functional Test 1        | -        | -                    | -        | -   | -     |
| Functional Test 2        | -        | -                    | -        | -   | -     |
| Functional Test 3        | -        | -                    | -        | -   | -     |
| Quiescent Current        | $I_{DD}$ | $\pm 120$            | -        | 400 | nA    |
| Low Level Input Current  | $I_{IL}$ | $\pm 20$             | -        | -50 | nA    |
| High Level Input Current | $I_{IH}$ | $\pm 20$             | -        | 50  | nA    |

| Characteristics             | Symbols          | Limits               |          |       | Units |
|-----------------------------|------------------|----------------------|----------|-------|-------|
|                             |                  | Drift Value $\Delta$ | Absolute |       |       |
|                             |                  |                      | Min      | Max   |       |
| Low Level Output Voltage 4  | V <sub>OL4</sub> | ±26                  | -        | 260   | mV    |
| Low Level Output Voltage 5  | V <sub>OL5</sub> | ±26                  | -        | 260   | mV    |
| High Level Output Voltage 4 | V <sub>OH4</sub> | ±0.2                 | 3.98     | -     | V     |
| High Level Output Voltage 5 | V <sub>OH5</sub> | ±0.2                 | 5.48     | -     | V     |
| Threshold Voltage N-Channel | V <sub>THN</sub> | ±0.3                 | -0.45    | -1.45 | V     |
| Threshold Voltage P-Channel | V <sub>THP</sub> | ±0.3                 | 0.45     | 1.35  | V     |

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values ( $\Delta$ ) are applicable to the Operating Life test only.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

| Characteristics                                     | Symbols          | Test Conditions         | Units |
|---|------------------|-------------------------|-------|
| Ambient Temperature                                 | T <sub>amb</sub> | +125 (+0 -5)            | °C    |
| Outputs Q (all gates)                               | V <sub>OUT</sub> | Open or V <sub>SS</sub> | V     |
| Inputs $\overline{\text{CLR}}$ , CLK, D (all gates) | V <sub>IN</sub>  | V <sub>SS</sub>         | V     |
| Positive Supply Voltage                             | V <sub>DD</sub>  | 6 (+0 -0.5)             | V     |
| Negative Supply Voltage                             | V <sub>SS</sub>  | 0                       | V     |
| Duration  | t                | 72                      | Hours |

**NOTES:**

1. Input Protection Resistor = 680 $\Omega$  min to 47k $\Omega$  max.
2. Output Load = 1k $\Omega$  min to 10k $\Omega$  max.

2.6.2 P-Channel HTRB

| Characteristics                                     | Symbols          | Test Conditions         | Units |
|---|------------------|-------------------------|-------|
| Ambient Temperature                                 | T <sub>amb</sub> | +125 (+0 -5)            | °C    |
| Outputs Q (all gates)                               | V <sub>OUT</sub> | Open or V <sub>DD</sub> | V     |
| Inputs $\overline{\text{CLR}}$ , CLK, D (all gates) | V <sub>IN</sub>  | V <sub>DD</sub>         | V     |
| Positive Supply Voltage                             | V <sub>DD</sub>  | 6 (+0 -0.5)             | V     |
| Negative Supply Voltage                             | V <sub>SS</sub>  | 0                       | V     |
| Duration  | t                | 72                      | Hours |

**NOTES:**

1. Input Protection Resistor = 680 $\Omega$  min to 47k $\Omega$  max.
2. Output Load = 1k $\Omega$  min to 10k $\Omega$  max.

2.7 POWER BURN-IN CONDITIONS

| Characteristics               | Symbols                                | Test Conditions  | Units |
|-------------------------------|--|--|-------|
| Ambient Temperature           | T <sub>amb</sub>                       | +125 (+0 -5)   | °C    |
| Outputs Q (all gates)         | V <sub>OUT</sub>                       | V <sub>DD</sub>  | V     |
| Input $\overline{\text{CLR}}$ | V <sub>IN</sub>                        | V <sub>DD</sub>  | V     |
| Input CLK                     | V <sub>IN</sub>                        | V <sub>GEN1</sub>  | V     |
| Inputs D (all gates)          | V <sub>IN</sub>                        | V <sub>GEN2</sub>  | V     |
| Pulse Voltage                 | V <sub>GEN</sub>                       | 0V to V <sub>DD</sub>  | V     |
| Pulse Frequency Square Wave   | f <sub>GEN1</sub><br>f <sub>GEN2</sub> | 100k ±10%<br>50k ±10%<br>50 ±15% Duty Cycle<br>t <sub>r</sub> = t <sub>f</sub> ≤ 400ns | Hz    |
| Positive Supply Voltage       | V <sub>DD</sub>                        | 6 (+0 -0.5)  | V     |
| Negative Supply Voltage       | V <sub>SS</sub>                        | 0  | V     |

**NOTES:**

1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.7 Power Burn-in.

2.9 TOTAL DOSE RADIATION TESTING

2.9.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

| Characteristics               | Symbols          | Test Conditions | Units |
|-------------------------------|------------------|-----------------|-------|
| Ambient Temperature           | T <sub>amb</sub> | +22 ±3          | °C    |
| Outputs Q (all gates)         | V <sub>OUT</sub> | Open            | V     |
| Input $\overline{\text{CLR}}$ | V <sub>IN</sub>  | V <sub>SS</sub> | V     |
| Inputs CLK, D (all gates)     | V <sub>IN</sub>  | V <sub>DD</sub> | V     |
| Positive Supply Voltage       | V <sub>DD</sub>  | 6 ±0.3          | V     |
| Negative Supply Voltage       | V <sub>SS</sub>  | 0               | V     |

**NOTES:**

1. Input Protection Resistor = 680Ω min to 47kΩ max.

2.9.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Para. 2.3.1 Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

| Characteristics             | Symbols   | Limits                   |          |      | Units   |
|-----------------------------|-----------|--------------------------|----------|------|---------|
|                             |           | Drift Values<br>$\Delta$ | Absolute |      |         |
|                             |           |                          | Min      | Max  |         |
| Quiescent Current           | $I_{DD}$  | -                        | -        | 40   | $\mu A$ |
| Threshold Voltage N-Channel | $V_{THN}$ | $\pm 0.6$                | -0.4     | -1.5 | V       |
| Threshold Voltage P-Channel | $V_{THP}$ | $\pm 0.6$                | 0.4      | 1.4  | V       |

**APPENDIX 'A'**  
**AGREED DEVIATIONS FOR STMICROELECTRONICS (F)**

| ITEMS AFFECTED   | DESCRIPTION OF DEVIATIONS  |
|--|--|
| Para. 2.1.1 Deviations from the Generic Specification: Deviations from Production Control - Chart F2               | Total Dose Radiation Testing: The following deviation from the procedures for qualification and procurement lot acceptance in ESCC Basic Specification No. <a href="#">22900</a> shall apply:<br>The radiation exposure and test sequence requirements including radiation levels, time intervals for measurement, and the flow chart for qualification and lot acceptance testing, may be replaced by the requirements of ST radiation test procedure 0043082.                                      |
| Para. 2.1.1 Deviations from the Generic Specification: Deviations from Screening Tests - Chart F3                  | External Visual Inspection: The criteria applicable to chip-outs are those described in <a href="#">MIL-STD-883</a> , <a href="#">Test Method 2009</a> , Paras 3.3.6(b) and 3.3.7(a).<br>High Temperature Reverse Bias Burn-in: The temperature limits of <a href="#">MIL-STD-883</a> , Para. 4.5.8(c) may be used.<br>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.<br>Solderability is not applicable unless specifically stipulated in the Purchase Order. |
| Para. 2.1.1 Deviations from the Generic Specification: Deviations from Qualification and Periodic Tests - Chart F4 | External Visual Inspection: The criteria applicable to chip-outs are those described in <a href="#">MIL-STD-883</a> , <a href="#">Test Method 2009</a> , Paras 3.3.6(b) and 3.3.7(a).<br>Operating Life: The temperature limits of <a href="#">MIL-STD-883</a> , Para. 4.5.8(c) may be used.   |
| Para. 2.3.1 Room Temperature Electrical Measurements   | All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.<br>A summary of the pilot lot testing shall be provided if required by the Purchase Order.  |
| Para. 2.3.2 High and Low Temperatures Electrical Measurements  | High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification.<br>A summary of the pilot lot testing shall be provided if required by the Purchase Order.  |