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INTEGRATED CIRCUITS, SILICON MONOLITHIC, BIPOLAR QUAD SET-RESET LATCHES, BASED ON TYPES 54LS279 AND 54LS279A ESCC Detail Specification No. 9202/053

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space components coordination group

		Approved by		
Issue/Rev.	Date	SCCG Chairman	ESA Director General or his Deputy	
Issue 4	July 1992	Pomonican's	tab	
Revision 'A'	January 1995	Ponomen's	Arm	
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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This issue supersedes	s Issue 3 and incorporates all modifications agreed on the	
		basis of the following		
			: Title amended to include Type 54LS279A	22823
		DCN		None
		Para. 1.1	: Paragraph amended to include Type 54ALS279A	22823
		Table 1(a)	: Table rewritten	22823/ 22881
		Figures 2(a), (b), (c)	: Imperial dimensions deleted	22881
			: Reference to Note 6 amended to "Note 10"	23519
			: New figure added	22881
		Notes to Figures	: Title of the notes amended	22881
			: Note 1, last sentence added	22881
			: Note 8, 'or terminals' added	22881
			: Note 9, rewritten	22881
		Figure 3(a)	: Notes 11 and 12 added	22881
			 Figure for chip carrier package added Subtitles added above both drawings 	22881 22881
			: Comparison table added	22881
			: Note 1 added	22881
		Figure 3(b)	: Note amended	23519
		Para. 4.2.2	: PIND deviation deleted, "None" added	21048
		Para. 4.2.4	: Deviation deleted, "None" added	22919
			: Deviation deleted, "None" added	22919
		Para. 4.3.2	: Paragraph rewritten	23460
		Para. 4.4.2	: Paragraph rewritten : Paragraph rewritten	22881 22881
			: Paragraph rewritten	23519
		Para. 4.6.3	: "and functional test sequence" deleted	23519
		Para. 4.7.1	: " T_{amb} " added before " + 22 ± 3°C"	23519
			: In title and paragraph, "burn-in" amended to read	23519
			"power burn-in"	
		Tables 2 & 3	: No. 32 to 41, Test Conditions amended to incorporate	22823
			Type 54LS279A	Nasa
			: No. 32 to 41, In Test Conditions, "Variants 09-16" amended to read "Variants 09-18"	None
		· · · ·	: No. 50 to 53, Min. limit amended	22823
		Figure 5	: "54LS279A" added to drawing	22823
		Para. 4.8	: Title amended	23519
'A'	Jan. '95	P1. Cover Page	· · · · · · · · · · · · · · · · · · ·	None
		P2. DCN		None
		P6. Table 1(b)	: Nos. 2 and 3, Notes reference changed to "1" and	23573
			"2" respectively.	
			: No. 6, Entry amended to include DIL and FP	23573
			: Notes renumbered to "2", "3" and "1" respectively	23573
			and resequenced : Old Note 2, new Note 3 amended	23573
			: New Note 4 added	23573
		P7. Figure 2(a)	: Drawing and Table amended	221033
		P8. Figure 2(b)	: Drawing and Table amended	221033
		P15. Para. 4.3.2	: Maximum weights amended	221047
		P22. Fiaure 4(h)	: Note 1 corrected	23573

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APPENDICES (Applicable to specific Manufacturers only)

'A' Agreed Deviations for Texas Instruments (F)

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5

1. <u>GENERAL</u>

1.1 <u>SCOPE</u>

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Silicon Monolithic, Low Power Bipolar Schottky Quad Set-Reset Latches, based on Types 54LS279 and 54LS279A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 <u>PIN ASSIGNMENT</u>

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

- 1.8 <u>CIRCUIT SCHEMATIC</u> As per Figure 3(c).
- 1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).



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TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	54LS279	FLAT	2(a)	D7
02	54LS279	FLAT	2(a)	G4
05	54LS279	DIL	2(b)	D7
06	54LS279	DIL	2(b)	G4
07	54LS279	DIL	2(c)	D7
08	54LS279	DIL	2(c)	D3 or D4
09	54LS279A	FLAT	2(a)	D7
10	54LS279A	FLAT	2(a)	G4
13	54LS279A	DIL	2(b)	D7
14	54LS279A	DIL	2(b)	G4
15	54LS279A	DIL	2(c)	D7
16	54LS279A	DIL	2(c)	D3 or D4
17	54LS279A	CCP	2(d)	7
18	54LS279A	CCP	2(d)	4

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V _{CC}	-0.5 to 7.0	V	-
2	Input Voltage	V _{IN}	-0.5 to 7.0	V	Note 1
3	Device Dissipation	PD	38.5	mWdc	Note 2
4	Operating Temperature Range	T _{op}	-55 to +125	°C	-
5	Storage Temperature Range	T _{stg}	65 to +150	°C	-
6	Soldering Temperature For FP and DIL For CCP	T _{sol}	+ 265 + 245	°C	Note 3 Note 4

NOTES

- 1. Input current limited to -18mA.
- 2. Must withstand added PD due to short circuit conditions (i.e. IOS) at one output for 5 seconds.
- 3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
- 4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.



FIGURE 2 - PHYSICAL DIMENSIONS

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SYMBOL	MILLIMETRES		NOTES
STWIDUL	MIN	MAX	NOTES
A	1.27	2.03	
b	0.38	0.56	8
С	0.08	0.23	8
D	9.42	10.16	.4
E	6.27	7.24	
E1	7.00 T	/PICAL	4
е	1.27 T)	(PICAL	5, 9
L	7.87	8.89	8
L1	23.88	24.38	
Q	0.51	1.02	2
S	0.25	0.64	7



FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE



SYMBOL	MILLIMETRES		NOTES
STNDUL	MIN	MAX	NOTES
А	-	5.08	
b	0.38	0.66	8
b1	-	1.78	8
С	0.20 ·	0.44	8
D	19.18	19.94	4
E	6.22	7.62	4
E1	7.37	8.13	
е	2.54 T)	/PICAL	6, 9
F	1.27 T	YPICAL	
Н	0.76	-	
L ·	3.30	5.08	8
Q	0.51	-	3
S	0.38	1.27	7
α	0°	15°	10



FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - DUAL-IN-LINE PACKAGE



- NOTE 10

11

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SYMBOL	MILLIMETRES		NOTES	
STWDUL	MIN.	MAX.	NUTES	
A	-	5.08	-	
b	0.36	0.58	8	
b1	0.76	1.78	8	
с	0.20	0.38	8	
D	18.80	22.10	-	
E	5.59	7.87	-	
E1	7.37	8.13	4	
е	2.54 TY	′PICAL	6, 9	
L	3.18	5.08	-	
Q	0.38	2.03	3	
[·] S	0.25	1.35	7	
x	0°	15°	10	

NOTES: See Page 11.



FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE)



20 Terminal



SYMBOL	MILLIMETRES		NOTES	
STMDUL	MIN.	MAX.	NOTES	
A	8.687	9.093	-	
В	7.798	9.093	-	
С	0.250	0.510	11	
D	0.889	1.143	12	
E	1.140	1.400	8	
F	0.559	0.712	8	
G	1.27 TYPICAL		5, 9	
н	1.630	2.540	-	

NOTES: See Page 11.



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FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(d)

- 1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(d).
- 2. Dimension Q shall be measured at the point of exit of the lead from the body.
- 3. Dimension Q shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-centre lids, meniscus and glass overrun.
- 5. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ± 0.13mm of its true longitudinal position relative to Pins 1 and 16.
- 6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25 mm of its true longitudinal position relative to Pins 1 and 16.
- 7. Applies to all four corners.
- 8. All leads or terminals.
- 14 spaces for flat and dual-in-line packages.
 16 spaces for chip carrier packages.
- 10. Lead centre when α is 0°.
- 11. Index corner only 2 dimensions.
- 12. 3 non-index corners 6 dimensions.



FIGURE 3(a) - PIN ASSIGNMENT





CHIP CARRIER PACKAGE

(TOP VIEW)

FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND		~	0		-	-			-							
DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	1	8	9	10	11	12	13	14	15	16
CHIP CARRIER PIN OUTS	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

NOTES

1. All references throughout this specification relate to FLAT/DIL packages only.

FIGURE 3(b) - TRUTH TABLE (EACH LATCH)

	INPUTS						
- Ŝ1	- Š2	Ŕ	(Q)				
L	L	L	h				
L	х	н	н				
Х	L	н	н				
н	Н	L	L				
Н	Н	Н	No change				

NOTES

1. Logic Level Definitions: L = Low Level (Steady State), H = High Level (Steady State), X = Don't Care.

2. h = the output is HIGH as long as S1 or S2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.



NOTES

1. All resistive values are nominal

FIGURE 3(d) - FUNCTIONAL DIAGRAM (EACH LATCH)





2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

V_{IC} - Input Clamp Voltage.

V_{CC} - Supply Voltage.

4. **REQUIREMENTS**

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

- 4.2.1 <u>Deviations from Special In-process Controls</u> None.
- 4.2.2 <u>Deviations from Final Production Tests (Chart II)</u> None.
- 4.2.3 Deviations from Burn-in Tests (Chart III)
 - (a) Para. 7.1.1(a), High Temperature Reverse Bias tests and subsequent electrical measurements related to this test shall be omitted.
 - (b) Para. 9.9.2, Electrical Measurements at High and Low Temperatures: Only a test result summary, based on go-no-go tests and presented in histogram form is required.
- 4.2.4 <u>Deviations from Qualification Tests (Chart IV)</u> None.
- 4.2.5 Deviations from Lot Acceptance Tests (Chart V) None.



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4.3 MECHANICAL REQUIREMENTS

4.3.1 <u>Dimension Check</u>

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 0.7 grammes for the flat package, 2.2 grammes for the dual-in-line package and 0.6 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be either Type 'D' or Type 'G' with either Type I'3 or 4', Type '4' or Type I'7' finish in accordance with the requirements of ESA/SCC Basic Specification No.123500. For chip carrier packages, the finish shall be either Type '4' or Type I'7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(d).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

	<u>920205302B</u>
Detail Specification Number	
Type Variant (see Table 1(a))	
Testing Level (B or C, as applicable))



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ± 3 °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at T_{amb} = +125 and -55 °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5 of this specification.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - D.C. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD	TEST	TEST CONDITIONS	LIM	ITS	UNIT
140.		UTMBOL	MIL-STD 883	FIG.	(PINS UNDER TEST)	MIN	MAX	ONIT
1	Functional Test	-	-	3(b)	Verify Truth Table with Load. Note 1	-	-	-
2 to 11	Input Current High Level 1	l _{IH1}	3010	4(a)	V _{CC} = 5.5V, V _{IN} = 2.7V (Pins 1-2-3-5-6-10-11-12- 14-15)	-	20	μА
12 to 21	Input Current High Level 2 (Max. Input Voltage)	l _{iH2}	3010	4(a)	V _{CC} = 5.5V, V _{IN} = 7.0V (Pins 1-2-3-5-6-10-11-12- 14-15)	-	100	μΑ
22 to 31	Input Clamp Voltage	V _{IC}	3009	4(b)	V _{CC} = 4.5V, I _{IN} = - 18mA Note 2 (Pins 1-2-3-5-6-10-11-12- 14-15)	-	- 1.5	V
32 to 41	Input Current Low Level	l _{IL}	3009	4(c)	$V_{CC} = 5.5V, V_{IL} = 0.4V$ Variants 01-08 Variants 09-18 (Pins 1-2-3-5-6-10-11-12- 14-15)	-	400 200	μА
42 to 45	Output Voltage Low Level	V _{OL}	3007	4(d)	$V_{CC} = 4.5V, V_{IL} = 0.7V$ $V_{IH} = 2.0V, I_{OL} = 4.0mA$ (Pins 4-7-9-13)	-	0.4	V
46 to 49	Output Voltage High Level	V _{OH}	3006	4(e)	V _{CC} = 4.5V, V _{IL} = 0.7V V _{IH} = 2.0V, I _{OH} = - 400µA (Pins 4-7-9-13)	2.5	-	V
50 to 53	Output Current Short Circuit	los	3011	4(f)	V _{CC} = 5.5V Note 3 (Pins 4-7-9-13)	- 20	- 100	mA
54	Supply Current	lcc	3005	4(g)	V _{CC} = 5.5V Note 4 (Pin 16)	-	7.0	mA

.

NOTES: See Page 18.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - A.C. PARAMETERS

No	No. CHARACTERISTICS		CHARACTERISTICS SYMBOL		TEST METHOD T		TEST CONDITIONS (PINS UNDER TEST)	LIM	IITS	UNIT
			MIL-STD 883	FIG.	(NOTE 5)	MIN	MAX	UNIT		
55 to 58	Low to High Level S to Q	^t PLH	3003	4(h)	$V_{CC} = 5.0V$ $R_L = 2.0k\Omega$ $C_L = 15pF$ (Pins 4-7-9-13)	-	22	ns		
59 to 62	High to Low Level S to Q	tphl			(1 113 4-7-5-13)	-	21			
-63 to 66	High to Low Level from R to Q	t _{PLH}				-	27			

NOTES

- 1. Go-no-go test with $V_{IL} = 0.3V$; $V_{IH} = 3.0V$; trip point 1.5V.
- 2. All inputs and outputs not under test shall be open.
- 3. No more than one output should be shorted at a time, and only for 1 second maximum.
- 4. I_{CC} is measured with all R inputs grounded and 4.5V applied to all S inputs.
- 5. Propagation delay measurements shall be performed as a go-no-go test on a 100% basis. Read-and-record measurements shall be performed on an LTPD7 sample basis following the Chart III Burn-in Test.



TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, + 125(+0-5) °C AND - 55(+5-0) °C

No	No. CHARACTERISTICS		TEST METHOD	TEST	TEST CONDITIONS	LIM	IITS	UNIT
110.	UNANAUTENIU NOU	STICS SYMBOL MILTIOD FIEST CONDITIONS MIL-STD FIG. (PINS UNDER TEST) 883		(PINS UNDER TEST)	MIN	MAX	UNIT	
1	Functional Test	-	-	3(b)	Verify Truth Table with Load. Note 1	-	-	-
2 to 11	Input Current High Level 1	l _{iH1}	3010	4(a)	V _{CC} = 5.5V, V _{IN} = 2.7V (Pins 1-2-3-5-6-10-11-12- 14-15)	-	20	μА
12 to 21	Input Current High Level 2 (Max. Input Voltage)	I _{IH2}	3010	4(a)	V _{CC} = 5.5V, V _{IN} = 7.0V (Pins 1-2-3-5-6-10-11-12- 14-15)	-	100	μА
22 to 31	Input Clamp Voltage	V _{IC}	3009	4(b)	V _{CC} = 4.5V, I _{IN} = - 18mA Note 2 (Pins 1-2-3-5-6-10-11-12- 14-15)	-	- 1.5	V
32 to 41	Input Current Low Level	Ι _{ΙL}	3009	4(c)	$V_{CC} = 5.5V, V_{IL} = 0.4V$ Variants 01-08 Variants 09-18 (Pins 1-2-3-5-6-10-11-12- 14-15)	-	400 200	μА
42 to 45	Output Voltage Low Level	V _{OL}	3007	4(d)	V _{CC} = 4.5V, V _{IL} = 0.7V V _{IH} = 2.0V, I _{OL} = 4.0mA (Pins 4-7-9-13)	-	0.4	V
46 to 49	Output Voltage High Level	V _{OH}	3006	4(e)	V _{CC} = 4.5V, V _{IL} = 0.7V V _{IH} = 2.0V, I _{OH} = - 400µA (Pins 4-7-9-13)	2.5	-	V
50 to 53	Output Current Short Circuit	los	3011	4(f)	V _{CC} = 5.5V Note 3 (Pins 4-7-9-13)	- 20	- 100	mA
54	Supply Current	lcc	3005	4(g)	V _{CC} = 5.5V Note 4 (Pin 16)		7.0	mA

NOTES: See Page 18.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - HIGH LEVEL INPUT CURRENT







NOTES

1. Each input to be tested separately.



1. Each input to be tested separately.

FIGURE 4(c) - LOW LEVEL INPUT CURRENT



NOTES

1. Each input to be tested separately.



FIGURE 4(d) - LOW LEVEL OUTPUT VOLTAGE

V_{CC}

<u>NOTES</u>

1. Test per Truth Table.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - HIGH LEVEL OUTPUT VOLTAGE

FIGURE 4(f) - SHORT CIRCUIT OUTPUT CURRENT



NOTES

1. Test per Truth Table.

NOTES

- 1. No more than one output should be shorted at a time.
- 2. Test per Truth Table.

FIGURE 4(g) - SUPPLY CURRENT



NOTES

1. See Note 4 for Table 2.



FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - DYNAMIC TEST AND SWITCHING WAVEFORMS



NOTES

- 1. Input pulse characteristics: PRR \leq 1.0MHz, t_r \leq 15ns, t_f \leq 6.0ns and t_p = 0.5µs.
- 2. All diodes are 1N3064 or 1N916.



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TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2 to 11	Input Current High Level 1	l _{iH1}	As per Table 2	As per Table 2	±20 or (1) ±0.5	% µА
32 to 41	Input Current Low Level	l _{IL}	As per Table 2	As per Table 2	±18	μΑ
42 to 45	Output Voltage Low Level	V _{OL}	As per Table 2	As per Table 2	± 60	mV
46 to 49	Output Voltage High Level	V _{OH}	As per Table 2	As per Table 2	±240	mV

<u>NOTES</u>

1. Whichever is greater, referred to the initial value.

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T _{amb}	+ 125(+ 0 – 5)	°C
2	Power Supply Voltage	V _{CC}	+ 5(+ 0.5 – 0)	V
3	Pulse Voltage	V _{GEN}	0.5 max. to 3.0 min.	V
4	Frequency	f	100 (See Note 1)	Hz
5	Fan-out	-	10	-
6	Rise Time	t _r	50 max.	μs
7	Fall Time	t _f	50 max.	μs
8	Duty Cycle	-	20 min.	%

NOTES

1. Tolerance $\pm 10\%$.



FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST





1. $R = 1.2k\Omega$.



4.8 <u>ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC</u> <u>SPECIFICATION NO. 9000)</u>

4.8.1 <u>Electrical Measurements on Completion of Environmental Tests</u>

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at T_{amb} = +22 ± 3 °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 <u>Electrical Measurements on Completion of Endurance Tests</u>

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3 \text{ °C}$.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be T_{amb} = +150(+0-5) °C.



TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS

No	No. CHARACTERISTICS S		SPEC. AND/OR	TEST	CHAN	UNIT	
NO.			TEST METHOD	CONDITIONS	(Δ)	ABSOLUTE	
2 to 11	Input Current High Level 1	l _{IH1}	As per Table 2	As per Table 2	± 1.0	-	μА
12 to 21	Input Current High Level 2	I _{IH2}	As per Table 2	As per Table 2		100	μA
32 to 41	Input Current Low Level	l _{iL}	As per Table 2	As per Table 2	<u>+</u> 12	-	μА
42 to 45	Output Voltage Low Level	V _{OL}	As per Table 2	As per Table 2	±60	-	mV
46 to 49	Output Voltage High Level	V _{OH}	As per Table 2	As per Table 2	±240	-	mV
54	Supply Current	lcc	As per Table 2	As per Table 2	± 20	-	%



APPENDIX 'A'

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AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Scanning Electron Microscope (SEM) Inspection may be performed using TIF document TIF 3.61.610.001.
Para. 4.2.2	Prior to Die Shear Test TIF may perform a Radiographic Inspection on the randomly chosen samples to be subjected to this test, using TIF document TIF 50.42-3002.
Para. 4.2.3	Radiographic Inspection may be performed using TIF document TIF 50.42-3002.