# INTEGRATED CIRCUITS, SILICON MONOLITHIC,

# LOW POWER BIPOLAR SCHOTTKY DUAL

# D-FLIP-FLOP WITH PRESET AND CLEAR,

# BASED ON TYPE 54LS74A

# ESCC Detail Specification No. 9203/013

**ISSUE 1**

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# INTEGRATED CIRCUITS, SILICON MONOLITHIC, LOW POWER BIPOLAR SCHOTTKY DUAL D-FLIP-FLOP WITH PRESET AND CLEAR, BASED ON TYPE 54LS74A

## ESA/SCC Detail Specification No. 9203/013

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| | | | |

## DOCUMENTATION CHANGE NOTICE

| Rev. Letter | Rev. Date | CHANGE Reference | Item | Approved DCR No. |
|---|---|---|---|---|
| | | This issue supersedes Issue 4 and incorporates all modifications agreed on the basis of the following DCR's: | | |
| | | Cover page | | None |
| | | DCN | | None |
| | | Table 1(a) | : Variants 11 and 12 added | 22881 |
| | | Figures 2(a), (b), (c) | : Imperial dimensions deleted | 22881 |
| | | Figure 2(d) | : New figure | 22881 |
| | | Figures 2(a) to (d) | : - Title of the notes amended | 22881 |
| | | | - Note 1, last sentence added | 22881 |
| | | | - Note 8, 'or terminals' added | 22881 |
| | | | - Note 9, rewritten | 22881 |
| | | | - Notes 11 and 12, new notes | 22881 |
| | | Figure 3(a) | : - Title added | 22881 |
| | | | - Figure for chip carrier package added | 22881 |
| | | | - Comparison table added | 22881 |
| | | | - Note 1 added | 22881 |
| | | Figure 3(c) | : Note 1, 'and in ohms' deleted | None |
| | | Para 4.2.2 | : Text amended (PIND deleted) | 21048 |
| | | Para 4.2.4 | : Deviation replaced by 'None' | 22919 |
| | | Para 4.2.5 | : Deviation replaced by 'None' | 22919 |
| | | Para 4.3.2 | : Para rewritten | 23460 |
| | | Para 4.4.2 | : Para rewritten | 22881 |
| | | Para 4.5.2 | : Para rewritten | 22881 |
| | | Table 6 | : 'ditto' changed into 'As per Table 2' | None |
| | | Appendix 'A' | : Last item about Table 3 added | 22910 |
| 'A' | July '92 | P1. Cover Page | | None |
| | | P2. DCN | | None |
| | | P3. Table of Contents | : Amended as relevant | None |
| | | P8. Figure 2(b) | : Reference to Note 6 changed to Note 10 | 23519 |
| | | P9. Figure 2(c) | : Reference to Note 6 changed to Note 10 | 23519 |
| | | | : Min. value of 'L' amended | None |
| | | P17. Para. 4.5.3 | : Wording amended | 23519 |
| | | P17. Para. 4.6.3 | : 'and functional test sequence' deleted | 23519 |
| | | P17. Para. 4.7.2 | : 'power' added before 'burn-in' | 23519 |
| | | P17. Para. 4.7.3 | : 'power' added before 'burn-in' | 23519 |
| | | P28. Para. 4.8 | : Title amended | 23519 |
| 'B' | Jan. '95 | P1. Cover Page | | None |
| | | P2. DCN | | None |
| | | P6. Table 1(b) | : Nos. 2 and 3, Notes reference changed to "1" and "2" respectively. | 23573 |
| | | | : No. 6, Entry amended to include DIL and FP | 23573 |
| | | | : Notes renumbered to "2", "3" and "1" respectively and resequenced | 23573 |
| | | | : Old Note 2, new Note 3 amended | 23573 |
| | | | : New Note 4 added | 23573 |
| | | P7. Figure 2(a) | : Drawing and Table amended | 221033 |
| | | P8. Figure 2(b) | : Drawing and Table amended | 221033 |
| | | P16. Para. 4.3.2 | : Maximum weights amended | 221047 |
| | | P25. Figure 4(h) | : Note 1 corrected | 23573 |

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**TABLES**



**FIGURES**



**APPENDICES** (Applicable to specific Manufacturers only)

## 1. GENERAL

### 1.1 SCOPE

This Specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, low power bipolar Schottky, Dual D-Flip-Flop with preset and clear, based on Type 54LS74A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

### 1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

### 1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

### 1.4 PARAMETER DERATING INFORMATION (Figure 1)

Not applicable.

### 1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

### 1.6 PIN ASSIGNMENT

As per Figure 3(a).

### 1.7 TRUTH TABLE

As per Figure 3(b).

### 1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

### 1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

## TABLE 1(a) - TYPE VARIANTS

| Variant | Case | Figure | Lead Material and/or Finish |
|---|---|---|---|
| 01 | FLAT | 2(a) | D7 |
| 02 | FLAT | 2(a) | G4 |
| 05 | DIL | 2(b) | D7 |
| 06 | DIL | 2(b) | G4 |
| 07 | DIL | 2(c) | D7 |
| 08 | DIL | 2(c) | D3 or D4 |
| 11 | CCP | 2(d) | 7 |
| 12 | CCP | 2(d) | 4 |

## TABLE 1(b) - MAXIMUM RATINGS

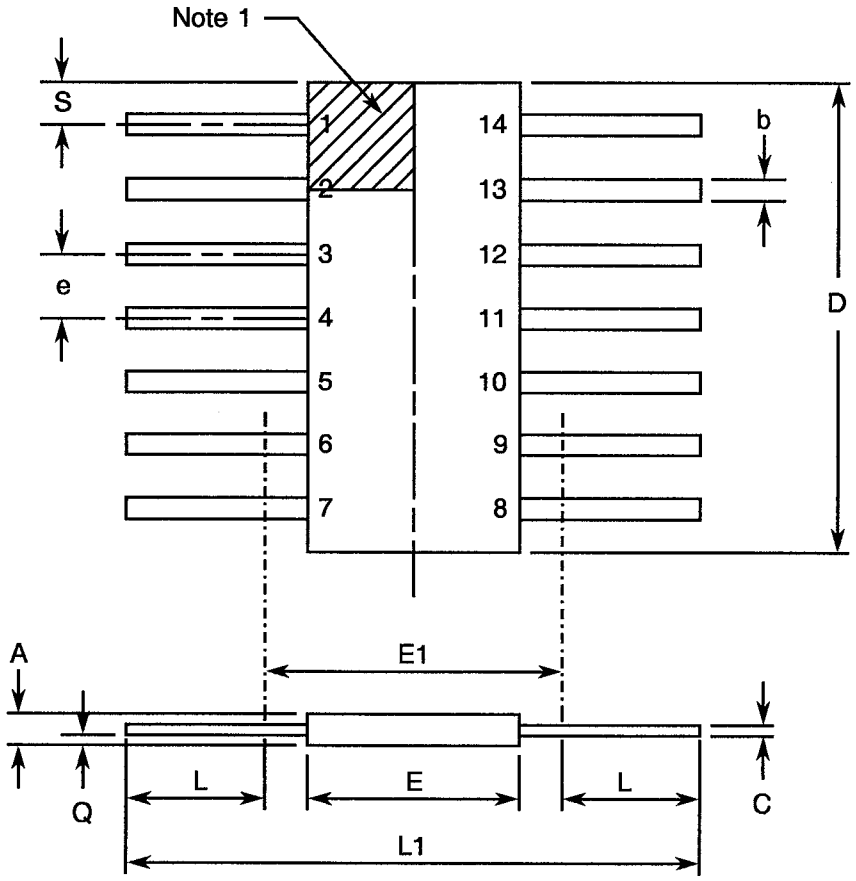
| No. | Characteristics | Symbol | Maximum Ratings | Unit | Remarks |
|---|---|---|---|---|---|
| 1 | Supply Voltage | $V_{CC}$ | -0.5 to 7.0 | V | |
| 2 | Input Voltage | $V_{IN}$ | -0.5 to 7.0 | V | Note 1 |
| 3 | Device Dissipation | $P_D$ | 44 | mWdc | Note 2 |
| 4 | Operating Temperature Range | $T_{op}$ | -55 to +125 | °C | |
| 5 | Storage Tempreature Range | $T_{stg}$ | -65 to +150 | °C | |
| 6 | Soldering Temperature<br>For FP and DIL<br>For CCP | $T_{sol}$ | <br>+265<br>+245 | °C | <br>Note 3<br>Note 4 |

**NOTES**

1. Input current limited to −18mA.
2. Must withstand added PD due to short circuit conditions (i.e. IOS) at one output for 5 seconds.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

## FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE

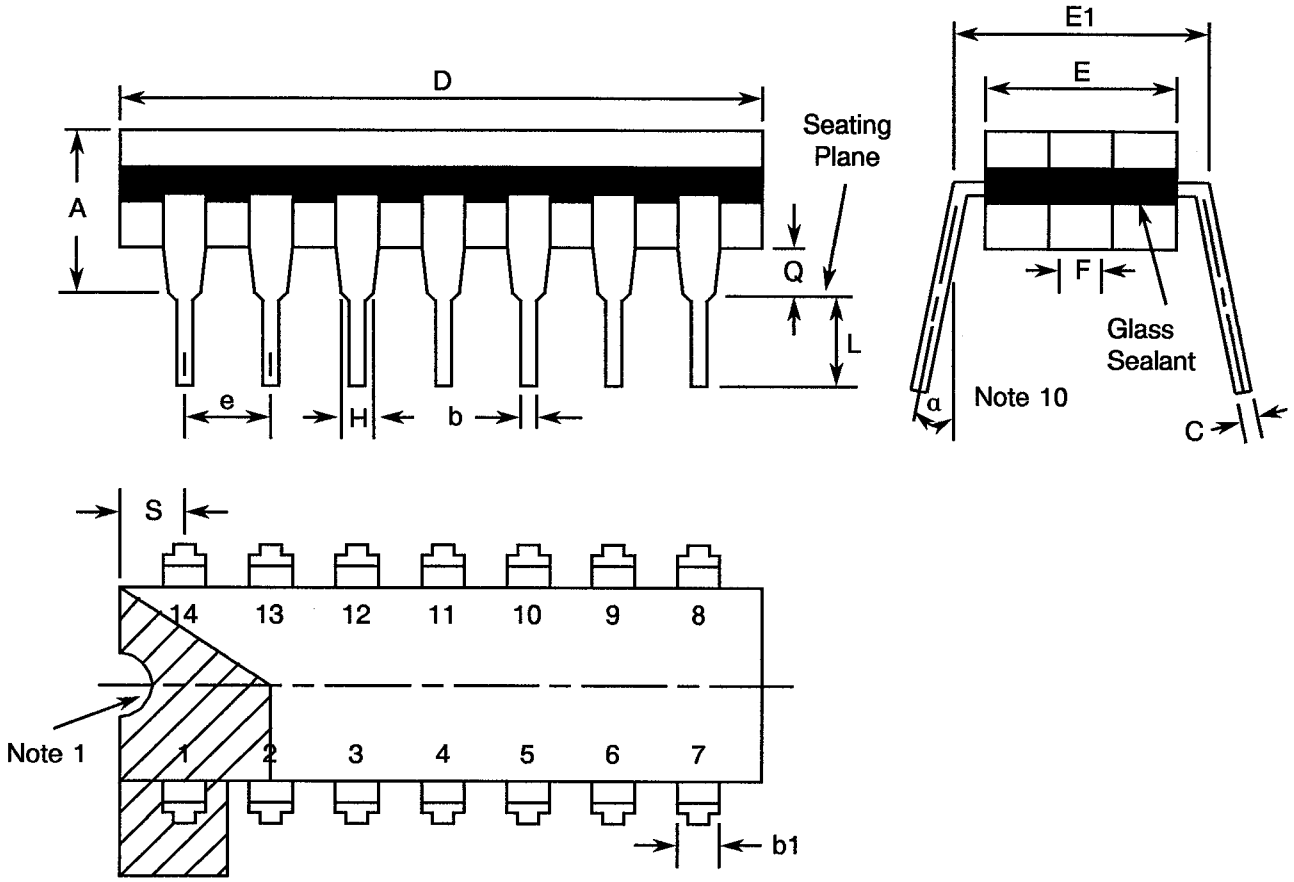



| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN | MAX | |
| A | 1.27 | 2.03 | |
| b | 0.38 | 0.56 | 8 |
| C | 0.08 | 0.23 | 8 |
| D | 8.56 | 8.89 | 4 |
| E | 5.97 | 6.73 | |
| E1 | 7.00 TYPICAL | | 4 |
| e | 1.27 TYPICAL | | 5, 9 |
| L | 6.86 | 8.00 | 8 |
| L1 | 21.34 | 21.84 | |
| Q | 0.51 | 1.02 | 2 |
| S | 0.25 | 0.64 | 7 |

**NOTES:** See Page 11.

## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE

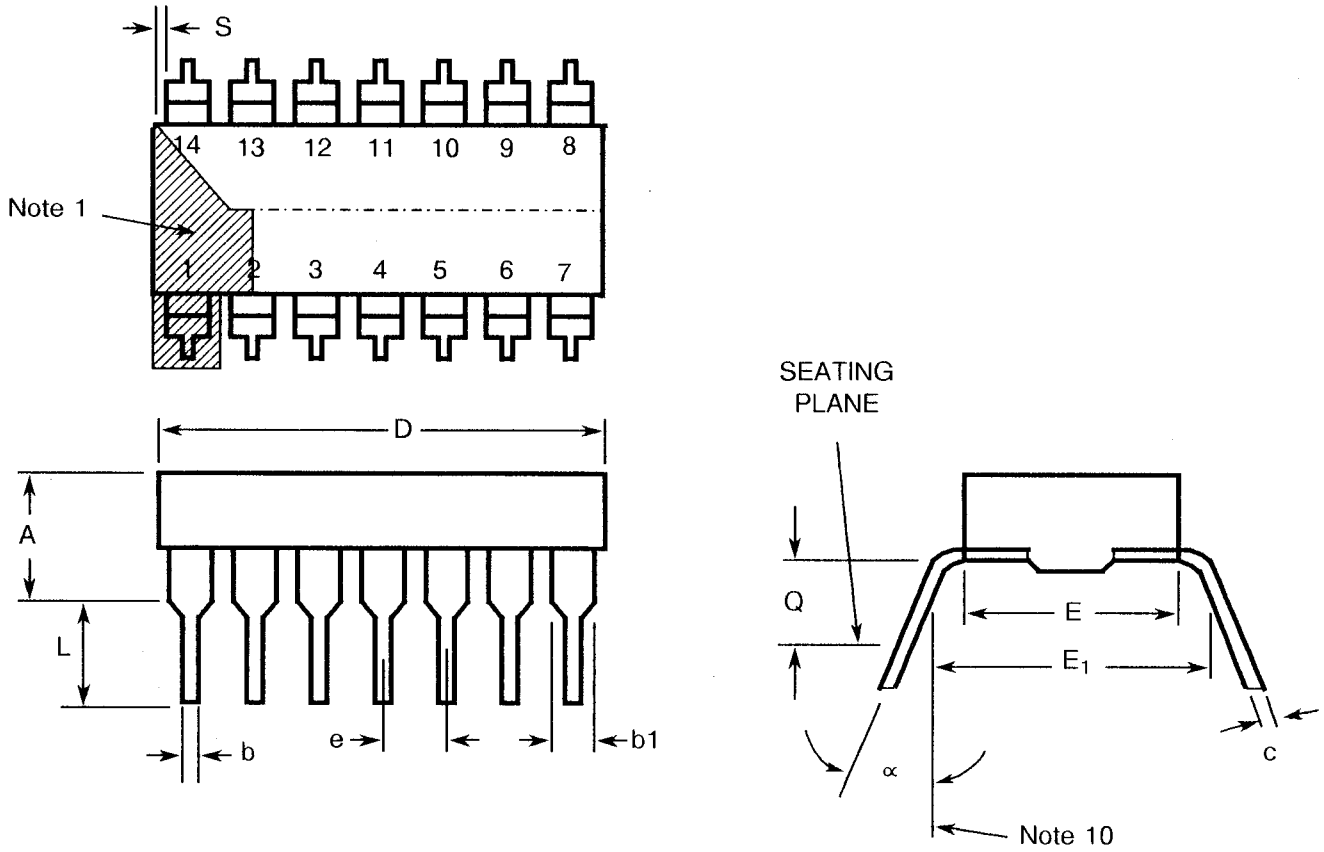



| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN | MAX | |
| A | - | 5.08 | |
| b | 0.38 | 0.66 | 8 |
| b1 | - | 1.78 | 8 |
| C | 0.20 | 0.44 | 8 |
| D | 19.18 | 19.94 | 4 |
| E | 6.22 | 7.62 | 4 |
| E1 | 7.37 | 8.13 | |
| e | 2.54 TYPICAL | | 6, 9 |
| F | 1.27 TYPICAL | | |
| H | 0.76 | - | 8 |
| L | 3.30 | 5.08 | 8 |
| Q | 0.51 | - | 3 |
| S | 1.78 | 2.54 | 7 |
| α | 0° | 15° | 10 |

**NOTES:** See Page 11.

## FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(c) - DUAL-IN-LINE PACKAGE

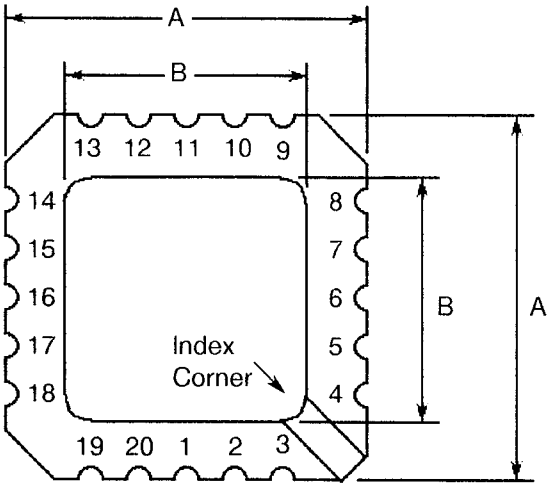



| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN. | MAX. | |
| A | - | 5.08 | |
| b | 0.36 | 0.58 | 8 |
| $b_1$ | 0.76 | 1.78 | 8 |
| c | 0.20 | 0.38 | 8 |
| D | 16.26 | 19.96 | |
| E | 5.59 | 7.87 | |
| $E_1$ | 7.37 | 8.13 | 4 |
| e | 2.54 Typical | | 6, 9 |
| L | 3.18 | 5.08 | |
| Q | 0.38 | 2.03 | 3 |
| S | 0.25 | 1.35 | 7 |
| ∝ | 0° | 15° | 10 |

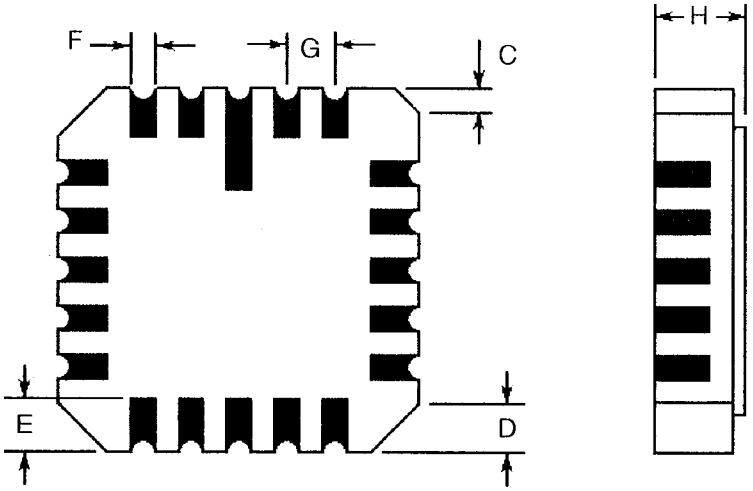
**NOTES:** See Page 11.

**FIGURE 2 - PHYSICAL DIMENSIONS (Continued)**

FIGURE 2(d) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE)




20 Terminal




| Symbol | Millimetres | | Notes |
|---|---|---|---|
| | Min. | Max. | |
| A | 8.687 | 9.093 | |
| B | 7.798 | 9.093 | |
| C | 0.250 | 0.510 | 11 |
| D | 0.889 | 1.143 | 12 |
| E | 1.140 | 1.400 | 8 |
| F | 0.559 | 0.712 | 8 |
| G | 1.27 Typical | | 5, 9 |
| H | 1.630 | 2.540 | |

**NOTES**: See Page 11.

## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

## NOTES TO FIGURES 2(a) to 2(d)

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(d).

2. Dimension Q shall be measured at the point of exit of the lead from the body.

3. Dimension Q shall be measured from the seating plane to the base plane.

4. This dimension allows for off-centre lids, meniscus and glass overrun.

5. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ± 0.13mm of its true longitudinal position relative to Pins 1 and 14 .

6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25mm of its true longitudinal position relative to Pins 1 and 14.

7. Applies to all four corners.

8. All leads or terminals.

9. 12 spaces for flat and dual-in-line packages.
   16 spaces for chip carrier packages.

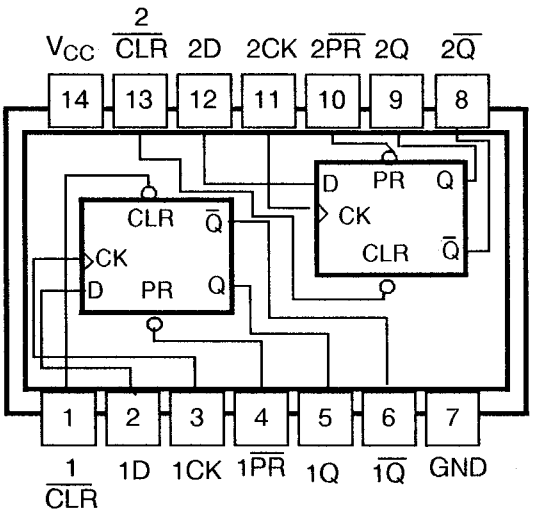
10. Lead centre when $\alpha$ is 0°.

11. Index corner only - 2 dimensions.

12. 3 non-index corners - 6 dimensions.

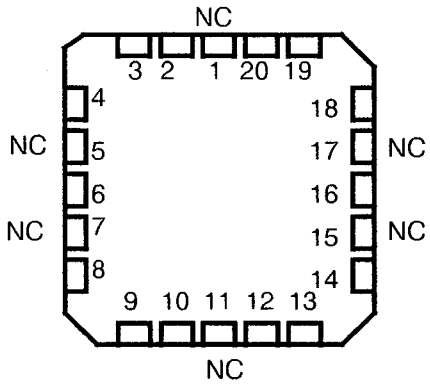
## FIGURE 3 (a) - PIN ASSIGNMENT

DUAL-IN-LINE AND FLAT PACKAGE




(TOP VIEW)

CHIP CARRIER PACKAGE




(TOP VIEW)

FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| CHIP CARRIER PIN OUTS | 2 | 3 | 4 | 6 | 8 | 9 | 10 | 12 | 13 | 14 | 16 | 18 | 19 | 20 |

**NOTES** 1. All references throughout this specification relate to FLAT/DIL packages only.

## FIGURE 3(b) - TRUTH TABLE

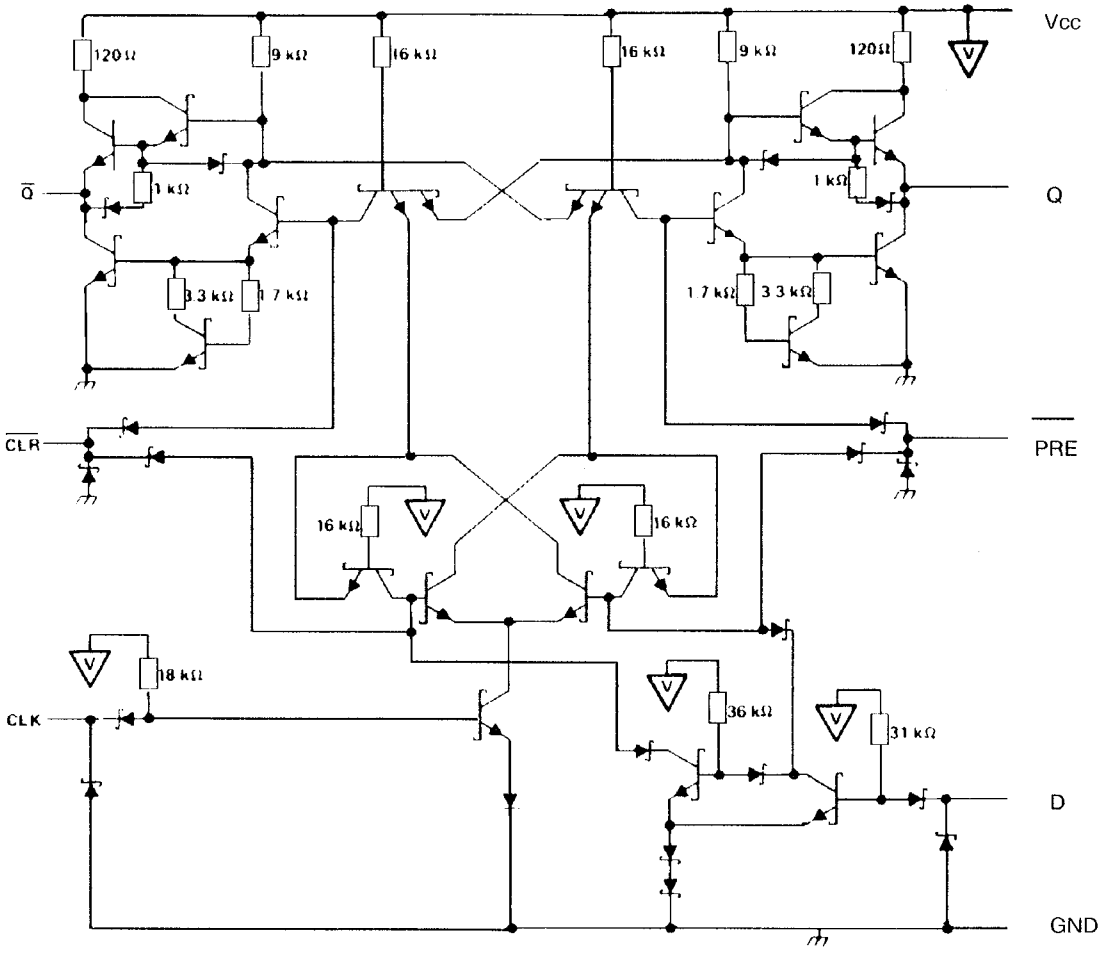
Function Table (each Flip Flop)

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{\text{PRESET}}$ | $\overline{\text{CLEAR}}$ | CLOCK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H * | H * |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q_0}$ |

**NOTES**

1. H = high level (steady state), L = low level (steady state), X = Irrelevant, $Q_0$ = level of Q before indicated steady-state input conditions were established, ↑ = transition from low to high level, * = Nonstable configuration, it will not persist when clear and preset return to high level.

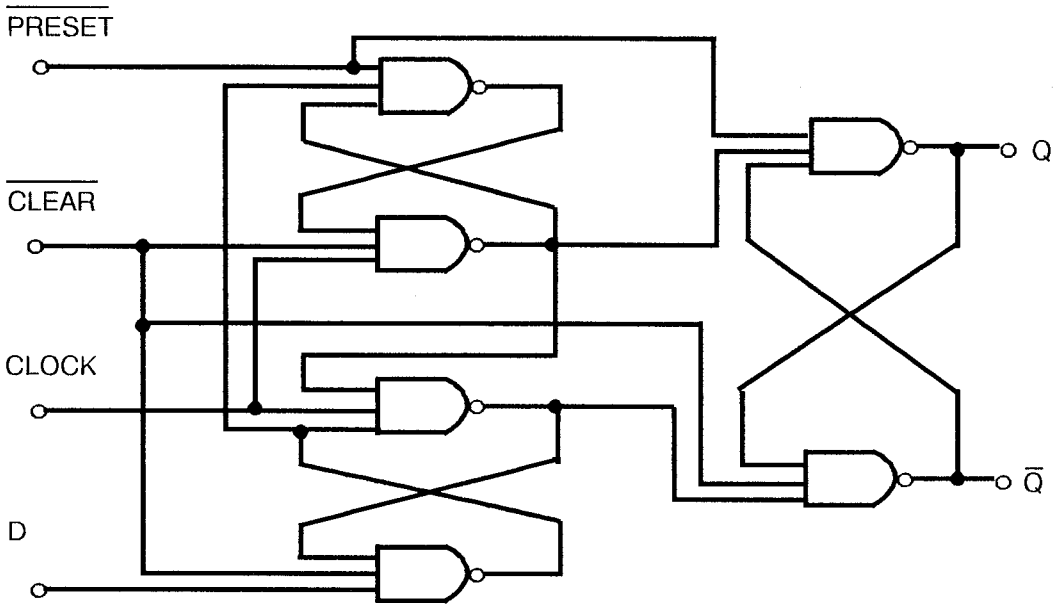
## FIGURE 3(c) - CIRCUIT SCHEMATIC




**NOTES**

1. Resistor values are nominal

**FIGURE 3(d) - FUNCTIONAL DIAGRAM**
(Each Flip-Flop)



## 2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

## 3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

$V_{IC}$ = Input Clamp Voltage

$V_{CC}$ = Supply Voltage

## 4. REQUIREMENTS

### 4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

### 4.2 DEVIATIONS FROM GENERIC SPECIFICATION

#### 4.2.1 Deviations from Special In-process Control

None.

#### 4.2.2 Deviations from Final Production Tests (Chart II)

None.

#### 4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), High Temperature Reverse Bias test and subsequent electrical measurements related to this test shall be omitted.

(b) Para. 9.9.2, Electrical Measurements at High and Low Temperatures: Only a test result summary, based on go-no-go tests and presented in histogram form is required.

#### 4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 0.7 grammes for the flat package, 2.2 grammes for the dual-in-line package and 0.6 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be either Type 'D' or Type 'G' with either Type '3 or 4', Type '4' or Type '7' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be either Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

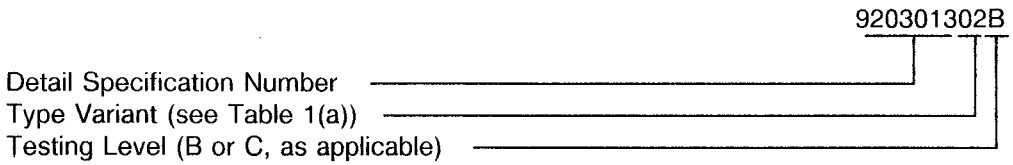
(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(d).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:-




4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL CHARACTERISTICS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb}$ = +22 ± 3 °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb}$ = +125 and -55 °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb}$ = +22 ± 3 °C. The parameter drift values (Δ) applicable to the parameters scheduled shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in test are shown in Figure 5 of this specification.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - D.C. PARAMETERS

| No. | Characteristics | Symbol | Test Method MIL-STD-883 | Test Fig. | Test Conditions (Pins under Test) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Max. | |
| 1 | Functional Test | - | - | 3(b) | Verify Truth Table with Load. Note 1 | - | - | - |
| 2 to 3 | Input Current High Level at D Input | $I_{IH1}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 2-12) Note 7 | - | 20 | µA |
| 4 to 5 | Input Current High Level at D Input (Max. Input Voltage) | $I_{IH2}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 7.0V (Pins 2-12) Note 7 | - | 100 | µA |
| 6 to 9 | Input Current High Level at $\overline{\text{Clear}}$ or $\overline{\text{Preset}}$ | $I_{IH3}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 1-4-10-13) Note 7 | - | 40 | µA |
| 10 to 13 | Input Current High Level at $\overline{\text{Clear}}$ or $\overline{\text{Preset}}$ (Max. Input Voltage) | $I_{IH4}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 7.0V (Pins 1-4-10-13) Note 7 | - | 200 | µA |
| 14 to 15 | Input Current High Level at Clock | $I_{IH5}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 3-11) Note 7 | - | 20 | µA |
| 16 to 17 | Input Current High Level at Clock (Max. Input Voltage) | $I_{IH6}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 7.0V (Pins 3-11) Note 7 | - | 100 | µA |
| 18 to 25 | Input Clamp Voltage | $V_{IC}$ | 3009 | 4(b) | $V_{CC}$ = 4.5V, $I_{IN}$ = -18mA (Pins 1-2-3-4-10-11-12-13) Note 2 | - | -1.5 | V |
| 26 to 29 | Input Current Low Level at D or Clock | $I_{IL1}$ | 3009 | 4(c) | $V_{CC}$ = 5.5V, $V_{IN}$ = 0.4V (Pins 2-3-11-12) Note 8 | - | -400 | µA |
| 30 to 33 | Input Current Low Level at $\overline{\text{Clear}}$ or $\overline{\text{Preset}}$ | $I_{IL2}$ | 3009 | 4(c) | $V_{CC}$ = 5.5V, $V_{IN}$ = 0.4V (Pins 1-4-10-13) Note 8 | - | -800 | µA |
| 34 to 37 | Output Voltage Low Level | $V_{OL}$ | 3007 | 4(d) | $V_{CC}$ = 4.5V, $V_{IH}$ = 2.0V $I_{OL}$ = 4mA, $V_{IL}$ = 0.7V (Pins 5-6-8-9) | - | 0.4 | V |

**NOTES**: See Page 20.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - D.C. PARAMETERS (CONTINUED)**

| No. | Characteristics | Symbol | Test Method MIL-STD-883 | Test Fig. | Test Conditions (Pins under Test) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Max. | |
| 38 to 41 | Output Voltage High Level | $V_{OH}$ | 3006 | 4(e) | $V_{CC}$ = 4.5V, $V_{IH}$ = 2.0V $V_{IL}$ = 0.7V, $I_{OH}$ = -400µA (Pins 5-6-8-9) | 2.5 | - | V |
| 42 to 45 | Output Current Short Circuit | $I_{OS}$ | 3011 | 4(f) | $V_{CC}$ = 5.5V (Pins 5-6-8-9) Note 3 | -15 | -100 | mA |
| 46 to 47 | Supply Current | $I_{CC}$ | 3005 | 4(g) | $V_{CC}$ = 5.5V, Note 4 (Pin 14) | - | 8 | mA |

**NOTES:** See Page 20.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - A.C. PARAMETERS

| No. | Characteristics | Symbol | Test Method MIL-STD-883 | Test Fig. | Test Conditions (Pins under Test) (Note 6) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Max. | |
| 48 to 51 | Propagation Delay Low to High Level from Clock, $\overline{\text{Clear}}$ or $\overline{\text{Preset}}$ | $t_{PLH}$ | 3003 | 4(h) | $V_{CC}$ = 5.0V<br>$R_L$ = 2kΩ<br>$C_L$ = 15pF | - | 25 | ns |
| 52 to 54 | Propagation Delay High to Low Level from Clock, $\overline{\text{Clear}}$ or $\overline{\text{Preset}}$ | $t_{PHL1}$ | | | (Pins 5-6-8-9) | - | 40 | |
| 55 to 56 | Maximum Clock Frequency | $f_{max}$ | - | 4(h) | $V_{CC}$ = 5.5V<br>$R_L$ = 2kΩ<br>$C_L$ = 15pF<br>(Pins 3-11)<br>Note 5 | 25 | - | MHz |

**NOTES**

1. Go-no-go test with $V_{IL}$ = 0.3V; $V_{IH}$ = 3.0V; trip point 1.5V.
2. All inputs and outputs not under test shall be open.
3. No more than one output shall be shorted at a time, and only for 1 second maximum.
4. With all outputs open, $I_{CC}$ is measured, after a momentary Ground, at 'D', Clock and $\overline{\text{Preset}}$; then with 'D', Clock and $\overline{\text{Clear}}$ grounded.
5. This parameter shall be measured only when required by purchase order. In any case, the Manufacturer shall guarantee that the devices meet this requirement.
6. Propagation delay measurements shall be performed as a go-no-go test on a 100% basis. Read-and-record measurements shall be performed on an LTPD7 sample basis following the Chart III burn-in test.
7. $I_{IH}$ Input Conditions:-

| Input under Test | Conditions |
|---|---|
| $\overline{\text{Clear}}$ | $\overline{\text{Preset}}$, Clock and D inputs at 5.5V. |
| $\overline{\text{Preset}}$ | $\overline{\text{Clear}}$ and D inputs at 5.5V, Clock input from Ground to 5.5V. |
| Clock | $\overline{\text{Preset}}$ and D inputs at 5.5V, $\overline{\text{Clear}}$ input grounded. |
| D | $\overline{\text{Preset}}$ and Clock inputs at 5.5V, $\overline{\text{Clear}}$ input grounded. |

8. $I_{IL}$ Input Conditions:-

| Input under Test | Conditions |
|---|---|
| $\overline{\text{Clear}}$ | $\overline{\text{Preset}}$, Clock and D inputs at 5.5V. |
| $\overline{\text{Preset}}$ | $\overline{\text{Clear}}$ and Clock inputs at 5.5V, D input grounded. |
| Clock | $\overline{\text{Clear}}$ input at 5.5V, $\overline{\text{Preset}}$ and D inputs grounded. |
| D | Clock and $\overline{\text{Clear}}$ inputs at 5.5V, Preset input grounded. |

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125°C AND -55°C**

| No. | Characteristics | Symbol | Test Method MIL-STD-883 | Test Fig. | Test Conditions (Pins under Test) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Max. | |
| 1 | Functional Test | - | - | 3(b) | Verify Truth Table with Load. Note 1 | - | - | - |
| 2 to 3 | Input Current High Level at D Input | $I_{IH1}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 2-12) Note 7 | - | 20 | µA |
| 4 to 5 | Input Current High Level at D Input (Max. Input Voltage) | $I_{IH2}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 7.0V (Pins 2-12) Note 7 | - | 100 | µA |
| 6 to 9 | Input Current High Level at $\overline{Clear}$ or $\overline{Preset}$ | $I_{IH3}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 1-4-10-13) Note 7 | - | 40 | µA |
| 10 to 13 | Input Current High Level at $\overline{Clear}$ or $\overline{Preset}$ (Max. Input Voltage) | $I_{IH4}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 7.0V (Pins 1-4-10-13) Note 7 | - | 200 | µA |
| 14 to 15 | Input Current High Level at Clock | $I_{IH5}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 3-11) Note 7 | - | 20 | µA |
| 16 to 17 | Input Current High Level at Clock (Max. Input Voltage) | $I_{IH6}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 7.0V (Pins 3-11) Note 7 | - | 100 | µA |
| 18 to 25 | Input Clamp Voltage | $V_{IC}$ | 3009 | 4(b) | $V_{CC}$ = 4.5V, $I_{IN}$ = -18mA (Pins 1-2-3-4-10-11-12-13) Note 2 | - | -1.5 | V |
| 26 to 29 | Input Current Low Level at D or Clock | $I_{IL1}$ | 3009 | 4(c) | $V_{CC}$ = 5.5V, $V_{IN}$ = 0.4V (Pins 2-3-11-12) Note 8 | - | -400 | µA |
| 30 to 33 | Input Current Low Level at $\overline{Clear}$ or $\overline{Preset}$ | $I_{IL2}$ | 3009 | 4(c) | $V_{CC}$ = 5.5V, $V_{IN}$ = 0.4V (Pins 1-4-10-13) Note 8 | - | -800 | µA |
| 34 to 37 | Output Voltage Low Level | $V_{OL}$ | 3007 | 4(d) | $V_{CC}$ = 4.5V, $V_{IH}$ = 2.0V $I_{OL}$ = 4mA, $V_{IL}$ = 0.7V (Pins 5-6-8-9) | - | 0.4 | V |

**NOTES**: See Page 20.

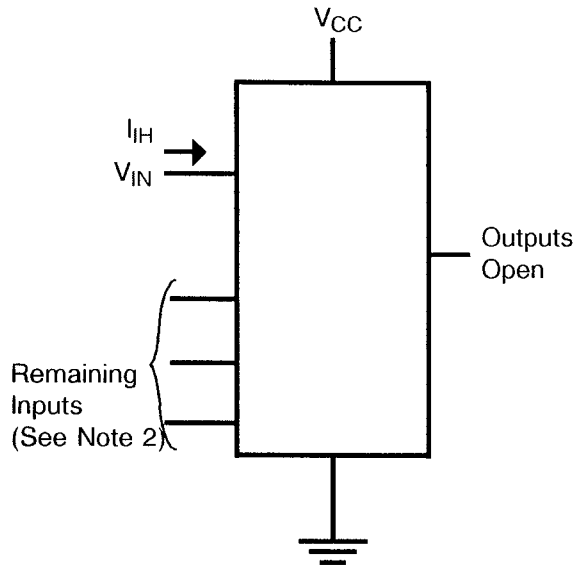
**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125°C AND -55°C (CONTINUED)**

| No. | Characteristics | Symbol | Test Method MIL-STD-883 | Test Fig. | Test Conditions (Pins under Test) | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Max. | |
| 38 to 41 | Output Voltage High Level | $V_{OH}$ | 3006 | 4(e) | $V_{CC}$ = 4.5V, $V_{IH}$ = 2.0V $V_{IL}$ = 0.7V, $I_{OH}$ = -400µA (Pins 5-6-8-9) | 2.5 | - | V |
| 42 to 45 | Output Current Short Circuit | $I_{OS}$ | 3011 | 4(f) | $V_{CC}$ = 5.5V (Pins 5-6-8-9) Note 3 | -15 | -100 | mA |
| 46 to 47 | Supply Current (per Flip-Flop) | $I_{CC}$ | 3005 | 4(g) | $V_{CC}$ = 5.5V, (Pin 14) Note 4 | - | 8 | mA |

**NOTES**: See Page 20.

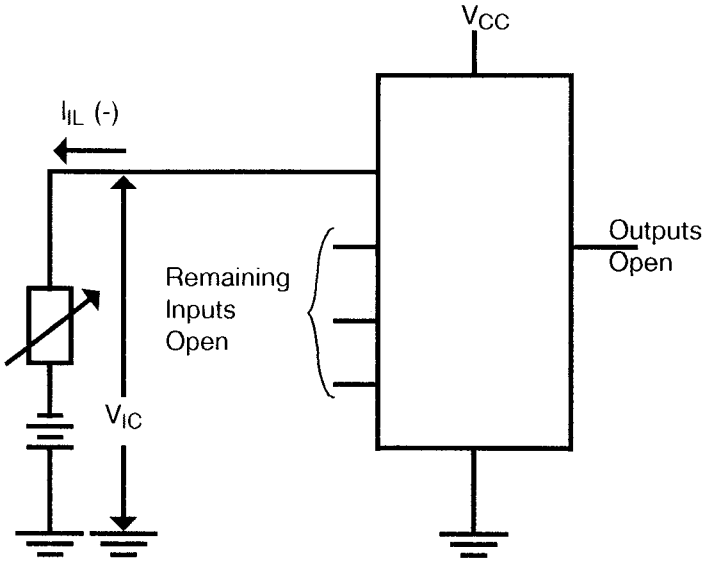
## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - INPUT CURRENT HIGH LEVEL



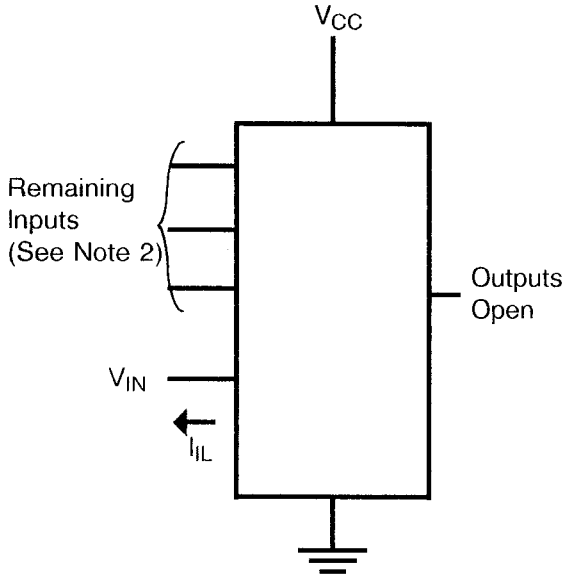

**NOTES** 1. Each input is tested separately.
2. See Note 7 on Page 20.

FIGURE 4(b) - INPUT CLAMP VOLTAGE



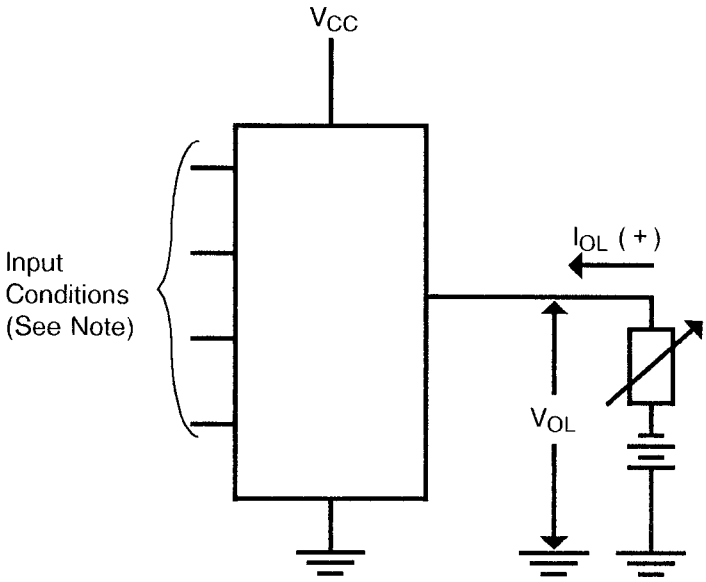

**NOTES** 1. Each input is tested separately.

FIGURE 4(c) - LOW LEVEL INPUT CURRENT




**NOTES** 1. Each input is tested separately.
2. See Note 8 on Page 20.

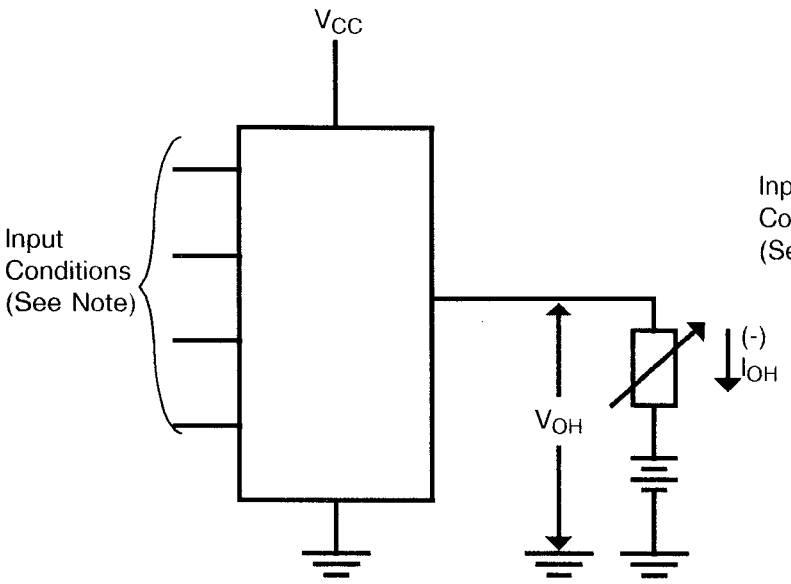
FIGURE 4(d) - LOW LEVEL OUTPUT VOLTAGE




**NOTES** 1. Test per truth table.

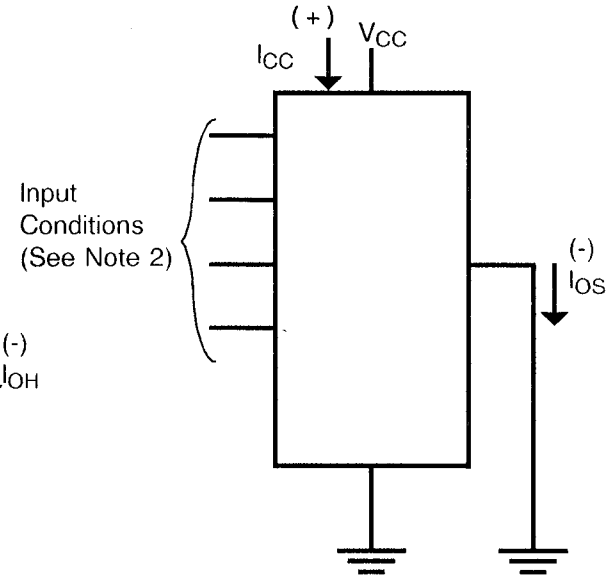
## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - HIGH LEVEL OUTPUT VOLTAGE



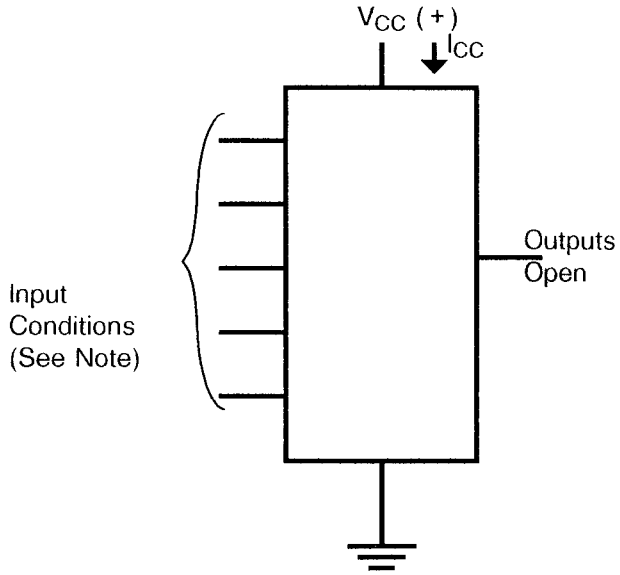

**NOTES**
1. Test per truth table.

FIGURE 4(f) - SHORT CIRCUIT OUTPUT CURRENT




**NOTES**
1. No more than one output should be shorted at a time.
2. For $\bar{Q}$ measurements: $\overline{Preset}$ = 4.5V, all other inputs at ground.
   For Q measurement: $\overline{Preset}$ = 0, Clock and D = 0, $\overline{Clear}$ = 4.5V.

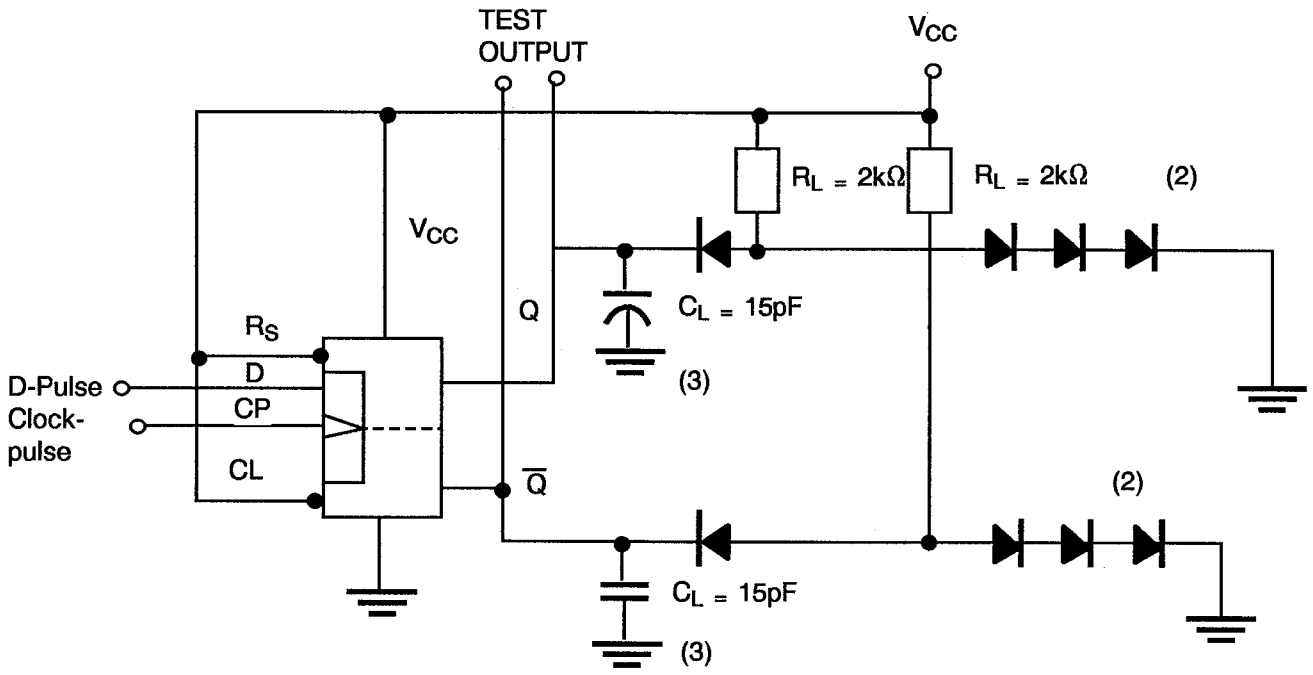
FIGURE 4(g) - SUPPLY CURRENT



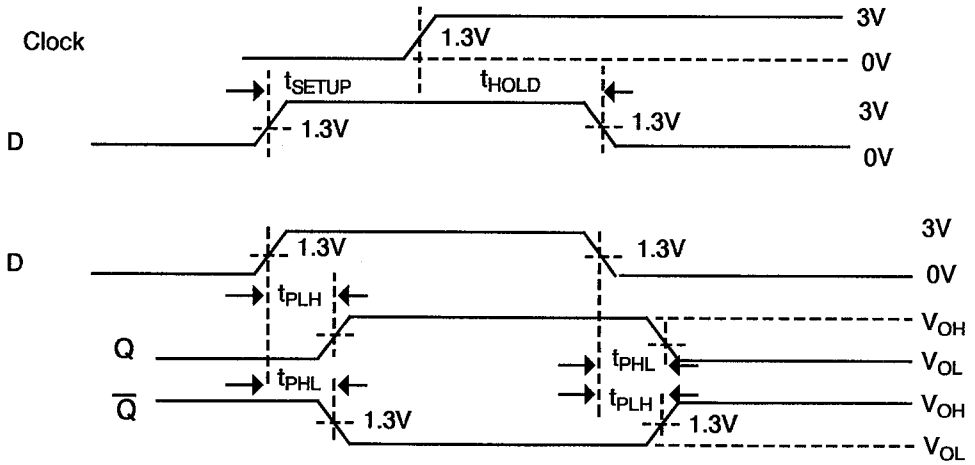

**NOTES**
1. See Note 4 on Page 20.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - DYNAMIC TEST AND SWITCHING WAVEFORMS




VOLTAGE WAVEFORMS




**NOTES**

1. The generator has the following characteristics: $V_{gen}$ = 3.0 ± 0.2V, $t_r$ < 6ns, $t_f$ < 15ns, $t_p$ = 0.5µs, PRR = 1MHz, $Z_{out}$ = 50Ω.
2. All diodes are In 916 or In 3064.
3. $C_L$ = 15pF ±5% including scope probe, wiring and stray capacitance without package in test fixture.
4. Each flip-flop tested separately.

**TABLE 4 - PARAMETER DRIFT VALUES**

| No. | Characteristics | Symbol | Spec. and/or Test Method | Test Conditions | Change Limits (Δ) | Unit |
|---|---|---|---|---|---|---|
| 2, 3 14, 15 | Input Current High Level 1 | $I_{IH1}$ | As per Table 2 | As per Table 2 | ± 0.5 or ± 20 (1) | µA % |
| 26 to 29 | Input Current Low Level | $I_{IL}$ | As per Table 2 | As per Table 2 | ± 18 | µA |
| 34 to 37 | Output Voltage Low Level | $V_{OL}$ | As per Table 2 | As per Table 2 | ± 60 | mV |
| 38 to 41 | Output Voltage High Level | $V_{OH}$ | As per Table 2 | As per Table 2 | ± 240 | mV |

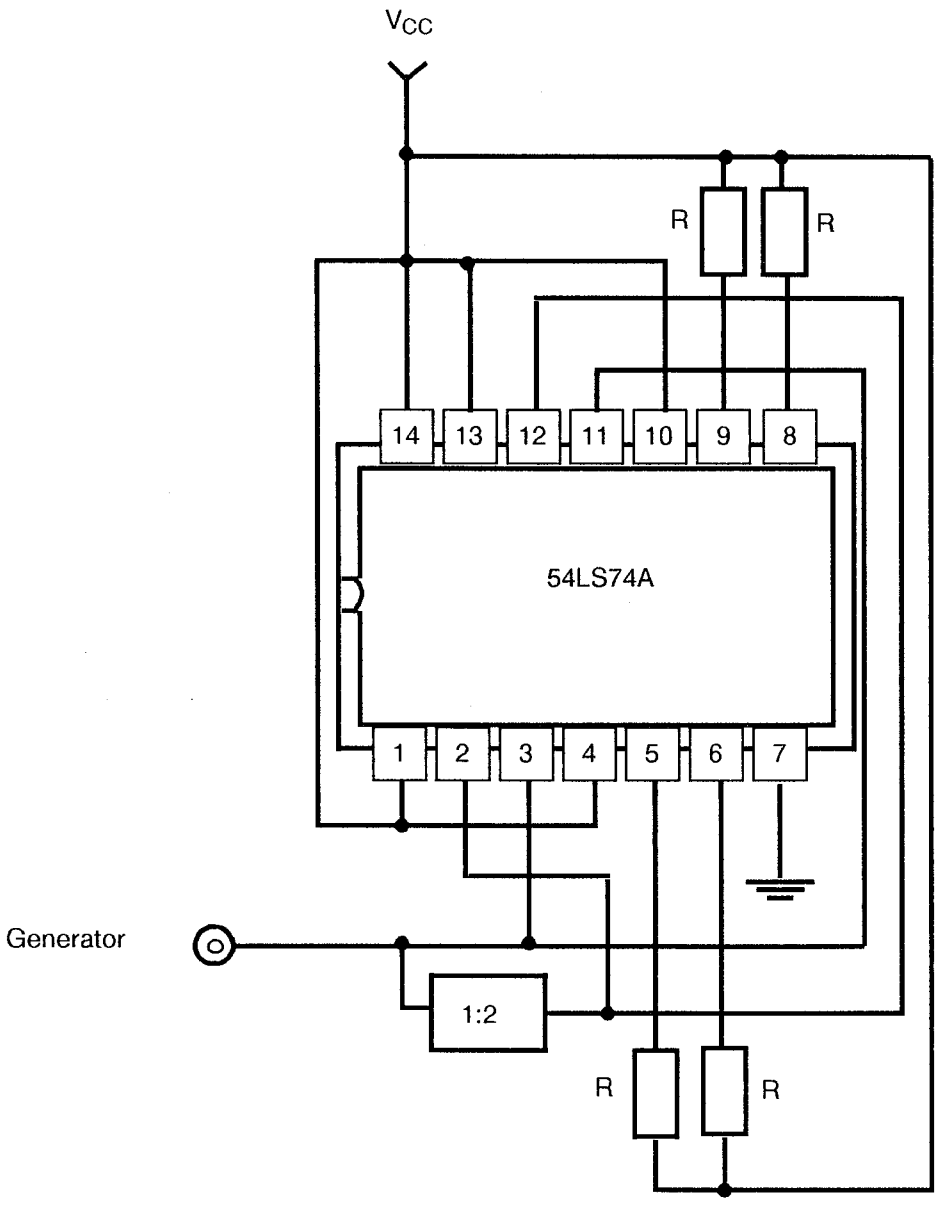
**NOTES** 1. Whichever is greater, referred to the initial value.

**TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST**

| No. | Characteristics | Symbol | Condition | Unit |
|---|---|---|---|---|
| 1 | Ambient Temperature | $T_{amb}$ | + 125( + 0-5) | °C |
| 2 | Power Supply Voltage | $V_{CC}$ | + 5( + 0.5-0) | V |
| 3 | Pulse Voltage | $V_{GEN}$ | 0.5 max to 3.0 min | V |
| 4 | Frequency | f | 100 (Note 1) | Hz |
| 5 | Fan-out | - | 10 | - |
| 6 | Rise Time | $t_r$ | 50 max. | µs |
| 7 | Fall Time | $t_f$ | 50 max. | µs |
| 8 | Duty Cycle | - | 20 min. | % |

**NOTES** 1. Tolerance ± 10%.

**FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST**




**NOTES**

1. R = 1.2kΩ.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb}$ = +22 ±3 °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb}$ = +22 ±3 °C.

4.8.4 Conditions for Operating Life Test

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Test

Circuits for use in performing the operating life test are shown in Figure 5.

4.8.6 Conditions for High Temperature Storage Test

The requirements for high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be Tamb = +150(+0-5) °C.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS**

| No. | Characteristics | Symbol | Spec. and/or Test Method | Test Conditions | Change Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | (Δ) | Absolute | |
| 2, 3 14, 15 | Input Current High Level 1 | $I_{IH1}$ | As per Table 2 | As per Table 2 | ± 1.0 | - | µA |
| 4,5 16, 17 | Input Current High Level 2 (Max. Input Voltage) | $I_{IH2}$ | As per Table 2 | As per Table 2 | - | 100 | µA |
| 26 to 29 | Input Current Low Level | $I_{IL}$ | As per Table 2 | As per Table 2 | ± 12 | - | µA |
| 34 to 37 | Output Voltage Low Level | $V_{OL}$ | As per Table 2 | As per Table 2 | ± 60 | - | mV |
| 38 to 41 | Output Voltage High Level | $V_{OH}$ | As per Table 2 | As per Table 2 | ± 240 | - | mV |
| 46 to 47 | Supply Current | $I_{CC}$ | As per Table 2 | As per Table 2 | ± 20 | - | % |

## APPENDIX 'A'



AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (FRANCE)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|---|---|
| Para. 4.2.1 | Scanning Electron Microscope (S.E.M.) Inspection may be performed using TIF document TIF 3.61.610.001. |
| Para. 4.2.2 | Prior to Die Shear Test TIF may perform a Radiographic Inspection on the randomly chosen samples to be subjected to this test, using TIF document TIF 50.42-3002. |
| Para. 4.2.3 | Radiographic Inspection may be performed using TIF document TIF 50.42-3002. |
| Table 3, Tests 34 to 41 | Electrical measurement may be performed with $V_{IL}$ = 600mV for $V_{OL}$ and $V_{OH}$ testing. |