INTEGRATED CIRCUITS, SILICON MONOLITHIC, SPARC V8 GNSS CONTROLLER

BASED ON TYPE AT7991

ESCC Detail Specification No. 9512/005

Issue 1	May 2020

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Method Standard for Microcircuits.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 951200501R

- Detail Specification Reference : 9512005
- Component Type Variant Number : 01 (as required)
- Total Dose Radiation Level Letter : R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 2)
01	AT7991	CQFP-352	D2 (Note 1)	27	R [100krad(Si)]

NOTES:

1. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in the Test Methods and Procedures of the applicable ESCC generic specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.3 to 2 -0.3 to 4	V	Notes 1, 2
I/O Input Voltage Range	V_{IN}	-0.3 to 2.25	V	Note 2
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	1	°C/W	
Soldering Temperature	T_{sol}	+345	°C	Note 3

NOTES:

1. V_{DD} is for core. V_{CC} is for I/O.
2. With reference to V_{SS} = 0V.
3. Duration 10 seconds maximum at a distance of not less than 1.6 mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

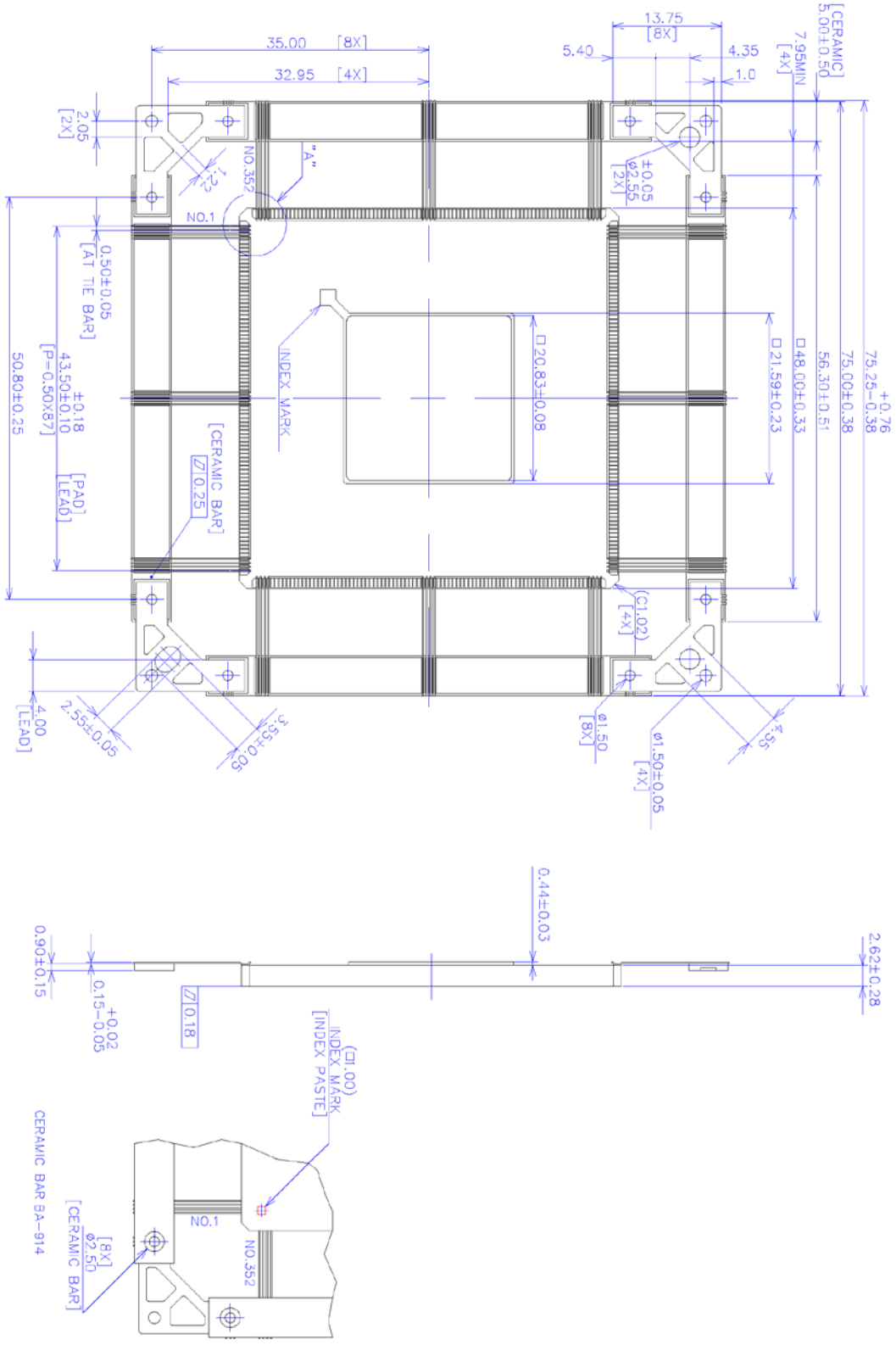
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

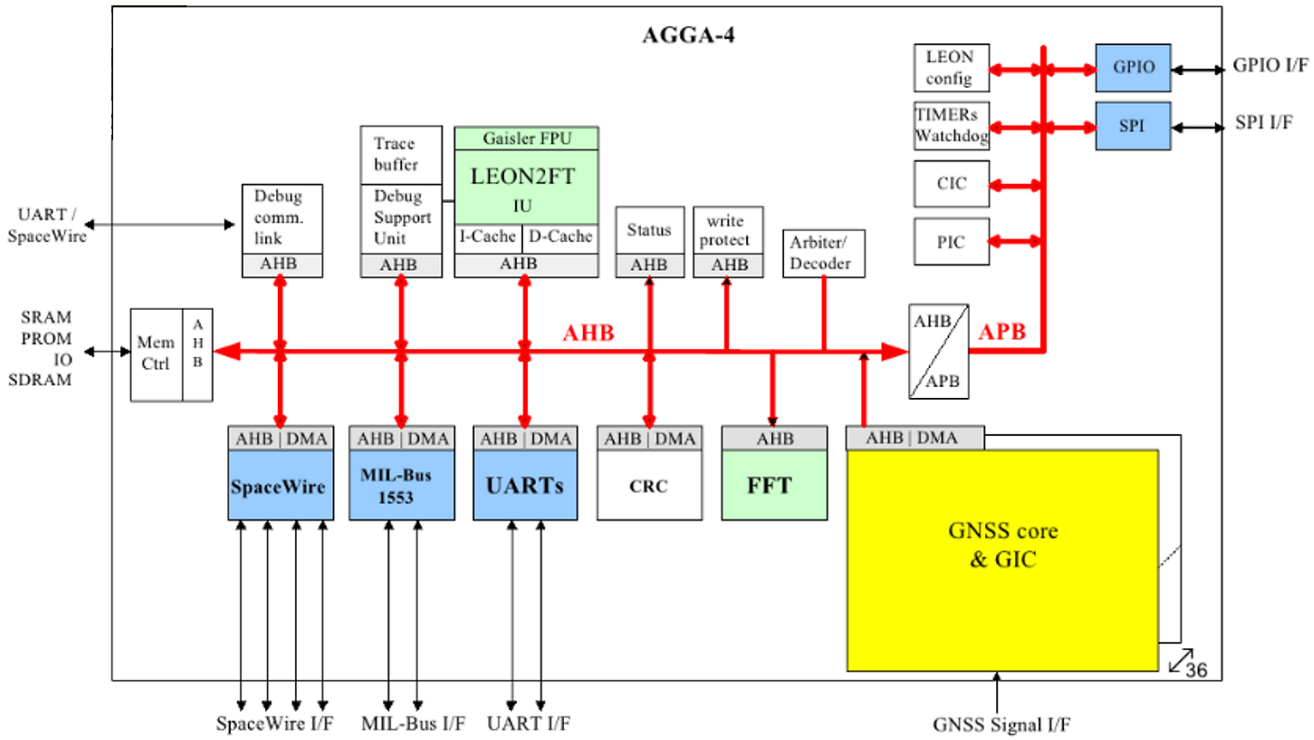
Multi-Deck Ceramic Quad Flat Package (CQFP-352) – 352 Tied Leads



NOTES:

1. Terminal identification is specified by reference to the index mark and detail “A” as shown.

1.8 FUNCTIONAL DIAGRAM



Legend:

: GNSS Core

: External Interfaces

: Internal Interface

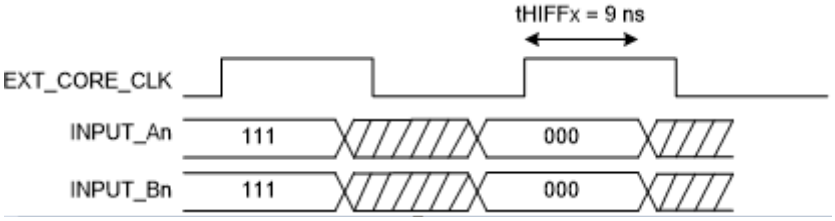
: On-chip Modules

1.9 PIN ASSIGNMENT

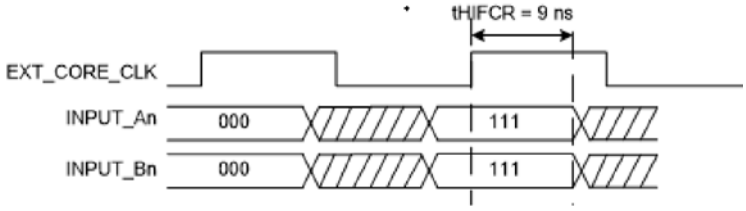
Pin	Signal	Pin	Signal	Pin	Signal
1	Not connected	61	WDOG_N	121	PVDDB11
2	SYS_PLL_BYPASS	62	WDOG_RST_N	122	PVSSB11
3	TEST_EN	63	DSU_SPW_TX_D	123	IOS_N
4	SCAN_EN	64	DSU_SPW_TX_S	124	RAMS_N[0]
5	TRST_N	65	EXT_SYS_CLK	125	RAMS_N[1]
6	TCK	66	DSU_SPW_RX_D	126	RAMS_N[2]
7	VSS1	67	DSU_SPW_RX_S	127	RAMS_N[3]
8	VDD1	68	Not connected	128	RAMS_N[4]
9	TDO	69	PVSSPLL1	129	PVDDB12
10	TMS	70	PVDDPLL1	130	PVSSB12
11	TDI	71	PVDDB5	131	ROMS_N[0]
12	UART0_RX	72	PVSSB5	132	ROMS_N[1]
13	UART0_TX	73	ADDRESS[0]	133	RAMOE_N[1]
14	UART1_RX	74	ADDRESS[1]	134	OE_N
15	UART1_TX	75	ADDRESS[2]	135	WRITE_N
16	SPI_IN_CLK	76	ADDRESS[3]	136	RAMOE_N[0]
17	SPI_OUT_CLK	77	ADDRESS[4]	137	Not connected
18	MOSI	78	ADDRESS[5]	138	PVDDB13
19	MISO	79	PVSSB6	139	PVSSB13
20	SPI_SEL_N[0]	80	PVDDB6	140	DATA[0]
21	SPI_SEL_N[1]	81	VSS1	141	DATA[1]
22	SPI_SEL_N[2]	82	VDD1	142	DATA[2]
23	SPI_SEL_N[3]	83	PVSSPLL2	143	DATA[3]
24	PVDDB1	84	PVDDPLL2	144	DATA[4]
25	PVSSB1	85	Not connected	145	PVDDB14
26	SPW_RX_D[0]	86	ADDRESS[6]	146	PVSSB14
27	SPW_RX_S[0]	87	MIL_PLL_LOCK	147	DATA[5]
28	GPIO[7]	88	EXT_MIL_CLK	148	DATA[6]
29	SPW_TX_D[0]	89	SYS_PLL_LOCK	149	DATA[7]
30	SPW_TX_S[0]	90	ADDRESS[7]	150	DATA[8]
31	GPIO[8]	91	PVSSB7	151	DATA[9]
32	SPW_RX_D[1]	92	PVDDB7	152	PVDDB15
33	SPW_RX_S[1]	93	ADDRESS[8]	153	PVSSB15
34	PVDDB2	94	ADDRESS[9]	154	DATA[10]
35	PVSSB2	95	VSS1	155	DATA[11]
36	SPW_TX_D[1]	96	VDD1	156	DATA[12]
37	SPW_TX_S[1]	97	ADDRESS[10]	157	DATA[13]
38	GPIO[9]	98	ADDRESS[11]	158	DATA[14]
39	SPW_RX_D[2]	99	ADDRESS[12]	159	PVDDB16
40	SPW_RX_S[2]	100	PVDDB8	160	PVSSB16
41	GPIO[10]	101	PVSSB8	161	DATA[15]
42	SPW_TX_D[2]	102	ADDRESS[13]	162	DATA[16]
43	SPW_TX_S[2]	103	ADDRESS[14]	163	DATA[17]
44	PVDDB3	104	ADDRESS[15]	164	DATA[18]
45	PVSSB3	105	ADDRESS[16]	165	DATA[19]
46	GPIO[11]	106	ADDRESS[17]	166	PVDDB17
47	SPW_RX_D[3]	107	PVDDB9	167	PVSSB17
48	SPW_RX_S[3]	108	PVSSB9	168	DATA[20]
49	GPIO[12]	109	ADDRESS[18]	169	VSS1
50	SPW_TX_D[3]	110	ADDRESS[19]	170	VDD1
51	SPW_TX_S[3]	111	ADDRESS[20]	171	DATA[21]
52	DSU_UART_RX	112	ADDRESS[21]	172	DATA[22]
53	DSU_UART_TX	113	ADDRESS[22]	173	DATA[23]
54	AGGA4_RESET_N	114	PVDDB10	174	DATA[24]
55	PWR_ON_RESET_N	115	PVSSB10	175	PVSSB18
56	DSU_SPW_EN	116	ADDRESS[23]	176	PVDDB18
57	ERROR_N	117	ADDRESS[24]	177	DATA[25]
58	NMI_INT	118	ADDRESS[25]	178	DATA[26]
59	PVDDB4	119	ADDRESS[26]	179	DATA[27]
60	PVSSB4	120	ADDRESS[27]	180	DATA[28]

Pin	Signal	Pin	Signal	Pin	Signal
181	DATA[29]	241	SCAN_IN[3]	301	PIO[3]
182	SCAN_IN[0]	242	CODE_OUT1[0]	302	PIO[4]
183	VSS1	243	CODE_OUT1[1]	303	PIO[5]
184	VDD1	244	SYS_PLL_ICP[0]	304	PIO[6]
185	PVDDB19	245	SYS_PLL_ICP[1]	305	PIO[7]
186	PVSSB19	246	MIL_PLL_ICP[0]	306	PIO[8]
187	DATA[30]	247	MIL_PLL_ICP[1]	307	PIO[9]
188	DATA[31]	248	PVDDB30	308	PIO[10]
189	CB[0]	249	PVSSB30	309	PIO[11]
190	CB[1]	250	GPIO[13]	310	PIO[12]
191	PVSSB20	251	GPIO[14]	311	PIO[13]
192	CB[2]	252	EEPROM_RESET_N	312	PIO[14]
193	PVDDB20	253	EEPROM_ENABLE	313	PIO[15]
194	CB[3]	254	SYS_PLL_FREQSEL[0]	314	GPIO[0]
195	CB[4]	255	SYS_PLL_FREQSEL[1]	315	GPIO[1]
196	CB[5]	256	GPIO[15]	316	GPIO[2]
197	PVDDB21	257	VSS1	317	GPIO[3]
198	PVSSB21	258	VDD1	318	PVDDB27
199	CB[6]	259	EEPROM_POWER	319	PVSSB27
200	BEXC_N	260	SCAN_IN[4]	320	GPIO[4]
201	BRDY_N	261	SCAN_IN[5]	321	GPIO[5]
202	SGPO	262	SCAN_IN[6]	322	GPIO[6]
203	RWE_N[0]	263	SCAN_IN[7]	323	SCAN_IN[9]
204	RWE_N[1]	264	SCAN_IN[8]	324	ASC[0]
205	RWE_N[2]	265	EXT_CORE_CLK	325	ASC[1]
206	RWE_N[3]	266	GNSS_RESET_N	326	ASEO
207	READ	267	HALF_SAMPLE_CLK	327	ASEI
208	PVSSB22	268	INPUT_A0[0]	328	MEO
209	PVDDB22	269	PVDDB25	329	MEI
210	MIL_RX0	270	PVSSB25	330	SCAN_IN[10]
211	MIL_RX0B	271	VSS1	331	SCAN_IN[11]
212	MIL_TX0	272	VDD1	332	PPSO
213	MIL_TX0B	273	INPUT_A0[1]	333	PPSI
214	DSU_ACT	274	INPUT_A0[2]	334	EXT_CLK
215	DSU_BRE	275	INPUT_A1[0]	335	AU_TRIGGER
216	DSU_EN	276	INPUT_A1[1]	336	SYS_CLK_OUT
217	MIL_TX0INH	277	INPUT_A1[2]	337	PVDDB28
218	MIL_RX1	278	INPUT_A2[0]	338	PVSSB28
219	MIL_RX1B	279	INPUT_A2[1]	339	DA_OUT[0]
220	MIL_TX1	280	INPUT_A2[2]	340	DA_OUT[1]
221	MIL_TX1B	281	INPUT_A3[0]	341	DA_OUT[2]
222	PVSSB23	282	INPUT_A3[1]	342	DA_OUT[3]
223	PVDDB23	283	INPUT_A3[2]	343	IMT_12
224	MIL_TX1INH	284	INPUT_B0[0]	344	SYS_CLK_DIV[0]
225	SCAN_IN[1]	285	INPUT_B0[1]	345	VSS1
226	MIL_RESET_OUT_N	286	INPUT_B0[2]	346	VDD1
227	SIGNAL_OUT_I[0]	287	INPUT_B1[0]	347	SYS_CLK_DIV[1]
228	SIGNAL_OUT_I[1]	288	INPUT_B1[1]	348	SYS_CLK_DIV[2]
229	SIGNAL_OUT_I[2]	289	INPUT_B1[2]	349	SYS_CLK_DIV[3]
230	SIGNAL_OUT_Q[0]	290	INPUT_B2[0]	350	PVDDB29
231	SIGNAL_OUT_Q[1]	291	INPUT_B2[1]	351	PVSSB29
232	SIGNAL_OUT_Q[2]	292	INPUT_B2[2]	352	MIL_CLK_OUT
233	PVDDB24	293	INPUT_B3[0]		
234	PVSSB24	294	PVDDB26		
235	INT_EPOCH1	295	PVSSB26		
236	CODE_OUT2[0]	296	INPUT_B3[1]		
237	CODE_OUT2[1]	297	INPUT_B3[2]		
238	INT_EPOCH2	298	PIO[0]		
239	SPI_SEL_N[4]	299	PIO[1]		
240	SCAN_IN[2]	300	PIO[2]		

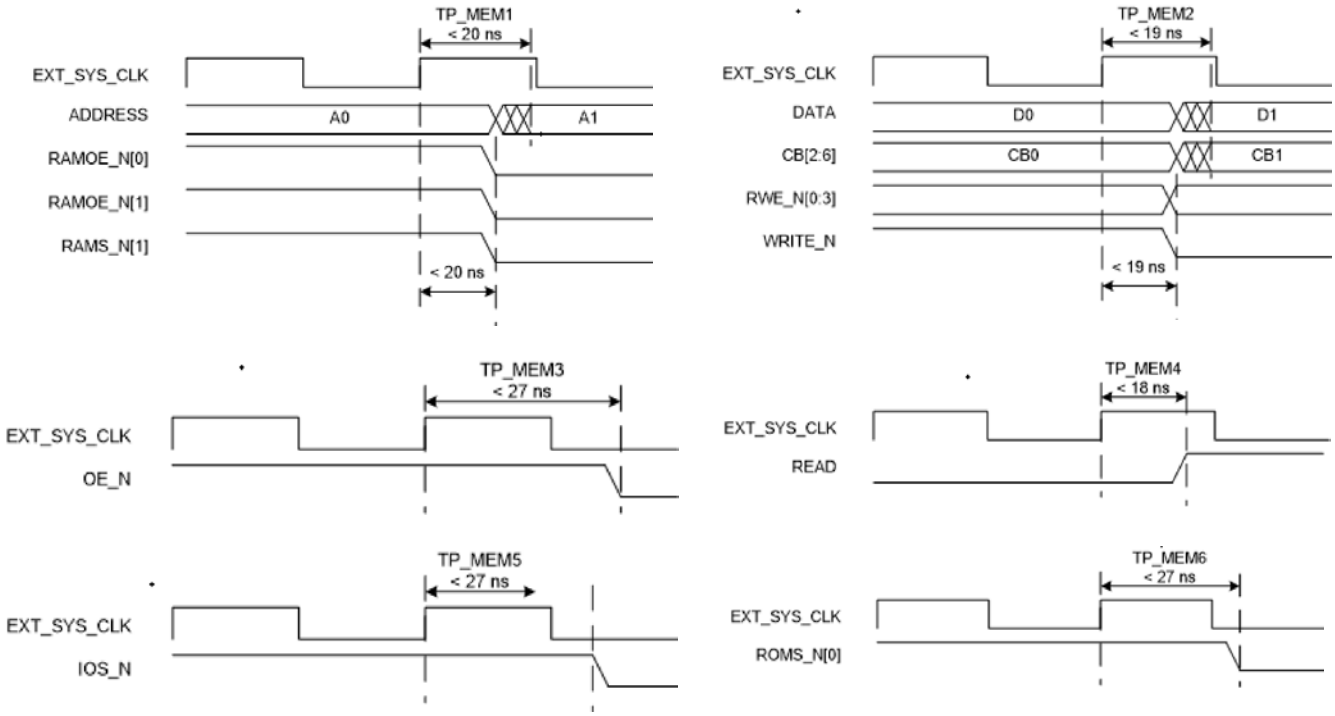
1.10 INSTRUCTION SET AND TIMING DIAGRAMS



HHIFFx timings

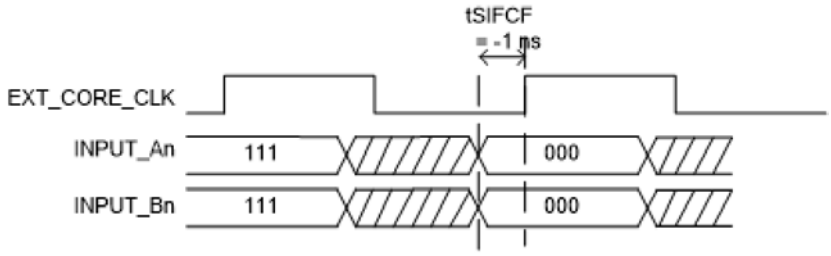


THIFCRx timings

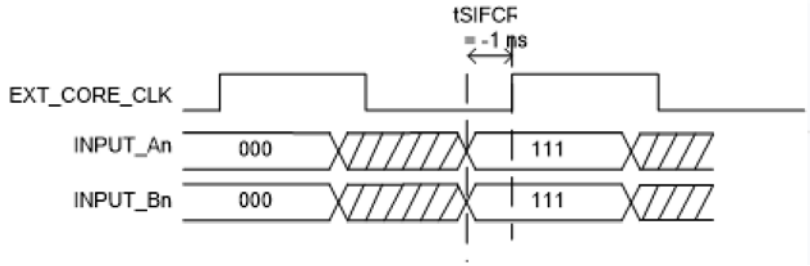


TP_MEMx timings

TSDDCx timings

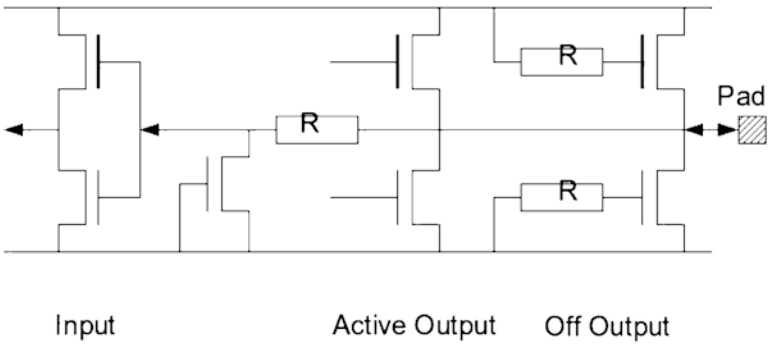


TSIFCFx timings



TSIFCRx timings

1.11 PROTECTION NETWORK



NOTES:

1. The ratio of Active Output to Off Output determines the output strength.
2. Resistors R are approximately 460Ω each.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests

High temperature reverse bias burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified component only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions 1.65V < V_{DD} < 1.95V 3V < V_{CC} < 3.6V (Note 1)	Limits		Units
				Min	Max	
Functional Tests (Min.)	-	3014	V_{DD} = 1.65V V_{CC} = 3V V_{IH} = V_{DD} V_{IL} = V_{SS}	-	-	-
Functional Tests (Typ.)	-	3014	V_{DD} = 1.8V V_{CC} = 3.3V V_{IH} = V_{DD} V_{IL} = V_{SS}	-	-	-
Functional Tests (Max.)	-	3014	V_{DD} = 1.95V V_{CC} = 3.6V V_{IH} = V_{DD} V_{IL} = V_{SS}	-	-	-
Low Level Input Voltage	V_{IL}	-	CMOS buffers	-	800	mV
High Level Input Voltage	V_{IH}	-	CMOS buffers	2	-	V
High Level Output Voltage	V_{OH}	3006	CMOS buffers I_{OH} = -2, -4, -8, -12, -16mA	V_{CC}-0.4	-	V
Low Level Output Voltage	V_{OL}	3006	CMOS buffers I_{OL}= 2, 4, 8, 12, 16mA	-	400	mV
Low Level Input Current	I_{IL}	3009	CMOS buffers V_{IN} = V_{SS}	-1	1	µA
Low Level Input Current with Pull-down	I_{ILPD}	3009	CMOS buffers V_{IN} = V_{SS}	-5	5	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions 1.65V < V_{DD} < 1.95V 3V < V_{CC} < 3.6V (Note 1)	Limits		Units
				Min	Max	
Low Level Input Current with Pull-up	I_{ILPU}	3009	CMOS buffers V_{IN} = V_{SS}	-400	-	µA
High Level Input Current	I_{IH}	3010	CMOS buffers V_{IN} = V_{CC} max	-1	1	µA
High Level Input Current with Pull-up	I_{IHPU}	3010	CMOS buffers V_{IN} = V_{CC} max	-5	5	µA
High Level Input Current with Pull-down	I_{IHPD}	3010	CMOS buffers V_{IN} = V_{CC} max	-	600	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	3020	CMOS buffers V_{IN} = V_{SS}	-1	1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	CMOS buffers V_{IN} = V_{CC} max	-1	1	µA
Array Stand-by Current	I_{CCSBA}	3005	V_{DD} max Output = 0mA Note 4	-	34	mA
Array Operating Current (all GNSS channels deactivated)	I_{CCOP1} POWER0	3005	V_{DD} max V_{CC} max GNSS clock = 2MHz System clock = 4MHz	-	100	mA
Array Operating Current (all 18 GNSS channels active)	I_{CCOP2} POWER18	3005	V_{DD} max V_{CC} max GNSS clock = 2MHz System clock = 4MHz	-	100	mA
Array Operating Current (all 36 GNSS channels active)	I_{CCOP3} POWER36	3005	V_{DD} max V_{CC} max GNSS clock = 2MHz System clock = 4MHz	-	200	mA
Array Operating Current (only GNSS clocks without SYS_CLK)	I_{CCOP4} POWER_G	3005	V_{DD} max V_{CC} max GNSS clock = 2MHz System clock = 4MHz	-	100	mA
Input Pin Capacitance (Note 2)	C_{I33}	3012	CMOS buffers	-	7	pF
Hold Time (EXT_CORE_CLK / GROUP_INPUT_0 GROUP_SIGNAL_OUT)	t_{HIFF0}	3003	Note 3	-	9	ns
Hold Time (EXT_CORE_CLK / GROUP_INPUT_1 GROUP_SIGNAL_OUT)	t_{HIFF1}	3003	Note 3	-	9	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions 1.65V < V_{DD} < 1.95V 3V < V_{CC} < 3.6V (Note 1)	Limits		Units
				Min	Max	
Hold Time (EXT_CORE_CLK / GROUP_INPUT_2 GROUP_SIGNAL_OUT)	t_{HIFF2}	3003	Note 3	-	9	ns
Hold Time (EXT_CORE_CLK / GROUP_INPUT_3 GROUP_SIGNAL_OUT)	t_{HIFF3}	3003	Note 3	-	9	ns
Hold Time (EXT_CORE_CLK / GROUP_INPUT_0 GROUP_SIGNAL_OUT)	t_{HIFCR0}	3003	Note 3	-	9	ns
Hold Time (EXT_CORE_CLK / GROUP_INPUT_1 GROUP_SIGNAL_OUT)	t_{HIFCR1}	3003	Note 3	-	9	ns
Hold Time (EXT_CORE_CLK / GROUP_INPUT_2 GROUP_SIGNAL_OUT)	t_{HIFCR2}	3003	Note 3	-	9	ns
Hold Time (EXT_CORE_CLK / GROUP_INPUT_3 GROUP_SIGNAL_OUT)	t_{HIFCR3}	3003	Note 3	-	9	ns
Propagation Time (EXT_SYS_CLK / GROUP_OUT_MEM1)	t_{P_MEM1}	3003	Note 3	-	20	ns
Propagation Time (EXT_SYS_CLK / GROUP_OUT_MEM2)	t_{P_MEM2}	3003	Note 3	-	19	ns
Propagation Time (EXT_SYS_CLK / OE_N)	t_{P_MEM3}	3003	Note 3	-	27	ns
Propagation Time (EXT_SYS_CLK / READ/2/3/)	t_{P_MEM4}	3003	Note 3	-	18	ns
Propagation Time (EXT_SYS_CLK / IOS_N)	t_{P_MEM5}	3003	Note 3	-	27	ns
Propagation Time (EXT_SYS_CLK / ROMS_N[0])	t_{P_MEM6}	3003	Note 3	-	27	ns
Propagation Time (EXT_SYS_CLK / GROUP_OUT_SPW1)	t_{P_SPW1}	3003	Note 3	-	24	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions 1.65V < V_{DD} < 1.95V 3V < V_{CC} < 3.6V (Note 1)	Limits		Units
				Min	Max	
Propagation Time (EXT_SYS_CLK / GROUP_OUT_SPW2)	t_{P_SPW2}	3003	Note 3	-	24	ns
DDC Mode						
Setup Time (HALF_SAMPLE_CLK / GROUP_INPUT_A GROUP_SIGNAL_OUT)	t_{SDDC1}	3003	Notes 3, 5	-	3	ns
Setup Time (HALF_SAMPLE_CLK / INPUT_B0[2] GROUP_SIGNAL_OUT)	t_{SDDC2}	3003	Notes 3, 5	-	3	ns
IFC Mode						
Setup Time (EXT_CORE_CLK / GROUP_INPUT_0 GROUP_SIGNAL_OUT)	t_{SIFCF0}	3003	Notes 3, 5	-	-1	ns
Setup Time (EXT_CORE_CLK / GROUP_INPUT_1 GROUP_SIGNAL_OUT)	t_{SIFCF1}	3003	Notes 3, 5	-	-1	ns
Setup Time (EXT_CORE_CLK / GROUP_INPUT_2 GROUP_SIGNAL_OUT)	t_{SIFCF2}	3003	Notes 3, 5	-	-1	ns
Setup Time (EXT_CORE_CLK / GROUP_INPUT_3 GROUP_SIGNAL_OUT)	t_{SIFCF3}	3003	Notes 3, 5	-	-1	ns
Setup Time (EXT_CORE_CLK / GROUP_INPUT_0 GROUP_SIGNAL_OUT)	t_{SIFCR0}	3003	Notes 3, 5	-	-1	ns
Setup Time (EXT_CORE_CLK / GROUP_INPUT_1 GROUP_SIGNAL_OUT)	t_{SIFCR1}	3003	Notes 3, 5	-	-1	ns
Setup Time (EXT_CORE_CLK / GROUP_INPUT_2 GROUP_SIGNAL_OUT)	t_{SIFCR2}	3003	Notes 3, 5	-	-1	ns
Setup Time (EXT_CORE_CLK / GROUP_INPUT_3 GROUP_SIGNAL_OUT)	t_{SIFCR3}	3003	Notes 3, 5	-	-1	ns

NOTES:

1. Unless otherwise specified, all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be V_{IN} = V_{SS} or V_{CC} and outputs not under test shall be open. V_{SS} = 0V.
2. Guaranteed, not tested.
3. Test conditions: Tester load = 5pF, V_{IL} = 0V, V_{IH} = V_{DD}, Input signals dynamic characteristics: t_r, t_f < 10ns, Threshold voltages: V_{OL} = V_{OH} = V_{DD}/2.
4. Inputs shall be configured in state corresponding to the minimum standby current.
5. Group definitions shall be as follows:

```
(GROUP GROUP_OUT_MEM1 ADDRESS[4] ADDRESS[5] ADDRESS[6]
                      ADDRESS[7] ADDRESS[8] ADDRESS[10] ADDRESS[11] ADDRESS[12]
                       ADDRESS[14] ADDRESS[15] ADDRESS[16] ADDRESS[17]
                       ADDRESS[18] ADDRESS[19] ADDRESS[20]
                      ADDRESS[22] RAMOE_N[0] RAMOE_N[1] RAMS_N[0])

(GROUP GROUP_OUT_MEM2 DATA[0] DATA[1]  DATA[2]  DATA[3]  DATA[4]  DATA[5]
                      DATA[6] DATA[7]  DATA[8]  DATA[9]
                      DATA[10] DATA[11] DATA[12] DATA[13] DATA[14]
                      DATA[15] DATA[16] DATA[17] DATA[18] DATA[19]
                      DATA[20] DATA[21] DATA[22] DATA[23] DATA[24]
                      DATA[25] DATA[26] DATA[27] DATA[28] DATA[29]
                      DATA[30] DATA[31]
                      CB[1] CB[2] CB[3] CB[4] CB[5] CB[6]
                      RWE_N[0] RWE_N[1] RWE_N[2] RWE_N[3] WRITE_N)

(GROUP GROUP_OUT_SPW1 SPW_TX_S[3] SPW_TX_S[2] SPW_TX_S[0] DSU_SPW_TX_D)
(GROUP GROUP_OUT_SPW2 SPW_TX_S[0] SPW_TX_D[2] SPW_TX_D[3] DSU_SPW_TX_S)

(GROUP GROUP_INPUT_0 INPUT_A0[0] INPUT_A0[1] INPUT_A0[2]
                       INPUT_B0[0] INPUT_B0[1] INPUT_B0[2] )
(GROUP GROUP_INPUT_1 INPUT_A1[0] INPUT_A1[1] INPUT_A1[2]
                       INPUT_B1[0] INPUT_B1[1] INPUT_B1[2] )
(GROUP GROUP_INPUT_2 INPUT_A2[0] INPUT_A2[1] INPUT_A2[2]
                       INPUT_B2[0] INPUT_B2[1] INPUT_B2[2] )
(GROUP GROUP_INPUT_3 INPUT_A3[0] INPUT_A3[1] INPUT_A3[2]
                       INPUT_B3[0] INPUT_B3[1] INPUT_B3[2] )

(GROUP GROUP_INPUT_A INPUT_A0[0] INPUT_A0[1] INPUT_A0[2]
                       INPUT_A1[0] INPUT_A1[1] INPUT_A1[2]
                       INPUT_A2[0] INPUT_A2[1] INPUT_A2[2]
                       INPUT_A3[0] INPUT_A3[1] INPUT_A3[2])

(GROUP GROUP_SIGNAL_OUT SIGNAL_OUT_I[0] SIGNAL_OUT_I[1] SIGNAL_OUT_I[2]
                        SIGNAL_OUT_Q[0] SIGNAL_OUT_Q[1] SIGNAL_OUT_Q[2])
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2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Array Stand-by Current	I_{CCSBA}	±3.4	-	34	mA
Low Level Input Current	I_{IL}	±0.1	-1	1	µA
High Level Input Current	I_{IH}	±0.1	-1	1	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.1	-1	1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.1	-1	1	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	V_{CC}-0.4	-	V

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125(+0 -3)	°C
Core Supply Voltage	V_{DD}	1.95	V
I/O Supply Voltage	V_{CC}	3.7	V
Forcing Inputs	S1 (Note 1)	1.65	MHz
	S4 (Note 2)	206.25	kHz

NOTES:

1. 6 pins connected, as shown in the pin connections table below.
2. 136 pins connected, as shown in the pin connections table below.

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
2	SYS_PLL_BYPASS	2.2kΩ	V_{SS}	179	DATA[27]	2.2kΩ	S4
3	TEST_EN	2.2kΩ	V_{CC}	180	DATA[28]	2.2kΩ	S4
4	SCAN_EN	2.2kΩ	V_{CC}	181	DATA[29]	2.2kΩ	S4
5	TRST_N	2.2kΩ	V_{SS}	182	SCAN_IN[0]	2.2kΩ	S4
6	TCK	2.2kΩ	S1	183	VSSA	0Ω	V_{SS}
7	VSSA	0Ω	V_{SS}	184	VDDA	0Ω	V_{DD}
8	VDDA	0Ω	V_{DD}	185	PVDDB19	0Ω	V_{CC}
9	TDO	5.6kΩ	V_{CC}-V_{SS}	186	PVSSB19	0Ω	V_{SS}
10	TMS	2.2kΩ	S4	187	DATA[30]	2.2kΩ	S4
11	TDI	2.2kΩ	S4	188	DATA[31]	2.2kΩ	S4
12	UART0_RX	2.2kΩ	S4	189	CB[0]	2.2kΩ	S4
13	UART0_TX	5.6kΩ	V_{CC}-V_{SS}	190	CB[1]	2.2kΩ	S4
14	UART1_RX	2.2kΩ	S4	191	PVSSB20	0Ω	V_{SS}
15	UART1_TX	5.6kΩ	V_{CC}-V_{SS}	192	CB[2]	2.2kΩ	S4
16	SPI_IN_CLK	2.2kΩ	S4	193	PVDDB20	0Ω	V_{CC}
17	SPI_OUT_CLK	5.6kΩ	V_{CC}-V_{SS}	194	CB[3]	2.2kΩ	S4
18	MOSI	5.6kΩ	V_{CC}-V_{SS}	195	CB[4]	2.2kΩ	S4
19	MISO	2.2kΩ	S4	196	CB[5]	2.2kΩ	S4
20	SPI_SEL_N[0]	5.6kΩ	V_{CC}-V_{SS}	197	PVDDB21	0Ω	V_{CC}
21	SPI_SEL_N[1]	5.6kΩ	V_{CC}-V_{SS}	198	PVSSB21	0Ω	V_{SS}
22	SPI_SEL_N[2]	5.6kΩ	V_{CC}-V_{SS}	199	CB[6]	2.2kΩ	S4
23	SPI_SEL_N[3]	5.6kΩ	V_{CC}-V_{SS}	200	BEXC_N	2.2kΩ	S4
24	PVDDB1	0Ω	V_{CC}	201	BRDY_N	2.2kΩ	S4
25	PVSSB1	0Ω	V_{SS}	202	SGPO	5.6kΩ	V_{CC}-V_{SS}
26	SPW_RX_D[0]	2.2kΩ	S4	203	RWE_N[0]	5.6kΩ	V_{CC}-V_{SS}
27	SPW_RX_S[0]	2.2kΩ	S4	204	RWE_N[1]	5.6kΩ	V_{CC}-V_{SS}
28	GPIO[7]	5.6kΩ	V_{CC}-V_{SS}	205	RWE_N[2]	5.6kΩ	V_{CC}-V_{SS}
29	SPW_TX_D[0]	5.6kΩ	V_{CC}-V_{SS}	206	RWE_N[3]	5.6kΩ	V_{CC}-V_{SS}

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
30	SPW_TX_S[0]	5.6kΩ	V_{CC}-V_{SS}	207	READ	5.6kΩ	V_{CC}-V_{SS}
31	GPIO[8]	2.2kΩ	S4	208	PVSSB22	0Ω	V_{SS}
32	SPW_RX_D[1]	2.2kΩ	S4	209	PVDDB22	0Ω	V_{CC}
33	SPW_RX_S[1]	2.2kΩ	S4	210	MIL_RX0	2.2kΩ	S4
34	PVDDB2	0Ω	V_{CC}	211	MIL_RX0B	2.2kΩ	S4
35	PVSSB2	0Ω	V_{SS}	212	MIL_TX0	5.6kΩ	V_{CC}-V_{SS}
36	SPW_TX_D[1]	5.6kΩ	V_{CC}-V_{SS}	213	MIL_TX0B	5.6kΩ	V_{CC}-V_{SS}
37	SPW_TX_S[1]	5.6kΩ	V_{CC}-V_{SS}	214	DSU_ACT	5.6kΩ	V_{CC}-V_{SS}
38	GPIO[9]	5.6kΩ	V_{CC}-V_{SS}	215	DSU_BRE	2.2kΩ	S4
39	SPW_RX_D[2]	2.2kΩ	S4	216	DSU_EN	2.2kΩ	S4
40	SPW_RX_S[2]	2.2kΩ	S4	217	MIL_TX0INH	5.6kΩ	V_{CC}-V_{SS}
41	GPIO[10]	2.2kΩ	S4	218	MIL_RX1	2.2kΩ	S4
42	SPW_TX_D[2]	5.6kΩ	V_{CC}-V_{SS}	219	MIL_RX1B	2.2kΩ	S4
43	SPW_TX_S[2]	5.6kΩ	V_{CC}-V_{SS}	220	MIL_TX1	5.6kΩ	V_{CC}-V_{SS}
44	PVDDB3	0Ω	V_{CC}	221	MIL_TX1B	5.6kΩ	V_{CC}-V_{SS}
45	PVSSB3	0Ω	V_{SS}	222	PVSSB23	0Ω	V_{SS}
46	GPIO[11]	5.6kΩ	V_{CC}-V_{SS}	223	PVDDB23	0Ω	V_{CC}
47	SPW_RX_D[3]	2.2kΩ	S4	224	MIL_TX1INH	5.6kΩ	V_{CC}-V_{SS}
48	SPW_RX_S[3]	2.2kΩ	S4	225	SCAN_IN[1]	2.2kΩ	S4
49	GPIO[12]	2.2kΩ	S4	226	MIL_RESET_OUT_N	5.6kΩ	V_{CC}-V_{SS}
50	SPW_TX_D[3]	5.6kΩ	V_{CC}-V_{SS}	227	SIGNAL_OUT_I[0]	5.6kΩ	V_{CC}-V_{SS}
51	SPW_TX_S[3]	5.6kΩ	V_{CC}-V_{SS}	228	SIGNAL_OUT_I[1]	5.6kΩ	V_{CC}-V_{SS}
52	DSU_UART_RX	2.2kΩ	S4	229	SIGNAL_OUT_I[2]	5.6kΩ	V_{CC}-V_{SS}
53	DSU_UART_TX	5.6kΩ	V_{CC}-V_{SS}	230	SIGNAL_OUT_Q[0]	5.6kΩ	V_{CC}-V_{SS}
54	AGGA4_RESET_N	2.2kΩ	V_{CC}	231	SIGNAL_OUT_Q[1]	5.6kΩ	V_{CC}-V_{SS}
55	PWR_ON_RESET_N	2.2kΩ	V_{CC}	232	SIGNAL_OUT_Q[2]	5.6kΩ	V_{CC}-V_{SS}
56	DSU_SPW_EN	2.2kΩ	S4	233	PVDDB24	0Ω	V_{CC}
57	ERROR_N	5.6kΩ	V_{CC}-V_{SS}	234	PVSSB24	0Ω	V_{SS}
58	NMI_INT	2.2kΩ	S4	235	INT_EPOCH1	5.6kΩ	V_{CC}-V_{SS}
59	PVDDB4	2.2kΩ	V_{CC}	236	CODE_OUT2[0]	5.6kΩ	V_{CC}-V_{SS}
60	PVSSB4	2.2kΩ	V_{SS}	237	CODE_OUT2[1]	5.6kΩ	V_{CC}-V_{SS}
61	WDOG_N	5.6kΩ	V_{CC}-V_{SS}	238	INT_EPOCH2	5.6kΩ	V_{CC}-V_{SS}
62	WDOG_RST_N	5.6kΩ	V_{CC}-V_{SS}	239	SPI_SEL_N[4]	5.6kΩ	V_{CC}-V_{SS}
63	DSU_SPW_TX_D	5.6kΩ	V_{CC}-V_{SS}	240	SCAN_IN[2]	2.2kΩ	S4
64	DSU_SPW_TX_S	5.6kΩ	V_{CC}-V_{SS}	241	SCAN_IN[3]	2.2kΩ	S4
65	EXT_SYS_CLK	2.2kΩ	S1	242	CODE_OUT1[0]	5.6kΩ	V_{CC}-V_{SS}
66	DSU_SPW_RX_D	2.2kΩ	S4	243	CODE_OUT1[1]	5.6kΩ	V_{CC}-V_{SS}
67	DSU_SPW_RX_S	2.2kΩ	S4	244	SYS_PLL_ICP[0]	2.2kΩ	S4
69	PVSSPLL1	0Ω	V_{SS}	245	SYS_PLL_ICP[1]	2.2kΩ	S4
70	PVDDPLL1	0Ω	V_{DD}	246	MIL_PLL_ICP[0]	2.2kΩ	S4

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
71	PVDDB5	0Ω	V_{CC}	247	MIL_PLL_ICP[1]	2.2kΩ	S4
72	PVSSB5	0Ω	V_{SS}	248	PVDDB30	0Ω	V_{CC}
73	ADDRESS[0]	5.6kΩ	V_{CC}-V_{SS}	249	PVSSB30	0Ω	V_{SS}
74	ADDRESS[1]	5.6kΩ	V_{CC}-V_{SS}	250	GPIO[13]	5.6kΩ	V_{CC}-V_{SS}
75	ADDRESS[2]	5.6kΩ	V_{CC}-V_{SS}	251	GPIO[14]	2.2kΩ	S4
76	ADDRESS[3]	5.6kΩ	V_{CC}-V_{SS}	252	EEPROM_RESET_N	5.6kΩ	V_{CC}-V_{SS}
77	ADDRESS[4]	5.6kΩ	V_{CC}-V_{SS}	253	EEPROM_ENABLE	5.6kΩ	V_{CC}-V_{SS}
78	ADDRESS[5]	5.6kΩ	V_{CC}-V_{SS}	254	SYS_PLL_FREQSEL[0]	2.2kΩ	S4
79	PVSSB6	0Ω	V_{SS}	255	SYS_PLL_FREQSEL[1]	2.2kΩ	S4
80	PVDDB6	0Ω	V_{CC}	256	GPIO[15]	5.6kΩ	V_{CC}-V_{SS}
81	VSSA	0Ω	V_{SS}	257	VSSA	0Ω	V_{SS}
82	VDDA	0Ω	V_{DD}	258	VDDA	0Ω	V_{DD}
83	PVSSPLL2	0Ω	V_{SS}	259	EEPROM_POWER	5.6kΩ	V_{CC}-V_{SS}
84	PVDDPLL2	0Ω	V_{DD}	260	SCAN_IN[4]	2.2kΩ	S4
86	ADDRESS[6]	5.6kΩ	V_{CC}-V_{SS}	261	SCAN_IN[5]	2.2kΩ	S4
87	MIL_PLL_LOCK	5.6kΩ	V_{CC}-V_{SS}	262	SCAN_IN[6]	2.2kΩ	S4
88	EXT_MIL_CLK	2.2kΩ	S1	263	SCAN_IN[7]	2.2kΩ	S4
89	SYS_PLL_LOCK	5.6kΩ	V_{CC}-V_{SS}	264	SCAN_IN[8]	2.2kΩ	S4
90	ADDRESS[7]	5.6kΩ	V_{CC}-V_{SS}	265	EXT_CORE_CLK	2.2kΩ	S1
91	PVSSB7	0Ω	V_{SS}	266	GNSS_RESET_N	2.2kΩ	V_{CC}
92	PVDDB7	0Ω	V_{CC}	267	HALF_SAMPLE_CLK	2.2kΩ	S1
93	ADDRESS[8]	5.6kΩ	V_{CC}-V_{SS}	268	INPUT_A0[0]	2.2kΩ	V_{CC}
94	ADDRESS[9]	5.6kΩ	V_{CC}-V_{SS}	269	PVDDB25	0Ω	V_{CC}
95	VSSA	0Ω	V_{SS}	270	PVSSB25	0Ω	V_{SS}
96	VDDA	0Ω	V_{DD}	271	VSSA	0Ω	V_{SS}
97	ADDRESS[10]	5.6kΩ	V_{CC}-V_{SS}	272	VDDA	0Ω	V_{DD}
98	ADDRESS[11]	5.6kΩ	V_{CC}-V_{SS}	273	INPUT_A0[1]	2.2kΩ	S4
99	ADDRESS[12]	5.6kΩ	V_{CC}-V_{SS}	274	INPUT_A0[2]	2.2kΩ	S4
100	PVDDB8	0Ω	V_{CC}	275	INPUT_A1[0]	2.2kΩ	S4
101	PVSSB8	0Ω	V_{SS}	276	INPUT_A1[1]	2.2kΩ	S4
102	ADDRESS[13]	5.6kΩ	V_{CC}-V_{SS}	277	INPUT_A1[2]	2.2kΩ	S4
103	ADDRESS[14]	5.6kΩ	V_{CC}-V_{SS}	278	INPUT_A2[0]	2.2kΩ	S4
104	ADDRESS[15]	5.6kΩ	V_{CC}-V_{SS}	279	INPUT_A2[1]	2.2kΩ	S4
105	ADDRESS[16]	5.6kΩ	V_{CC}-V_{SS}	280	INPUT_A2[2]	2.2kΩ	S4
106	ADDRESS[17]	5.6kΩ	V_{CC}-V_{SS}	281	INPUT_A3[0]	2.2kΩ	S4
107	PVDDB9	0Ω	V_{CC}	282	INPUT_A3[1]	2.2kΩ	S4
108	PVSSB9	0Ω	V_{SS}	283	INPUT_A3[2]	2.2kΩ	S4
109	ADDRESS[18]	5.6kΩ	V_{CC}-V_{SS}	284	INPUT_B0[0]	2.2kΩ	S4
110	ADDRESS[19]	5.6kΩ	V_{CC}-V_{SS}	285	INPUT_B0[1]	2.2kΩ	S4
111	ADDRESS[20]	5.6kΩ	V_{CC}-V_{SS}	286	INPUT_B0[2]	2.2kΩ	S4

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
112	ADDRESS[21]	5.6kΩ	V_{CC}-V_{SS}	287	INPUT_B1[0]	2.2kΩ	S4
113	ADDRESS[22]	5.6kΩ	V_{CC}-V_{SS}	288	INPUT_B1[1]	2.2kΩ	S4
114	PVDDB10	0Ω	V_{CC}	289	INPUT_B1[2]	2.2kΩ	S4
115	PVSSB10	0Ω	V_{SS}	290	INPUT_B2[0]	2.2kΩ	S4
116	ADDRESS[23]	5.6kΩ	V_{CC}-V_{SS}	291	INPUT_B2[1]	2.2kΩ	S4
117	ADDRESS[24]	5.6kΩ	V_{CC}-V_{SS}	292	INPUT_B2[2]	2.2kΩ	S4
118	ADDRESS[25]	5.6kΩ	V_{CC}-V_{SS}	293	INPUT_B3[0]	2.2kΩ	S4
119	ADDRESS[26]	5.6kΩ	V_{CC}-V_{SS}	294	PVDDB26	0Ω	V_{CC}
120	ADDRESS[27]	5.6kΩ	V_{CC}-V_{SS}	295	PVSSB26	0Ω	V_{SS}
121	PVDDB11	0Ω	V_{CC}	296	INPUT_B3[1]	2.2kΩ	S4
122	PVSSB11	0Ω	V_{SS}	297	INPUT_B3[2]	2.2kΩ	S4
123	IOS_N	5.6kΩ	V_{CC}-V_{SS}	298	PIO[0]	2.2kΩ	S4
124	RAMS_N[0]	5.6kΩ	V_{CC}-V_{SS}	299	PIO[1]	2.2kΩ	S4
125	RAMS_N[1]	5.6kΩ	V_{CC}-V_{SS}	300	PIO[2]	2.2kΩ	S4
126	RAMS_N[2]	5.6kΩ	V_{CC}-V_{SS}	301	PIO[3]	2.2kΩ	S4
127	RAMS_N[3]	5.6kΩ	V_{CC}-V_{SS}	302	PIO[4]	2.2kΩ	S4
128	RAMS_N[4]	5.6kΩ	V_{CC}-V_{SS}	303	PIO[5]	2.2kΩ	S4
129	PVDDB12	0Ω	V_{CC}	304	PIO[6]	2.2kΩ	S4
130	PVSSB12	0Ω	V_{SS}	305	PIO[7]	2.2kΩ	S4
131	ROMS_N[0]	5.6kΩ	V_{CC}-V_{SS}	306	PIO[8]	2.2kΩ	S4
132	ROMS_N[1]	5.6kΩ	V_{CC}-V_{SS}	307	PIO[9]	2.2kΩ	S4
133	RAMOE_N[1]	5.6kΩ	V_{CC}-V_{SS}	308	PIO[10]	2.2kΩ	S4
134	OE_N	5.6kΩ	V_{CC}-V_{SS}	309	PIO[11]	2.2kΩ	S4
135	WRITE_N	5.6kΩ	V_{CC}-V_{SS}	310	PIO[12]	2.2kΩ	S4
136	RAMOE_N[0]	5.6kΩ	V_{CC}-V_{SS}	311	PIO[13]	2.2kΩ	S4
138	PVDDB13	0Ω	V_{CC}	312	PIO[14]	2.2kΩ	S4
139	PVSSB13	0Ω	V_{SS}	313	PIO[15]	2.2kΩ	S4
140	DATA[0]	2.2kΩ	S4	314	GPIO[0]	5.6kΩ	V_{CC}-V_{SS}
141	DATA[1]	2.2kΩ	S4	315	GPIO[1]	5.6kΩ	V_{CC}-V_{SS}
142	DATA[2]	2.2kΩ	S4	316	GPIO[2]	5.6kΩ	V_{CC}-V_{SS}
143	DATA[3]	2.2kΩ	S4	317	GPIO[3]	5.6kΩ	V_{CC}-V_{SS}
144	DATA[4]	2.2kΩ	S4	318	PVDDB27	0Ω	V_{CC}
145	PVDDB14	0Ω	V_{CC}	319	PVSSB27	0Ω	V_{SS}
146	PVSSB14	0Ω	V_{SS}	320	GPIO[4]	5.6kΩ	V_{CC}-V_{SS}
147	DATA[5]	2.2kΩ	S4	321	GPIO[5]	5.6kΩ	V_{CC}-V_{SS}
148	DATA[6]	2.2kΩ	S4	322	GPIO[6]	2.2kΩ	S4
149	DATA[7]	2.2kΩ	S4	323	SCAN_IN[9]	2.2kΩ	S4
150	DATA[8]	2.2kΩ	S4	324	ASC[0]	5.6kΩ	V_{CC}-V_{SS}
151	DATA[9]	2.2kΩ	S4	325	ASC[1]	5.6kΩ	V_{CC}-V_{SS}
152	PVDDB15	0Ω	V_{CC}	326	ASEO	5.6kΩ	V_{CC}-V_{SS}

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
153	PVSSB15	0Ω	V_{SS}	327	ASEI	2.2kΩ	S4
154	DATA[10]	2.2kΩ	S4	328	MEO	5.6kΩ	V_{CC}-V_{SS}
155	DATA[11]	2.2kΩ	S4	329	MEI	2.2kΩ	S4
156	DATA[12]	2.2kΩ	S4	330	SCAN_IN[10]	2.2kΩ	S4
157	DATA[13]	2.2kΩ	S4	331	SCAN_IN[11]	2.2kΩ	S4
158	DATA[14]	2.2kΩ	S4	332	PPSO	5.6kΩ	V_{CC}-V_{SS}
159	PVDDB16	0Ω	V_{CC}	333	PPSI	2.2kΩ	S4
160	PVSSB16	0Ω	V_{SS}	334	EXT_CLK	2.2kΩ	S1
161	DATA[15]	2.2kΩ	S4	335	AU_TRIGGER	2.2kΩ	S4
162	DATA[16]	2.2kΩ	S4	336	SYS_CLK_OUT	5.6kΩ	V_{CC}-V_{SS}
163	DATA[17]	2.2kΩ	S4	337	PVDDB28	0Ω	V_{CC}
164	DATA[18]	2.2kΩ	S4	338	PVSSB28	0Ω	V_{SS}
165	DATA[19]	2.2kΩ	S4	339	DA_OUT[0]	5.6kΩ	V_{CC}-V_{SS}
166	PVDDB17	0Ω	V_{CC}	340	DA_OUT[1]	5.6kΩ	V_{CC}-V_{SS}
167	PVSSB17	0Ω	V_{SS}	341	DA_OUT[2]	5.6kΩ	V_{CC}-V_{SS}
168	DATA[20]	2.2kΩ	S4	342	DA_OUT[3]	5.6kΩ	V_{CC}-V_{SS}
169	VSSA	0Ω	V_{SS}	343	IMT_12	5.6kΩ	V_{CC}-V_{SS}
170	VDDA	0Ω	V_{DD}	344	SYS_CLK_DIV[0]	2.2kΩ	S4
171	DATA[21]	2.2kΩ	S4	345	VSSA	0Ω	V_{SS}
172	DATA[22]	2.2kΩ	S4	346	VDDA	0Ω	V_{DD}
173	DATA[23]	2.2kΩ	S4	347	SYS_CLK_DIV[1]	2.2kΩ	S4
174	DATA[24]	2.2kΩ	S4	348	SYS_CLK_DIV[2]	2.2kΩ	S4
175	PVSSB18	0Ω	V_{SS}	349	SYS_CLK_DIV[3]	2.2kΩ	S4
176	PVDDB18	0Ω	V_{CC}	350	PVDDB29	0Ω	V_{CC}
177	DATA[25]	2.2kΩ	S4	351	PVSSB29	0Ω	V_{SS}
178	DATA[26]	2.2kΩ	S4	352	MIL_CLK_OUT	5.6kΩ	V_{CC}-V_{SS}

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.6, Power Burn-in Conditions.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22±3	°C
Core Supply Voltage	V_{DD}	1.8	V
I/O Supply Voltage	V_{CC}	3.3	V

NOTES:

1. Pin connections shall be as follows, where NC = not connected:

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
2	SYS_PLL_BYPASS	2.2kΩ	V_{SS}	179	DATA[27]	0Ω	NC
3	TEST_EN	2.2kΩ	V_{CC}	180	DATA[28]	0Ω	NC
4	SCAN_EN	2.2kΩ	V_{SS}	181	DATA[29]	0Ω	NC
5	TRST_N	2.2kΩ	V_{SS}	182	SCAN_IN[0]	2.2kΩ	V_{SS}
6	TCK	2.2kΩ	V_{SS}	183	VSSA	0Ω	V_{SS}
7	VSSA	0Ω	V_{SS}	184	VDDA	0Ω	V_{DD}
8	VDDA	0Ω	V_{DD}	185	PVDDB19	0Ω	V_{CC}
9	TDO	0Ω	NC	186	PVSSB19	0Ω	V_{SS}
10	TMS	2.2kΩ	V_{SS}	187	DATA[30]	0Ω	NC
11	TDI	2.2kΩ	V_{SS}	188	DATA[31]	0Ω	NC
12	UART0_RX	2.2kΩ	V_{SS}	189	CB[0]	0Ω	NC
13	UART0_TX	0Ω	NC	190	CB[1]	0Ω	NC
14	UART1_RX	2.2kΩ	V_{SS}	191	PVSSB20	0Ω	V_{SS}
15	UART1_TX	0Ω	NC	192	CB[2]	0Ω	NC
16	SPI_IN_CLK	2.2kΩ	V_{SS}	193	PVDDB20	0Ω	V_{CC}
17	SPI_OUT_CLK	0Ω	NC	194	CB[3]	0Ω	NC
18	MOSI	0Ω	NC	195	CB[4]	0Ω	NC
19	MISO	2.2kΩ	V_{SS}	196	CB[5]	0Ω	NC
20	SPI_SEL_N[0]	0Ω	NC	197	PVDDB21	0Ω	V_{CC}
21	SPI_SEL_N[1]	0Ω	NC	198	PVSSB21	0Ω	V_{SS}
22	SPI_SEL_N[2]	0Ω	NC	199	CB[6]	0Ω	NC
23	SPI_SEL_N[3]	0Ω	NC	200	BEXC_N	2.2kΩ	V_{SS}
24	PVDDB1	0Ω	V_{CC}	201	BRDY_N	2.2kΩ	V_{SS}
25	PVSSB1	0Ω	V_{SS}	202	SGPO	0Ω	NC
26	SPW_RX_D[0]	2.2kΩ	V_{SS}	203	RWE_N[0]	0Ω	NC
27	SPW_RX_S[0]	2.2kΩ	V_{SS}	204	RWE_N[1]	0Ω	NC
28	GPIO[7]	0Ω	NC	205	RWE_N[2]	0Ω	NC

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
29	SPW_TX_D[0]	0Ω	NC	206	RWE_N[3]	0Ω	NC
30	SPW_TX_S[0]	0Ω	NC	207	READ	0Ω	NC
31	GPIO[8]	0Ω	NC	208	PVSSB22	0Ω	V_{SS}
32	SPW_RX_D[1]	2.2kΩ	V_{SS}	209	PVDDB22	0Ω	V_{CC}
33	SPW_RX_S[1]	2.2kΩ	V_{SS}	210	MIL_RX0	2.2kΩ	V_{SS}
34	PVDDB2	0Ω	V_{CC}	211	MIL_RX0B	2.2kΩ	V_{SS}
35	PVSSB2	0Ω	V_{SS}	212	MIL_TX0	0Ω	NC
36	SPW_TX_D[1]	0Ω	NC	213	MIL_TX0B	0Ω	NC
37	SPW_TX_S[1]	0Ω	NC	214	DSU_ACT	0Ω	NC
38	GPIO[9]	0Ω	NC	215	DSU_BRE	2.2kΩ	V_{SS}
39	SPW_RX_D[2]	2.2kΩ	V_{SS}	216	DSU_EN	2.2kΩ	V_{SS}
40	SPW_RX_S[2]	2.2kΩ	V_{SS}	217	MIL_TX0INH	0Ω	NC
41	GPIO[10]	0Ω	NC	218	MIL_RX1	2.2kΩ	V_{SS}
42	SPW_TX_D[2]	0Ω	NC	219	MIL_RX1B	2.2kΩ	V_{SS}
43	SPW_TX_S[2]	0Ω	NC	220	MIL_TX1	0Ω	NC
44	PVDDB3	0Ω	V_{CC}	221	MIL_TX1B	0Ω	NC
45	PVSSB3	0Ω	V_{SS}	222	PVSSB23	0Ω	V_{SS}
46	GPIO[11]	0Ω	NC	223	PVDDB23	0Ω	V_{CC}
47	SPW_RX_D[3]	2.2kΩ	V_{SS}	224	MIL_TX1INH	0Ω	NC
48	SPW_RX_S[3]	2.2kΩ	V_{SS}	225	SCAN_IN[1]	2.2kΩ	V_{SS}
49	GPIO[12]	0Ω	NC	226	MIL_RESET_OUT_N	0Ω	NC
50	SPW_TX_D[3]	0Ω	NC	227	SIGNAL_OUT_I[0]	0Ω	NC
51	SPW_TX_S[3]	0Ω	NC	228	SIGNAL_OUT_I[1]	0Ω	NC
52	DSU_UART_RX	2.2kΩ	V_{SS}	229	SIGNAL_OUT_I[2]	0Ω	NC
53	DSU_UART_TX	0Ω	NC	230	SIGNAL_OUT_Q[0]	0Ω	NC
54	AGGA4_RESET_N	2.2kΩ	V_{CC}	231	SIGNAL_OUT_Q[1]	0Ω	NC
55	PWR_ON_RESET_N	2.2kΩ	V_{CC}	232	SIGNAL_OUT_Q[2]	0Ω	NC
56	DSU_SPW_EN	2.2kΩ	V_{SS}	233	PVDDB24	0Ω	V_{CC}
57	ERROR_N	0Ω	NC	234	PVSSB24	0Ω	V_{SS}
58	NMI_INT	2.2kΩ	V_{SS}	235	INT_EPOCH1	0Ω	NC
59	PVDDB4	0Ω	V_{CC}	236	CODE_OUT2[0]	0Ω	NC
60	PVSSB4	0Ω	V_{SS}	237	CODE_OUT2[1]	0Ω	NC
61	WDOG_N	0Ω	NC	238	INT_EPOCH2	0Ω	NC
62	WDOG_RST_N	0Ω	NC	239	SPI_SEL_N[4]	0Ω	NC
63	DSU_SPW_TX_D	0Ω	NC	240	SCAN_IN[2]	2.2kΩ	V_{SS}
64	DSU_SPW_TX_S	0Ω	NC	241	SCAN_IN[3]	2.2kΩ	V_{SS}
65	EXT_SYS_CLK	2.2kΩ	V_{SS}	242	CODE_OUT1[0]	0Ω	NC
66	DSU_SPW_RX_D	2.2kΩ	V_{SS}	243	CODE_OUT1[1]	0Ω	NC
67	DSU_SPW_RX_S	2.2kΩ	V_{SS}	244	SYS_PLL_ICP[0]	2.2kΩ	V_{SS}
69	PVSSPLL1	0Ω	V_{SS}	245	SYS_PLL_ICP[1]	2.2kΩ	V_{SS}

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
70	PVDDPLL1	0Ω	V_{DD}	246	MIL_PLL_ICP[0]	2.2kΩ	V_{SS}
71	PVDDB5	0Ω	V_{CC}	247	MIL_PLL_ICP[1]	2.2kΩ	V_{SS}
72	PVSSB5	0Ω	V_{SS}	248	PVDDB30	0Ω	V_{CC}
73	ADDRESS[0]	0Ω	NC	249	PVSSB30	0Ω	V_{SS}
74	ADDRESS[1]	0Ω	NC	250	GPIO[13]	0Ω	NC
75	ADDRESS[2]	0Ω	NC	251	GPIO[14]	0Ω	NC
76	ADDRESS[3]	0Ω	NC	252	EEPROM_RESET_N	0Ω	NC
77	ADDRESS[4]	0Ω	NC	253	EEPROM_ENABLE	0Ω	NC
78	ADDRESS[5]	0Ω	NC	254	SYS_PLL_FREQSEL[0]	2.2kΩ	V_{SS}
79	PVSSB6	0Ω	V_{SS}	255	SYS_PLL_FREQSEL[1]	2.2kΩ	V_{SS}
80	PVDDB6	0Ω	V_{CC}	256	GPIO[15]	0Ω	NC
81	VSSA	0Ω	V_{SS}	257	VSSA	0Ω	V_{SS}
82	VDDA	0Ω	V_{DD}	258	VDDA	0Ω	V_{DD}
83	PVSSPLL2	0Ω	V_{SS}	259	EEPROM_POWER	0Ω	NC
84	PVDDPLL2	0Ω	V_{DD}	260	SCAN_IN[4]	2.2kΩ	V_{SS}
86	ADDRESS[6]	0Ω	NC	261	SCAN_IN[5]	2.2kΩ	V_{SS}
87	MIL_PLL_LOCK	0Ω	NC	262	SCAN_IN[6]	2.2kΩ	V_{SS}
88	EXT_MIL_CLK	2.2kΩ	V_{SS}	263	SCAN_IN[7]	2.2kΩ	V_{SS}
89	SYS_PLL_LOCK	0Ω	NC	264	SCAN_IN[8]	2.2kΩ	V_{SS}
90	ADDRESS[7]	0Ω	NC	265	EXT_CORE_CLK	2.2kΩ	V_{SS}
91	PVSSB7	0Ω	V_{SS}	266	GNSS_RESET_N	2.2kΩ	V_{CC}
92	PVDDB7	0Ω	V_{CC}	267	HALF_SAMPLE_CLK	2.2kΩ	V_{SS}
93	ADDRESS[8]	0Ω	NC	268	INPUT_A0[0]	2.2kΩ	V_{SS}
94	ADDRESS[9]	0Ω	NC	269	PVDDB25	0Ω	V_{CC}
95	VSSA	0Ω	V_{SS}	270	PVSSB25	0Ω	V_{SS}
96	VDDA	0Ω	V_{DD}	271	VSSA	0Ω	V_{SS}
97	ADDRESS[10]	0Ω	NC	272	VDDA	0Ω	V_{DD}
98	ADDRESS[11]	0Ω	NC	273	INPUT_A0[1]	2.2kΩ	V_{SS}
99	ADDRESS[12]	0Ω	NC	274	INPUT_A0[2]	2.2kΩ	V_{SS}
100	PVDDB8	0Ω	V_{CC}	275	INPUT_A1[0]	2.2kΩ	V_{SS}
101	PVSSB8	0Ω	V_{SS}	276	INPUT_A1[1]	2.2kΩ	V_{SS}
102	ADDRESS[13]	0Ω	NC	277	INPUT_A1[2]	2.2kΩ	V_{SS}
103	ADDRESS[14]	0Ω	NC	278	INPUT_A2[0]	2.2kΩ	V_{SS}
104	ADDRESS[15]	0Ω	NC	279	INPUT_A2[1]	2.2kΩ	V_{SS}
105	ADDRESS[16]	0Ω	NC	280	INPUT_A2[2]	2.2kΩ	V_{SS}
106	ADDRESS[17]	0Ω	NC	281	INPUT_A3[0]	2.2kΩ	V_{SS}
107	PVDDB9	0Ω	V_{CC}	282	INPUT_A3[1]	2.2kΩ	V_{SS}
108	PVSSB9	0Ω	V_{SS}	283	INPUT_A3[2]	2.2kΩ	V_{SS}
109	ADDRESS[18]	0Ω	NC	284	INPUT_B0[0]	2.2kΩ	V_{SS}
110	ADDRESS[19]	0Ω	NC	285	INPUT_B0[1]	2.2kΩ	V_{SS}

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
111	ADDRESS[20]	0Ω	NC	286	INPUT_B0[2]	2.2kΩ	V_{SS}
112	ADDRESS[21]	0Ω	NC	287	INPUT_B1[0]	2.2kΩ	V_{SS}
113	ADDRESS[22]	0Ω	NC	288	INPUT_B1[1]	2.2kΩ	V_{SS}
114	PVDDB10	0Ω	V_{CC}	289	INPUT_B1[2]	2.2kΩ	V_{SS}
115	PVSSB10	0Ω	V_{SS}	290	INPUT_B2[0]	2.2kΩ	V_{SS}
116	ADDRESS[23]	0Ω	NC	291	INPUT_B2[1]	2.2kΩ	V_{SS}
117	ADDRESS[24]	0Ω	NC	292	INPUT_B2[2]	2.2kΩ	V_{SS}
118	ADDRESS[25]	0Ω	NC	293	INPUT_B3[0]	2.2kΩ	V_{SS}
119	ADDRESS[26]	0Ω	NC	294	PVDDB26	0Ω	V_{CC}
120	ADDRESS[27]	0Ω	NC	295	PVSSB26	0Ω	V_{SS}
121	PVDDB11	0Ω	V_{CC}	296	INPUT_B3[1]	2.2kΩ	V_{SS}
122	PVSSB11	0Ω	V_{SS}	297	INPUT_B3[2]	2.2kΩ	V_{SS}
123	IOS_N	0Ω	NC	298	PIO[0]	0Ω	NC
124	RAMS_N[0]	0Ω	NC	299	PIO[1]	0Ω	NC
125	RAMS_N[1]	0Ω	NC	300	PIO[2]	0Ω	NC
126	RAMS_N[2]	0Ω	NC	301	PIO[3]	0Ω	NC
127	RAMS_N[3]	0Ω	NC	302	PIO[4]	0Ω	NC
128	RAMS_N[4]	0Ω	NC	303	PIO[5]	0Ω	NC
129	PVDDB12	0Ω	V_{CC}	304	PIO[6]	0Ω	NC
130	PVSSB12	0Ω	V_{SS}	305	PIO[7]	0Ω	NC
131	ROMS_N[0]	0Ω	NC	306	PIO[8]	0Ω	NC
132	ROMS_N[1]	0Ω	NC	307	PIO[9]	0Ω	NC
133	RAMOE_N[1]	0Ω	NC	308	PIO[10]	0Ω	NC
134	OE_N	0Ω	NC	309	PIO[11]	0Ω	NC
135	WRITE_N	0Ω	NC	310	PIO[12]	0Ω	NC
136	RAMOE_N[0]	0Ω	NC	311	PIO[13]	0Ω	NC
138	PVDDB13	0Ω	V_{CC}	312	PIO[14]	0Ω	NC
139	PVSSB13	0Ω	V_{SS}	313	PIO[15]	0Ω	NC
140	DATA[0]	0Ω	NC	314	GPIO[0]	0Ω	NC
141	DATA[1]	0Ω	NC	315	GPIO[1]	0Ω	NC
142	DATA[2]	0Ω	NC	316	GPIO[2]	0Ω	NC
143	DATA[3]	0Ω	NC	317	GPIO[3]	0Ω	NC
144	DATA[4]	0Ω	NC	318	PVDDB27	0Ω	V_{CC}
145	PVDDB14	0Ω	V_{CC}	319	PVSSB27	0Ω	V_{SS}
146	PVSSB14	0Ω	V_{SS}	320	GPIO[4]	0Ω	NC
147	DATA[5]	0Ω	NC	321	GPIO[5]	0Ω	NC
148	DATA[6]	0Ω	NC	322	GPIO[6]	0Ω	NC
149	DATA[7]	0Ω	NC	323	SCAN_IN[9]	2.2kΩ	V_{SS}
150	DATA[8]	0Ω	NC	324	ASC[0]	0Ω	NC
151	DATA[9]	0Ω	NC	325	ASC[1]	0Ω	NC

Pin	Signal	Serial Resist-ance	Wired To	Pin	Signal	Serial Resist-ance	Wired To
152	PVDDB15	0Ω	V_{CC}	326	ASEO	0Ω	NC
153	PVSSB15	0Ω	V_{SS}	327	ASEI	2.2kΩ	V_{SS}
154	DATA[10]	0Ω	NC	328	MEO	0Ω	NC
155	DATA[11]	0Ω	NC	329	MEI	2.2kΩ	V_{SS}
156	DATA[12]	0Ω	NC	330	SCAN_IN[10]	2.2kΩ	V_{SS}
157	DATA[13]	0Ω	NC	331	SCAN_IN[11]	2.2kΩ	V_{SS}
158	DATA[14]	0Ω	NC	332	PPSO	0Ω	NC
159	PVDDB16	0Ω	V_{CC}	333	PPSI	2.2kΩ	V_{SS}
160	PVSSB16	0Ω	V_{SS}	334	EXT_CLK	2.2kΩ	V_{SS}
161	DATA[15]	0Ω	NC	335	AU_TRIGGER	2.2kΩ	V_{SS}
162	DATA[16]	0Ω	NC	336	SYS_CLK_OUT	0Ω	NC
163	DATA[17]	0Ω	NC	337	PVDDB28	0Ω	V_{CC}
164	DATA[18]	0Ω	NC	338	PVSSB28	0Ω	V_{SS}
165	DATA[19]	0Ω	NC	339	DA_OUT[0]	0Ω	NC
166	PVDDB17	0Ω	V_{CC}	340	DA_OUT[1]	0Ω	NC
167	PVSSB17	0Ω	V_{SS}	341	DA_OUT[2]	0Ω	NC
168	DATA[20]	0Ω	NC	342	DA_OUT[3]	0Ω	NC
169	VSSA	0Ω	V_{SS}	343	IMT_12	0Ω	NC
170	VDDA	0Ω	V_{DD}	344	SYS_CLK_DIV[0]	2.2kΩ	V_{SS}
171	DATA[21]	0Ω	NC	345	VSSA	0Ω	V_{SS}
172	DATA[22]	0Ω	NC	346	VDDA	0Ω	V_{DD}
173	DATA[23]	0Ω	NC	347	SYS_CLK_DIV[1]	2.2kΩ	V_{SS}
174	DATA[24]	0Ω	NC	348	SYS_CLK_DIV[2]	2.2kΩ	V_{SS}
175	PVSSB18	0Ω	V_{SS}	349	SYS_CLK_DIV[3]	2.2kΩ	V_{SS}
176	PVDDB18	0Ω	V_{CC}	350	PVDDB29	0Ω	V_{CC}
177	DATA[25]	0Ω	NC	351	PVSSB29	0Ω	V_{SS}
178	DATA[26]	0Ω	NC	352	MIL_CLK_OUT	0Ω	NC

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall have successfully met the Room Temperature Electrical Measurements specified in Para. 2.3.1.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22±3°C.

The characteristics, test methods, conditions and limits shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.