RESIN-ENCAPSULATED MICROELECTRONIC MODULE, SILICON, CMOS, 256K X 32-BIT, NON-VOLATILE MAGNETO-RESISTIVE RANDOM ACCESS MEMORY (MRAM)

BASED ON TYPE 3DMR8M32VS8420 SS

ESCC Detail Specification No. 6001/001

Issue 1	December 2021

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE
(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 6001.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification Nos. 21300 and 2566001 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 600100101P

- Detail Specification Reference: 6001001
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: P

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Weight max g	Total Dose Radiation Level Letter
01	3DMR8M32VS8420 SS	V8a (68 Pin SOP)	8.5	P [30krad(Si)]

The total dose radiation level letter shall be as defined in ESCC Basic Specification No 22900.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to +4	V	Note 1
Input / Output Voltage	V_{IN}, V_{OUT}	-0.5 to V_{DD} +0.5	V	Note 1
Input / Output Current (per pin)	I_{IN}, I_{OUT}	±20	mA	
Power Dissipation	P_{Dmax}	2.4	W	
Maximum Magnetic Field during Write: during Read or Standby:	 H_{MAX-W} H_{MAX-R}	 2000 8000	A/m	
Operating Temperature Range	T_{op}	-55 to +105	°C	T_{case}. Notes 2, 3
Storage Temperature Range	T_{stg}	-55 to +150	°C	
Case Temperature (short term exposure)	$T_{case-max}$	+215	°C	For < 60s. T_{case}. Note 2
Junction Temperature	T_j	+150	°C	Note 4
Thermal Resistance, junction to case	$R_{th(j-c)}$	21	°C/W	Notes 2, 4
Thermal Resistance, junction to ambient	$R_{th(j-a)}$	44	°C/W	Notes 4, 5
Soldering Temperature	T_{sol}	+310	°C	Manual soldering. Note 6
		+235		Reflow soldering (e.g. vapour phase)

NOTES:

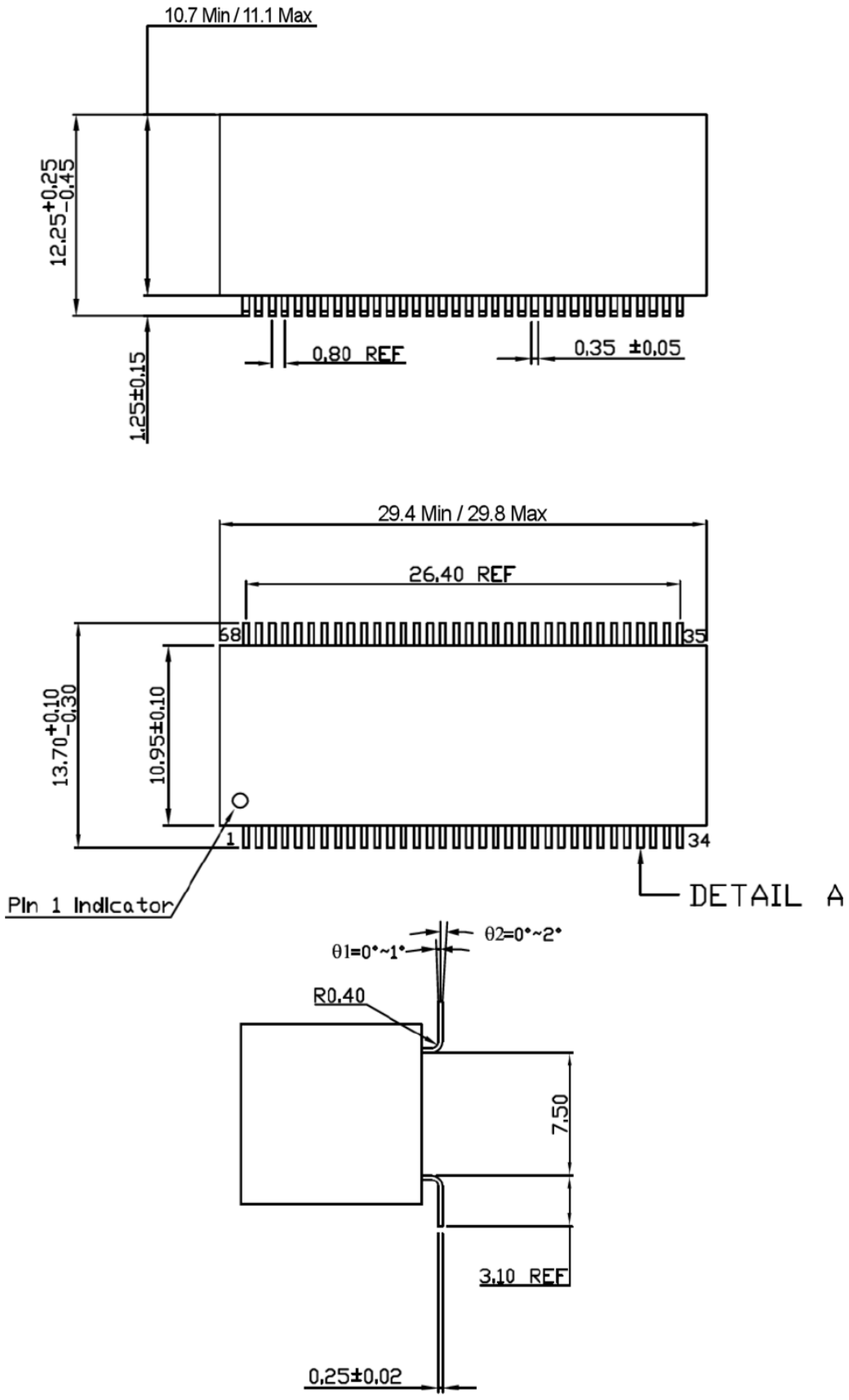
1. All voltages are with respect to V_{SS}.
   Components are functional with the following conditions:
   - Supply Voltage: $3V \leq V_{DD} \leq 3.6V$.
   - For Write Enable input, $\overline{WE}$: $-0.5V \leq V_{IL} \leq 0.8V$; $2.5V \leq V_{IH} \leq 3V$
   - For all other inputs: $-0.5V \leq V_{IL} \leq 0.8V$; $2.2V \leq V_{IH} \leq V_{DD} +0.3V$.
   - For all other inputs with a pulse width ≤ 10ns: $-2V \leq V_{IL} \leq 0.8V$; $2.2V \leq V_{IH} \leq V_{DD} +2V$
2. Case Temperature is defined as the temperature at the module's lateral sides.
3. Maximum operating temperature may be exceeded, up to T_{op-max} = +125°C, only during testing in accordance with this specification.
4. Junction Temperature is defined as the temperature of the top die in the stack.
5. Ambient temperature is defined as the temperature at the leads mounted on a PCB.
6. Duration 4 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

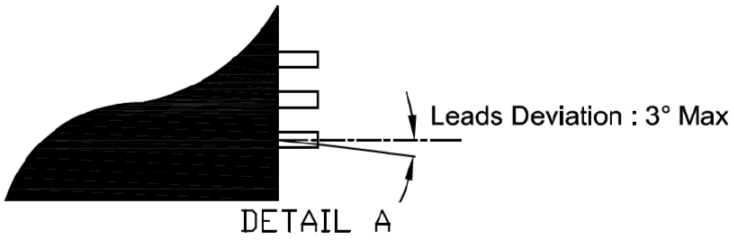
1.6 HANDLING PRECAUTIONS

These components are susceptible to damage by electrostatic discharge and magnetic fields (see Para. 1.5). Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000V.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

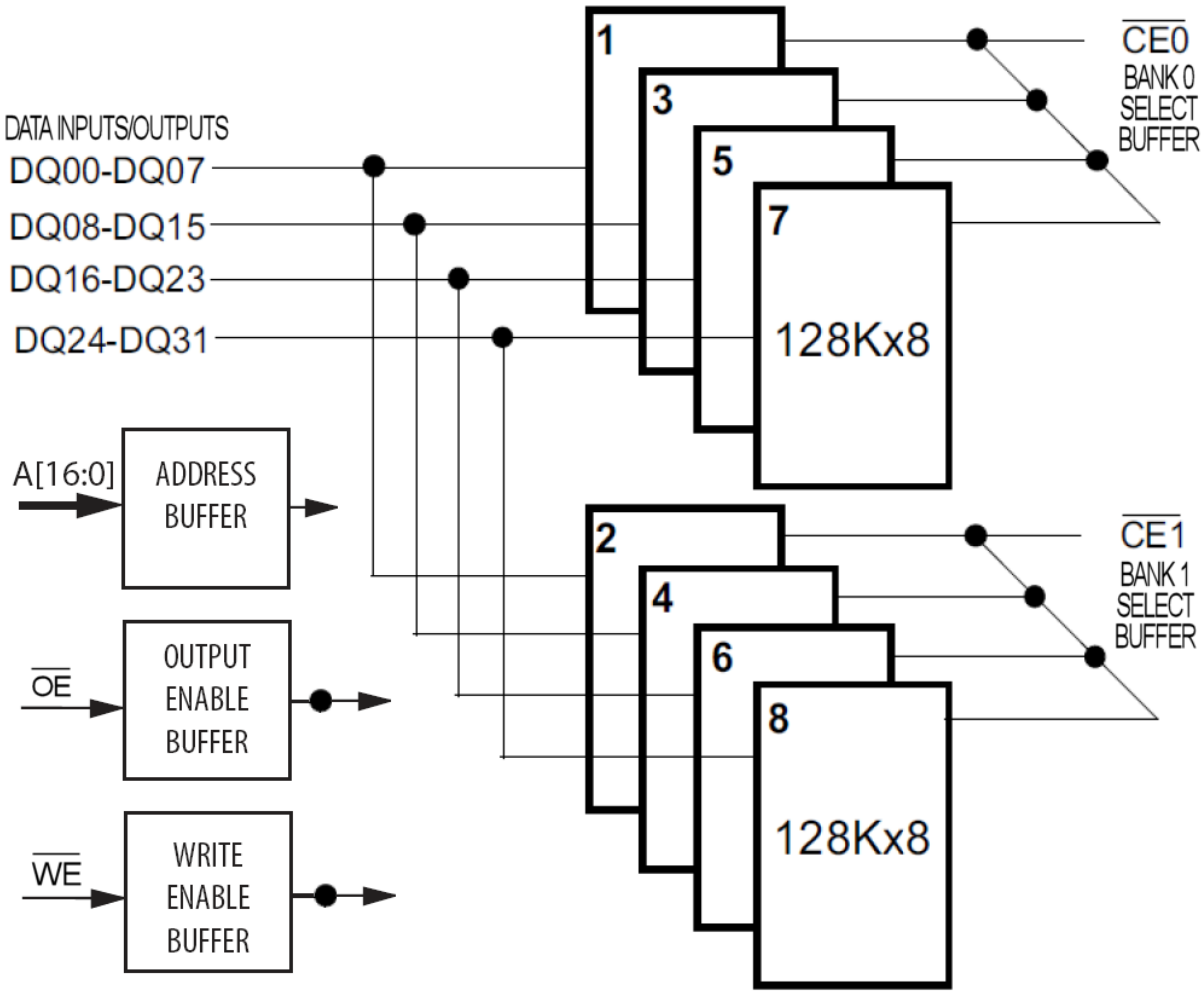




NOTES:

1. All dimensions in mm.
2. Terminal Identification: a pin 1 identification mark shall be located adjacent to pin 1 as shown. All other pins are identified by their position relative to pin 1, as shown.

1.8 FUNCTIONAL DIAGRAM



NOTES:

1. Inputs A0 to A16, $\overline{OE}$, $\overline{WE}$ are common to all 8 individual MRAM add-on components in the stack.
2. The case is connected to V_{SS}.

1.9 PIN ASSIGNMENT

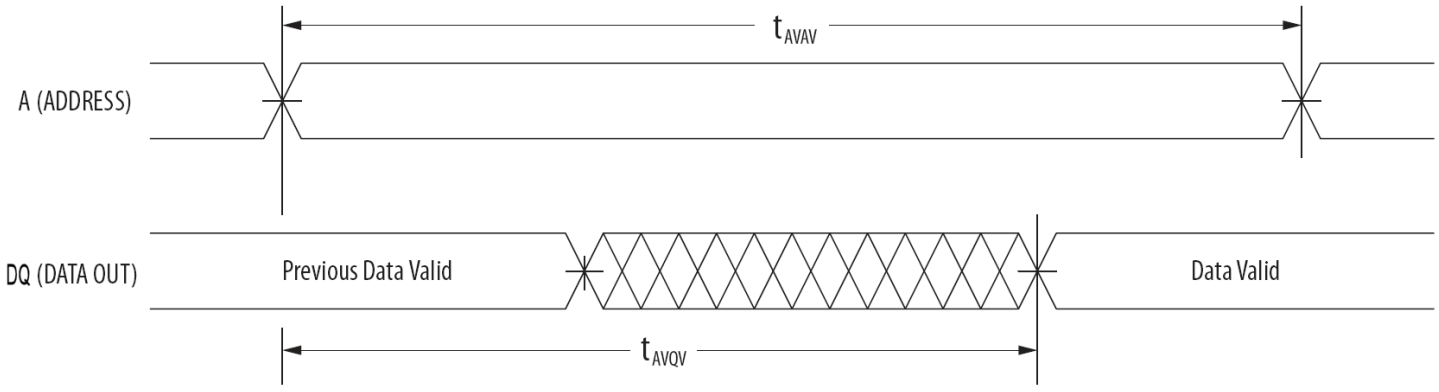
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	DQ09 (Bidirectional Data Input/Output)	18	V_{SS} (Ground)	35	DQ12 (Bidirectional Data Input/Output)	52	V_{SS} (Ground)
2	DQ08 (Bidirectional Data Input/Output)	19	DQ02 (Bidirectional Data Input/Output)	36	DQ13 (Bidirectional Data Input/Output)	53	DQ06 (Bidirectional Data Input/Output)
3	DQ17 (Bidirectional Data Input/Output)	20	DQ03 (Bidirectional Data Input/Output)	37	DQ20 (Bidirectional Data Input/Output)	54	DQ07 (Bidirectional Data Input/Output)
4	DQ16 (Bidirectional Data Input/Output)	21	$\overline{WE}$ (Write Enable Input)	38	DQ21 (Bidirectional Data Input/Output)	55	$\overline{OE}$ (Output Enable Input)
5	$\overline{CE1}$ (Chip Enable / Bank 1 Select)	22	A5 (Address Bus Input)	39	DQ29 (Bidirectional Data Input/Output)	56	A15 (Address Bus Input)
6	No Connection	23	A6 (Address Bus Input)	40	DQ28 (Bidirectional Data Input/Output)	57	A16 (Address Bus Input)
7	No Connection	24	A7 (Address Bus Input)	41	No Connection	58	DQ25 (Bidirectional Data Input/Output)
8	No Connection	25	A8 (Address Bus Input)	42	No Connection	59	DQ24 (Bidirectional Data Input/Output)
9	A0 (Address Bus Input)	26	A9 (Address Bus Input)	43	A10 (Address Bus Input)	60	No Connection
10	A1 (Address Bus Input)	27	No Connection	44	A11 (Address Bus Input)	61	No Connection
11	A2 (Address Bus Input)	28	No Connection	45	A12 (Address Bus Input)	62	No Connection
12	A3 (Address Bus Input)	29	DQ27 (Bidirectional Data Input/Output)	46	A13 (Address Bus Input)	63	DQ31 (Bidirectional Data Input/Output)
13	A4 (Address Bus Input)	30	DQ26 (Bidirectional Data Input/Output)	47	A14 (Address Bus Input)	64	DQ30 (Bidirectional Data Input/Output)
14	$\overline{CE0}$ (Chip Enable / Bank 0 Select)	31	DQ19 (Bidirectional Data Input/Output)	48	No Connection	65	DQ22 (Bidirectional Data Input/Output)
15	DQ00 (Bidirectional Data Input/Output)	32	DQ18 (Bidirectional Data Input/Output)	49	DQ04 (Bidirectional Data Input/Output)	66	DQ23 (Bidirectional Data Input/Output)
16	DQ01 (Bidirectional Data Input/Output)	33	DQ11 (Bidirectional Data Input/Output)	50	DQ05 (Bidirectional Data Input/Output)	67	DQ14 (Bidirectional Data Input/Output)
17	V_{DD} (Positive Supply)	34	DQ10 (Bidirectional Data Input/Output)	51	V_{DD} (Positive Supply)	68	DQ15 (Bidirectional Data Input/Output)

1.10 TRUTH TABLE AND TIMING DIAGRAMS

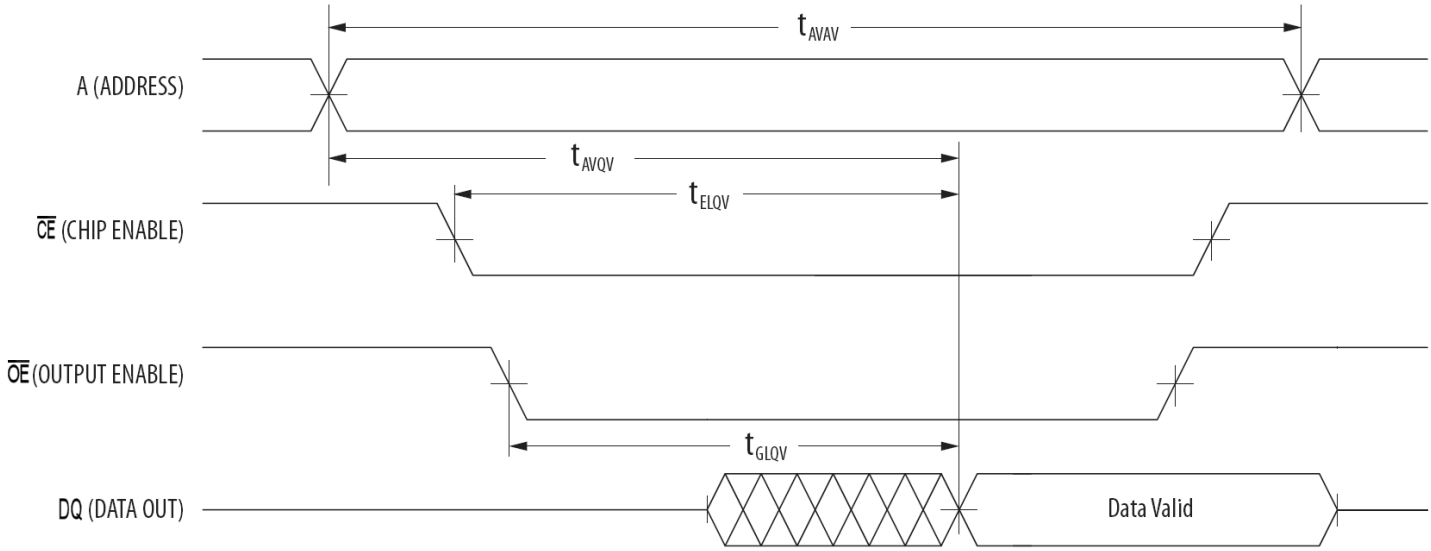
Inputs (Note 1)				Bank Selected	DQ[31:0] Data Inputs/Outputs	Mode	Total Maximum V_{DD} Current (Note 2)
$\overline{CE0}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$				
H	H	X	X	None	Z	Deselected	I_{SB1} I_{SB2}
L	H	H	H	0	Z	All Outputs disabled	I_{DDR} + 0.5x I_{SB1} I_{DDR} + 0.5x I_{SB2}
H	L	H	H	1	Z	All Outputs disabled	I_{DDR} + 0.5x I_{SB1} I_{DDR} + 0.5x I_{SB2}
L	L	H	H	0 & 1	Z	All Outputs disabled	2 x I_{DDR}
L	H	L	H	0	Data out	Read Bank 0 only	I_{DDR} + 0.5x I_{SB1} I_{DDR} + 0.5x I_{SB2}
H	L	L	H	1	Data out	Read Bank 1 only	I_{DDR} + 0.5x I_{SB1} I_{DDR} + 0.5x I_{SB2}
L	H	X	L	0	Data in	Write Bank 0 only	I_{DDW} + 0.5x I_{SB1} I_{DDW} + 0.5x I_{SB2}
H	L	X	L	1	Data in	Write Bank 1 only	I_{DDW} + 0.5x I_{SB1} I_{DDW} + 0.5x I_{SB2}
L	L	L	H	-	-	Note 3	-
L	L	X	L	-	-	Note 4	-

NOTES:

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant, Z = High Impedance.
2. The total maximum supply current for both banks. See Para. 2.3.1 for limits.
3. This configuration is not permitted (due to bus contention).
4. This configuration is not specified or tested, and has no guaranteed performance.
5. The timing diagrams for the Read cycle are as follows:



Note: Device is continuously selected (Chip Enable & Output Enable = L)



1.11 ADD-ON COMPONENTS

Add-on components used in the production of the memory modules specified herein shall meet the requirements of this specification, the ESCC Generic Specification and the Manufacturer's PID. Element evaluation performed on add-on components, including screening and lot acceptance testing prior to assembly of the memory modules specified herein, shall be as specified in the ESCC Generic Specification and the ESCC Executive approved Manufacturer's PID.

The memory module specified herein is produced as a stack of 8 individually-packaged, 128k x 8 non-volatile, MRAM add-on components, each with a 44 lead, plastic, small-outline, TSOP2 package.

The specific active memory add-on component used shall be as specified in the ESCC Executive approved Manufacturer's PID.

1.12 MATERIAL AND FINISHES

(a) Case
Polymeric resin with gold metallization, thickness 1.5 to 3µm, over nickel, with thickness 3.5 to 5.5µm.

(b) Terminals
The terminal material shall be Kovar. The terminal finish shall be gold, with thickness 1 to 2µm, over nickel, with thickness 3 to 5µm.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Production Control – Chart F2

(a) Paras. 4.6.3, 4.7, 5.2.1.1, 8.1, Total Dose Radiation Testing of Active Memory Add-on Components
During procurement of memory modules, Total Dose Radiation Testing of the applicable lot of active memory add-on components in accordance with the Generic Specification and Para. 2.9 herein, is mandatory. Any failures shall result in the lot of add-on components being rejected.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the memory module shall be:

(a) Terminal identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

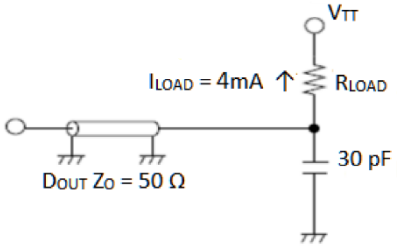
The measurements shall be performed at T_{amb} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table Note 2	-	-	-
Active Supply Current – Read Mode (single bank only)	I_{DDR}	3005	V_{DD} = 3.6V; V_{SS} = 0V I_{OUT} = 0mA Note 3	-	128	mA
Active Supply Current – Write Mode (single bank only)	I_{DDW}	3005	V_{DD} = 3.6V; V_{SS} = 0V Note 3	-	228	mA
Stand-by Supply Current 1 (both banks deselected)	I_{SB1}	3005	V_{DD} = 3.6V; V_{SS} = 0V $\overline{CE0}$, $\overline{CE1}$ = V_{IH} Note 4	-	56	mA
Stand-by Supply Current 2 (both banks deselected)	I_{SB2}	3005	V_{DD} = 3.6V; V_{SS} = 0V f = 0MHz $\overline{CE0}$, $\overline{CE1}$ = V_{DD} -0.2V $V_{IL} \leq V_{SS}$ +0.2V $V_{IH} \geq V_{DD}$ -0.2V	-	48	mA
Low Level Input Current	I_{IL}	3009	V_{DD} = 3.6V; V_{SS} = 0V V_{IL} = V_{SS}	-8	+8	µA
High Level Input Current	I_{IH}	3010	V_{DD} = 3.6V; V_{SS} = 0V V_{IH} = V_{DD}	-8	+8	µA
Output Leakage Current	I_{OZL}	3020	V_{DD} = 3.6V; V_{SS} = 0V	-8	+8	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Third State, Low Level Applied			V_{OUT} = V_{SS}			
Output Leakage Current Third State, High Level Applied	I_{OZH}	3021	V_{DD} = 3.6V; V_{SS} = 0V V_{OUT} = V_{DD}	-8	+8	µA
Low Level Output Voltage	V_{OL}	3007	V_{DD} = 3V; V_{SS} = 0V I_{OL} = 4mA	-	400	mV
High Level Output Voltage	V_{OH}	3006	V_{DD} = 3V; V_{SS} = 0V I_{OH} = -4mA	2.4	-	V
Input Capacitance	C_{IN}	3012	f = 1Mhz, ΔV = 3V Note 5	-	50	pF
Data Input/Output Capacitance	$C_{I/O}$	3012	f = 1Mhz, ΔV = 3V Note 5	-	20	pF
Address Access Time	t_{AVQV}	3003	V_{DD} = 3V; V_{SS} = 0V Notes 6, 7	-	40	ns
Enable Access Time	t_{ELQV}	3003	V_{DD} = 3V; V_{SS} = 0V Notes 6, 7	-	40	ns
Output Enable Access Time	t_{GLQV}	3003	V_{DD} = 3V; V_{SS} = 0V Notes 6, 7	-	20	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be V_{IN} = V_{SS} or V_{DD} and outputs not under test shall be open.
2. Functional go-no-go test with the following test conditions:
   - Supply Voltage: V_{DDmin} (3V) and V_{DDmax} (3.6V); V_{SS} = 0V
   - Input Voltages: V_{IL} = V_{SS} ; V_{IH} = V_{DD}
   - Test Patterns:
     - Zeros; Ones; Checkerboard; Checkerboard Invert; March; on the full memory.
     - Bank Decoder on the partial memory.
   - Read Cycle Time, t_{AVAV} = 50ns (see Para. 1.10)
   - Output Voltage Test Levels: V_{OL} < 1.4V; V_{OH} > 1.4V
3. Active supply current shall be measured with one address transition per cycle with a minimum cycle time.
4. No other restrictions on other outputs.
5. Characteristic shall be guaranteed but not tested.
6. Test pattern shall be: Walking One. Output load condition shall be as follows:



7. See Para. 1.10.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +105 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1 Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Active Supply Current – Read Mode	I_{DDR}	±10%	-	128	mA
Active Supply Current – Write Mode	I_{DDW}	±10%	-	228	mA
Stand-by Supply Current 1	I_{SB1}	±8	-	56	mA
Stand-by Supply Current 2	I_{SB2}	±8	-	48	mA
Low Level Input Current	I_{IL}	±0.5	-8	+8	µA
High Level Input Current	I_{IH}	±0.5	-8	+8	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	±0.5	-8	+8	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	±0.5	-8	+8	µA
Low Level Output Voltage	V_{OL}	±100	-	400	mV
High Level Output Voltage	V_{OH}	±0.1	2.4	-	V
Address Access Time	t_{AVQV}	±10%	-	40	ns
Enable Access Time	t_{ELQV}	±10%	-	40	ns
Output Enable Access Time	t_{GLQV}	±10%	-	20	ns

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be as specified for Para. 2.3.1 Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	125 (+0 -5)	°C
Inputs $\overline{CE0}$, $\overline{CE1}$, $\overline{OE}$, $\overline{WE}$, A0 to A16	V_{IN}	V_{GEN} (Note 1)	V
Data Inputs/Outputs DQ00 to DQ31	V_{IN}	V_{GEN} (Note 1)	V
Pulse Voltage	V_{GEN}	V_{SS} to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	125 ±20%	kHz
Positive Supply Voltage	V_{DD}	3.6	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Each input or output is connected to a pulse generator, through an isolation/load resistor (1kΩ to 10kΩ), that provides a suitable test pattern to the component under test.
   Pins with no connection shall be left open (see Para. 1.9)

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.8 HUMIDITY TEST CONDITIONS

Temperature Humidity Bias (THB) shall be performed as specified in the Generic Specification. The following bias conditions shall apply:

Characteristics	Symbols	Bias Conditions	Units
Inputs $\overline{CE0}$, $\overline{CE1}$, $\overline{OE}$, A1 to A15 (odd Nos. only)	V_{IN}	V_{DD} (Note 1)	V
Inputs $\overline{WE}$, A0 to A16 (even Nos. only)	V_{IN}	V_{SS} (Note 1)	V
Data Inputs/Outputs DQ01 to DQ31 (odd Nos. only)	V_{IN}	V_{DD} (Note 1)	V
Data Inputs/Outputs DQ00 to DQ30 (even Nos. only)	V_{IN}	V_{SS} (Note 1)	V
Positive Supply Voltage	V_{DD}	3.6	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Each input or output is connected to V_{DD} or V_{SS}, through an input protection/pull-up/pull-down resistor (1kΩ). Pins with no connection shall be left open (see Para. 1.9).

2.9 TOTAL DOSE RADIATION TESTING

2.9.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Radiation testing shall be performed on 10 samples from the lot of individual MRAM add-on components (see Para. 1.11) used to produce each memory module lot, in accordance with ESCC Basic Specification No. 22900 with low dose rate (window 2: 36rad(Si) to 360rad(Si) per hour).

Unless otherwise specified, the total dose level applied shall be as specified in Para. 1.4.2.

5 samples shall be irradiated with no bias applied; all pins shall be connected to ground.

For the remaining 5 samples, continuous bias shall be applied during irradiation testing as follows:

Characteristics	Symbols	Bias Conditions (Note 1)	Units
Inputs: $\overline{OE}$, A0, A1 to A9	V_{IN}	V_{DD}	V
Inputs: $\overline{CE}$, $\overline{WE}$, A10 to A16	V_{IN}	V_{SS}	V
Data Inputs/Outputs: DQ0, DQ2, DQ4, DQ6	V_{IN}	V_{DD}	V
Data Inputs/Outputs: DQ1, DQ3, DQ5, DQ7	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	3.6	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:

1. Input protection/pull-up/pull-down resistors = 1kΩ to 10kΩ. Pins with no connection shall be left open (see Para. 1.9).

2.9.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the components shall successfully meet the following Electrical Measurements.

Unless otherwise specified, the test methods and conditions shall be the same as specified in Para. 2.3.1 Room Temperature Electrical Measurements.

Characteristics	Symbols	Limits		Units
		Min	Max	
Functional Test 1 (Note 1)	-	-	-	-
Active Supply Current – Read Mode	I_{DDR}	-	25	mA
Active Supply Current – Write Mode	I_{DDW}	-	50	mA
Stand-by Supply Current 1	I_{SB1}	-	7	mA
Stand-by Supply Current 2	I_{SB2}	-	6	mA
Low Level Input Current	I_{IL}	-1	+1	µA
High Level Input Current	I_{IH}	-1	+1	µA
Output Leakage Current Third State, Low Level Applied	I_{OZL}	-1	+1	µA
Output Leakage Current Third State, High Level Applied	I_{OZH}	-1	+1	µA
Low Level Output Voltage	V_{OL}	-	400	mV
High Level Output Voltage	V_{OH}	2.4	-	V
Address Access Time	t_{AVQV}	-	37	ns
Enable Access Time	t_{ELQV}	-	35	ns
Output Enable Access Time	t_{GLQV}	-	15	ns

NOTES:

1. Test Patterns: Zeros; Ones; Checkerboard; Checkerboard Invert; March.

APPENDIX A

AGREED DEVIATIONS FOR 3D-PLUS SA (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 1.11 Add-on Components: Element Evaluation Screening Para. 2.1.1 Deviations from the Generic Specification: Para. 5.2.1 Element Evaluation: Validation of Active Memory Add-on Components	Element evaluation screening of each single homogeneous lot of active memory add-on components shall be performed at memory module level (after assembly of the memory modules) in accordance with 3D-PLUS specification 3DPA-8113.
	Element evaluation lot acceptance of each single homogeneous lot of active memory add-on components shall be performed on samples at add-on component level in accordance with 3D-PLUS specification 3DPE-0380.
Para. 2.9 Total Dose Radiation Testing	Each single homogeneous lot of active memory add-on components shall be subjected to a total dose radiation test on samples at add-on component level in accordance with 3D-PLUS specification 3DPE-0380 with test requirements as specified in Para. 2.9 herein and as follows: • The maximum total dose radiation exposure level shall be 50krad(Si). **NOTE:** The total dose radiation level letter (P) shall remain unchanged (see Para. 1.4.2).

ADDITIONAL DATA - 3D-PLUS SA (F)

(a) Single Event Effects (SEE) Information
These components are susceptible to Single Event Latch-up (SEL) and Single Event Upset (SEU) if operated in a space environment.

Typical performance:
- SEL: Threshold > 85MeV.cm^2 /mg.
- SEU:
  - In Standby Mode: LET Threshold > 85MeV.cm^2 /mg (memory cell SEU immune).
  - In Dynamic Mode (Transient): LET Threshold > 8.3MeV.cm^2 /mg; Saturated Cross Section: 4.004 x10^{-6} cm^2/device.