



**TRANSISTORS, POWER, MOSFET, P-CHANNEL,  
RAD-HARD**

**BASED ON TYPE STRH12P10**

**ESCC Detail Specification No. 5205/029**

Issue 7	October 2020
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(Refer to <https://escies.org> for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
1365	Specification updated to incorporate changes per DCR.

**TABLE OF CONTENTS**

1	GENERAL	5
1.1	SCOPE	5
1.2	APPLICABLE DOCUMENTS	5
1.3	TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS	5
1.4	THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS	5
1.4.1	THE ESCC COMPONENT NUMBER	5
1.4.2	COMPONENT TYPE VARIANTS	5
1.5	MAXIMUM RATINGS	6
1.6	HANDLING PRECAUTIONS	7
1.7	PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION	8
1.7.1	METAL FLANGE MOUNT PACKAGE (TO-257AA) – 3 LEAD	8
1.7.2	DIE	9
1.8	FUNCTIONAL DIAGRAM	10
1.9	MATERIALS AND FINISHES	10
1.9.1	MATERIALS AND FINISHES OF PACKAGED COMPONENTS	10
1.9.2	MATERIALS AND FINISHES OF DIE COMPONENTS	10
2	REQUIREMENTS	10
2.1	GENERAL	10
2.1.1	DEVIATIONS FROM THE GENERIC SPECIFICATION	10
2.1.1.1	DEVIATIONS FROM SCREENING TESTS - CHART F3	10
2.2	WAFER LOT ACCEPTANCE	11
2.3	MARKING	11
2.4	CASE ISOLATION	11
2.5	TERMINAL STRENGTH	11
2.6	ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES	11
2.6.1	ROOM TEMPERATURE ELECTRICAL MEASUREMENTS	11
2.6.2	HIGH AND LOW TEMPERATURES ELECTRICAL MEASUREMENTS	12
2.6.3	NOTES TO ROOM, HIGH AND LOW TEMPERATURES ELECTRICAL MEASUREMENTS	13
2.7	PARAMETER DRIFT VALUES	13
2.8	INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS	14
2.9	HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS	14
2.10	HIGH TEMPERATURE FORWARD BIAS BURN-IN CONDITIONS	14
2.11	OPERATING LIFE CONDITIONS	15
2.12	TOTAL DOSE RADIATION TESTING	15
2.12.1	BIAS CONDITIONS AND TOTAL DOSE LEVEL FOR TOTAL DOSE RADIATION TESTING	15
2.12.2	ELECTRICAL MEASUREMENTS FOR TOTAL DOSE RADIATION TESTING	16
	APPENDIX 'A'	17

## 1 GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

### 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. [5000](#)
- (b) [MIL-STD-750](#), Test Methods and Procedures for Semiconductor Devices

### 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. [21300](#) shall apply.

### 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

#### 1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520502901R

- Detail Specification Reference: 5205029
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: R (as required)

#### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead Material and Finish	Weight max g	Total Dose Radiation Level Letter
01	STRH12P10	TO-257AA	S14	5	R [100krad(Si)]
02	STRH12P10	TO-257AA	S4	5	R [100krad(Si)]
03	STRH12P10	Die	N/A	N/A	R [100krad(Si)]

The lead material and finish shall be in accordance with the requirements of ESCC Basic Specification No. [23500](#).

Total dose radiation level letters are defined in ESCC Basic Specification No. [22900](#). If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

### 1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Drain-Source Voltage	V <sub>DS</sub>	-100	V	Over T <sub>op</sub> , V <sub>GS</sub> = 0V Note 2
Gate-Source Voltage	V <sub>GS</sub>	±18	V	Over T <sub>op</sub>
Drain Current	I <sub>DS</sub>	-12	A	Continuous, At T <sub>case</sub> ≤ +25°C Note 1
		-7.5	A	Continuous, At T <sub>case</sub> > +100°C Note 1
Drain Current (Pulsed)	I <sub>DM</sub>	-48	A	Note 2
Power Dissipation	P <sub>tot</sub>	75	W	At T <sub>case</sub> ≤ +25°C Note 1
Avalanche Energy (Single Pulse)	E <sub>AS</sub>	597 112	mJ	V <sub>DS</sub> = -50V, I <sub>A</sub> = -6A T <sub>j</sub> = +25 ±3°C T <sub>j</sub> = +110 (+0 -5)°C
Avalanche Energy (Repetitive Pulse)	E <sub>AR</sub>	17 5.5	mJ	V <sub>DS</sub> = -50V, I <sub>A</sub> = -6A, f = 10kHz, Duty Cycle = 50% T <sub>j</sub> = +25 ±3°C T <sub>j</sub> = +110 (+0 -5)°C
Operating Temperature Range	T <sub>op</sub>	-55 to +150	°C	Note 3
Junction Temperature	T <sub>j</sub>	+150	°C	
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C	Note 3
Soldering Temperature	T <sub>sol</sub>	+260	°C	Note 4
Thermal Resistance, Junction-to-Heat Sink	R <sub>th(j-s)</sub>	0.2	°C/W	Note 5
Thermal Resistance, Junction-to-Ambient	R <sub>th(j-a)</sub>	62.5	°C/W	Note 2

#### **NOTES:**

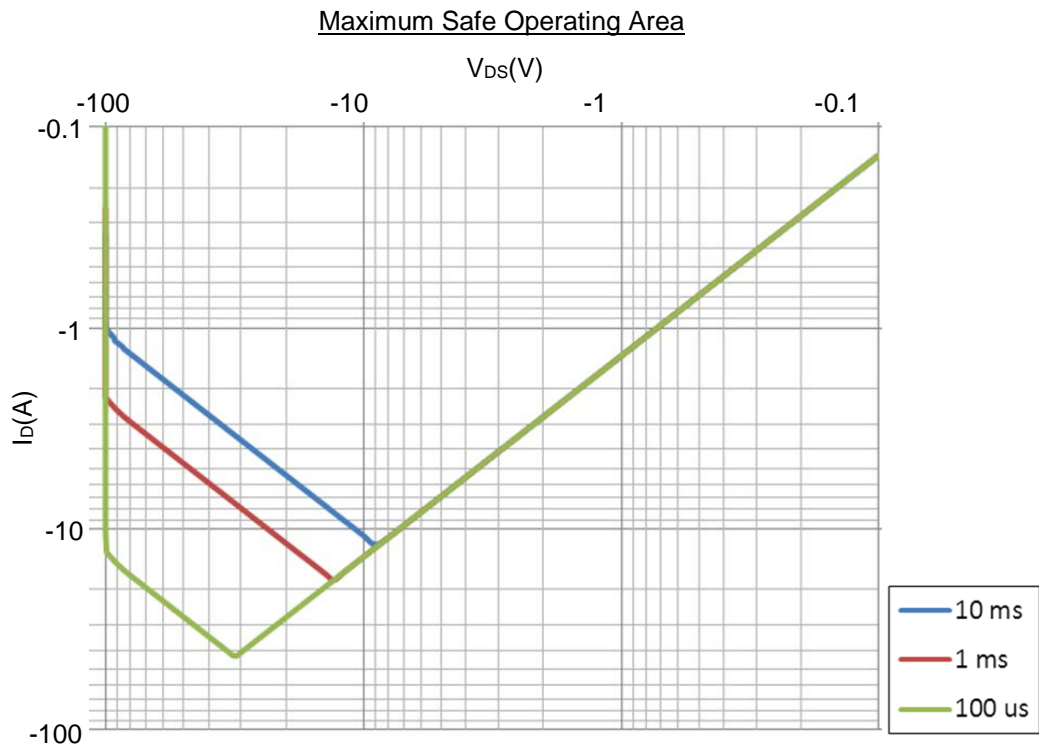
- I<sub>DS</sub> and P<sub>tot</sub> ratings are in accordance with R<sub>th(j-s)</sub>. The maximum theoretical I<sub>D</sub> limit at T<sub>case</sub> > +25°C can be obtained by using the following formula (I<sub>D</sub> is limited by the package and device construction):

$$I_D = \sqrt{\frac{T_j(max) - T_{case}}{R_{th(j-s)} \times (r_{DS(on)} \text{ at } T_j(max))}}$$

Where r<sub>DS(on)</sub> at T<sub>j</sub>(max) = 550mΩ.

For T<sub>case</sub> > +25°C, the power dissipation derates linearly to 0W at T<sub>case</sub> = +150°C.

- Safe Operating Area applies as follows:



- For Variants with hot solder dip lead finish all testing and any handling performed at  $T_{amb} > +125^{\circ}\text{C}$  shall be carried out in a 100% inert atmosphere.
- Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
- Package is mounted on an infinite heatsink.

#### 1.6 HANDLING PRECAUTIONS

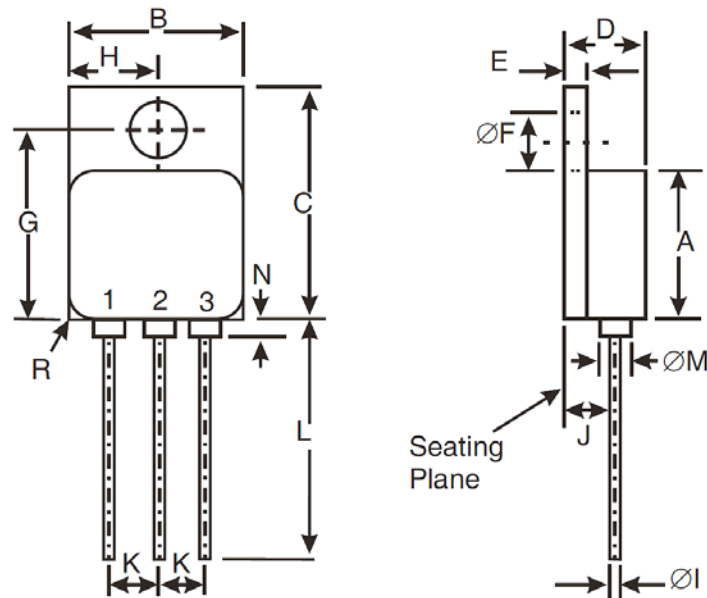
These components are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. [23800](#) with a Minimum Critical Path Failure Voltage of 1500 Volts.

The TO-257AA package contains Beryllium Oxide (BeO) and therefore it must not be ground, machined, sandblasted or subjected to any mechanical operation which will produce dust. The case must not be subjected to any chemical process (e.g. etching) which will produce fumes.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Metal Flange Mount Package (TO-257AA) – 3 Lead

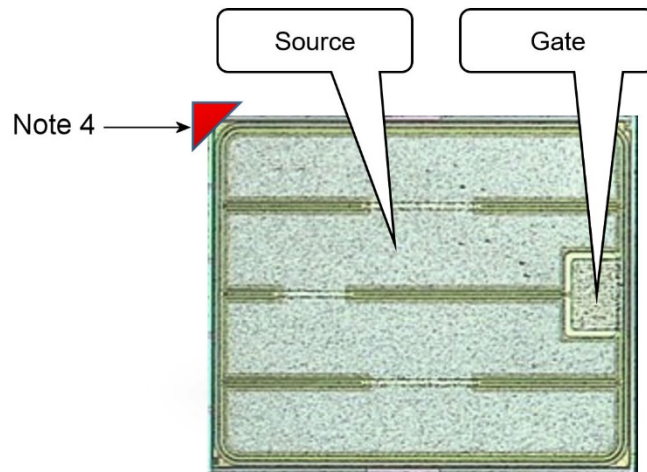


Symbols	Dimensions mm		Notes
	Min	Max	
A	10.41	10.67	
B	10.41	10.67	
C	16.51	16.76	
D	4.7	5.33	
E	0.89	1.14	
ØF	3.56	3.81	
G	13.39	13.64	
H	5.13	5.38	
ØI	0.64	0.89	2
J	2.92	3.16	
K	2.41	2.67	
L	15.24	16.51	
ØM	2.29 Typical		2
N	-	0.71	2
R	1.65 Typical		3

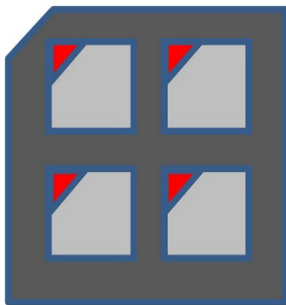
**NOTES:**

1. The terminal identification is specified by the components geometry. See Para. 1.8 Functional Diagram for the terminal connections.
2. Applies to all leads.
3. Radius of body corner, 4 places.



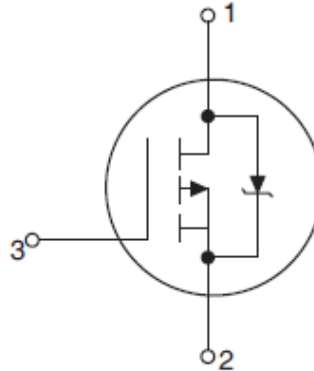
1.7.2 Die**NOTES:**

1. Die materials and dimensions:
  - Die substrate: Silicon
  - Die length: 2922  $\mu\text{m}$
  - Die width: 2440  $\mu\text{m}$
  - Die thickness: 280  $\pm 20\mu\text{m}$
  - Top glassivation: Nitride with thickness 1  $\mu\text{m}$
  - Top metallisation: Al/Si with thickness 4.5  $\mu\text{m}$
  - Backside metallisation: Cr/Ni/Ag with thickness 620 nm
  - Gate pad dimensions: 344  $\times$  460  $\mu\text{m}$
  - Source bondable area: approx. 4.5 mm<sup>2</sup> (N.B. bonds shall not touch or overlap the fingers which are passivated areas).
2. Terminal identification is indicated by the die mask.
3. Bias details: backside contact = Drain
4. Die packaging orientation: The die corner highlighted with the red triangle is positioned in the waffle pack as follows:



## 1.8 FUNCTIONAL DIAGRAM

Terminal 1: Drain  
Terminal 2: Source  
Terminal 3: Gate



### **NOTES:**

1. For TO-257AA, the case is not connected to any lead.
2. For Die Components, the terminal numbering is not applicable.

## 1.9 MATERIALS AND FINISHES

### 1.9.1 Materials and Finishes of Packaged Components

For Variants 01 and 02, the materials and finishes shall be as follows:

- (a) Case  
The case shall be hermetically sealed and have a metal body. The leads pass through ceramic eyelets brazed into the frame and the lid shall be welded.
- (b) Leads  
As specified in Para. 1.4.2, Component Type Variants.

### 1.9.2 Materials and Finishes of Die Components

For Variant 03, the materials and finishes shall be as specified in Para. 1.7.2.

## 2 REQUIREMENTS

### 2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

#### 2.1.1 Deviations from the Generic Specification

##### 2.1.1.1 *Deviations from Screening Tests - Chart F3*

- (a) Verification of Safe Operating Area  
The Safe Operating Area shall be verified by performing the  $\Delta V_{SD}$  test specified in Para. 2.6.1 Room Temperature Electrical Measurements (Thermal Resistance, Junction-to-Heat Sink).
- (b) A High Temperature Forward Bias test shall be performed instead of Power Burn-in.

2.2 WAFER LOT ACCEPTANCE

A SEM inspection shall be performed as specified in the ESCC Generic Specification.

2.3 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component or its primary package shall be:

- (a) The ESCC Qualified Component symbol (for ESCC qualified components only).
- (b) The ESCC Component Number (see Para. 1.4.1).
- (c) Traceability information.
- (d) Warning sign for Beryllium Oxide (TO-257AA only).

2.4 CASE ISOLATION

Case Isolation shall be performed as specified in the ESCC Generic Specification and as follows:

- Test Conditions:
  - Test voltage: 500Vdc
  - Duration of application of test voltage: 1s
  - Points of application of test voltage: between case metal tab and all terminals connected together.
  - Maximum leakage current: 10nA

2.5 TERMINAL STRENGTH

The test conditions for terminal strength, tested as specified in the ESCC Generic Specification, shall be as follows:

- For TO-257AA, Test Condition: A, tension, with an applied force of 10N for a duration of 10s.

2.6 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given after the tables in Para. 2.6.3.

2.6.1 Room Temperature Electrical Measurements

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	3407	$V_{GS} = 0V, I_D = -1mA$ Bias condition C	-100	-	V
Gate-to-Source Leakage Current 1	$I_{GSS1}$	3411	$V_{GS} = -16V, V_{DS} = 0V$ Bias condition C	-	-100	nA
Gate-to-Source Leakage Current 2	$I_{GSS2}$	3411	$V_{GS} = 16V, V_{DS} = 0V$ Bias condition C	100	-	nA
Drain Current	$I_{DSS}$	3413	$V_{DS} = -80V, V_{GS} = 0V$ Bias condition C	-	-10	$\mu A$
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -1mA$	-2	-4.5	V

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Static Drain-to-Source On Resistance	$r_{DS(on)}$	3421	$V_{GS} = -12V, I_D = -12A$ Note 1	-	0.3	$\Omega$
Source-to-Drain Diode Forward Voltage	$V_{SD}$	4011	$V_{GS} = 0V, I_{SD} = -12A$ Note 1	-	-1.5	V
Thermal Resistance, Junction-to-Heat Sink	$R_{th(j-s)}$	3161	Note 2	-	0.2	$^{\circ}C/W$
Input Capacitance	$C_{iss}$	3431	$V_{GS} = 0V, V_{DS} = -25V$ $f = 1MHz$	940	1410	pF
Output Capacitance	$C_{oss}$	3453		135	205	pF
Reverse Transfer Capacitance	$C_{rss}$	3433		55	85	pF
Total Gate Charge	$Q_g$	3471	$V_{GS} = -12V, V_{DS} = -50V$ $I_D = -12A$	32	48	nC
Gate-to-Source Charge	$Q_{gs}$			3.5	6.5	nC
Gate-to-Drain Charge	$Q_{gd}$			7	13	nC
Turn-on Delay Time	$t_{d(on)}$	3472	$V_{GS} = -12V, V_{DS} = -50V$ $I_D = -6A, R_G = 4.7\Omega$	5	13	ns
Rise Time	$t_r$			7	31	ns
Turn-off Delay Time	$t_{d(off)}$			18	42	ns
Fall Time	$t_f$			3.5	10.5	ns
Reverse Recovery Time	$t_{rr}$	3473	$V_{DS} = -60V, I_{SD} = -12A$ $di/dt = 40A/\mu s$ $T_j = +25 \pm 3^{\circ}C$	178	258	ns

2.6.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 3	Limits		Units
				Min	Max	
Gate-to-Source Leakage Current 1	$I_{GSS1}$	3411	$V_{GS} = -16V,$ $V_{DS} = 0V$ Bias condition C $T_{case} = +125 (+0-5)^{\circ}C$	-	-200	nA
Gate-to-Source Leakage Current 2	$I_{GSS2}$	3411	$V_{GS} = 16V,$ $V_{DS} = 0V$ Bias condition C $T_{case} = +125 (+0-5)^{\circ}C$	200	-	nA
Drain Current	$I_{DSS}$	3413	$V_{DS} = -80V,$ $V_{GS} = 0V$ Bias condition C $T_{case} = +125 (+0-5)^{\circ}C$	-	-100	$\mu A$
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -1mA$ $T_{case} = +125 (+0-5)^{\circ}C$	-1.6	-3.8	V
			$V_{DS} \geq V_{GS}$ $I_D = -1mA$ $T_{case} = -55 (+5-0)^{\circ}C$	-2.2	-5.2	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	3421	$V_{GS} = -12V, I_D = -12A$ $T_{case} = +125 (+0-5)^{\circ}C$ Note 1	-	0.6	$\Omega$

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 3	Limits		Units
				Min	Max	
Source-to-Drain Diode Forward Voltage	V <sub>SD</sub>	4011	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -12A T <sub>case</sub> = +125 (+0-5)°C Note 1	-	-1.25	V

2.6.3 Notes to Room, High and Low Temperatures Electrical Measurements

- Pulsed measurement: Pulse Width ≤ 680µs, Duty Cycle ≤ 2%.
- The R<sub>th(j-s)</sub> limit is guaranteed by performing a ΔV<sub>SD</sub> (go-no-go) test. The following test conditions and limits shall apply:
  - V<sub>DS</sub> = -7V
  - I<sub>D</sub> = -5.6A
  - I<sub>cal</sub> = -7mA
  - t<sub>pulse</sub> = 20ms
  - t<sub>cal</sub> = 50µs
  - V<sub>SD</sub> = -60mV minimum, -130mV maximum
- Read and record measurements shall be performed on a sample of 5 components with 0 failures allowed. Alternatively a 100% inspection may be performed.

2.7 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T<sub>amb</sub> = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.6.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Gate-to-Source Leakage Current 1	I <sub>GSS1</sub>	±50 or (1) ±100%	-	-100	nA
Gate-to-Source Leakage Current 2	I <sub>GSS2</sub>	±50 or (1) ±100%	100	-	nA
Drain Current	I <sub>DSS</sub>	±4 or (1) ±100%	-	-10	µA
Gate-to-Source Threshold Voltage	V <sub>GS(th)</sub>	±5%	-2	-4.5	V
Static Drain-to-Source On Resistance	r <sub>DS(on)</sub>	±10%	-	0.3	Ω

**NOTES:**

- Whichever is the greater referred to the initial value.

**2.8 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS**

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.6.1, Room Temperature Electrical Measurements.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Drain Current	$I_{DSS}$	-	-10	$\mu A$
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	-2	-4.5	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	-	0.3	$\Omega$

**2.9 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS**

HTRB Burn-in shall be performed in accordance with [MIL-STD-750, Test Method 1042](#), Test Condition A with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+150 (+0-5)	$^{\circ}C$
Drain-to-Source Voltage	$V_{DS}$	-80	V
Gate-to-Source Voltage	$V_{GS}$	0	V
Duration	t	240 minimum	Hours

**2.10 HIGH TEMPERATURE FORWARD BIAS BURN-IN CONDITIONS**

HTFB Burn-in shall be performed in accordance with [MIL-STD-750, Test Method 1042](#), Test Condition B with the following conditions:

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+150 (+0-5)	$^{\circ}C$
Drain-to-Source Voltage	$V_{DS}$	0	V
Gate-to-Source Voltage	$V_{GS}$	-16	V
Duration	t	48 minimum	Hours

2.11 OPERATING LIFE CONDITIONS

Operating Life shall consist of High Temperature Reverse Bias in accordance with [MIL-STD-750, Test Method 1042](#), Test Condition A, followed by High Temperature Forward Bias in accordance with [MIL-STD-750, Test Method 1042](#), Test Condition B. The test conditions are as follows:

High Temperature Reverse Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T <sub>amb</sub>	+150 (+0-5)	°C
Drain-to-Source Voltage	V <sub>DS</sub>	-80	V
Gate-to-Source Voltage	V <sub>GS</sub>	0	V
Duration	t	1000 minimum	Hours

High Temperature Forward Bias Conditions

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T <sub>amb</sub>	+150 (+0-5)	°C
Drain-to-Source Voltage	V <sub>DS</sub>	0	V
Gate-to-Source Voltage	V <sub>GS</sub>	-16	V
Duration	t	1000 minimum	Hours

2.12 TOTAL DOSE RADIATION TESTING

All lots shall be irradiated in accordance with ESCC Basic Specification No. [22900](#), standard dose rate (window 1: 3.6krad(Si) to 36krad(Si) per hour).

2.12.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

The following bias condition (worst-case) shall be used for Total Dose Radiation Testing at T<sub>amb</sub> = +22 ±3°C:

With V<sub>GS</sub> bias = -15V and V<sub>DS</sub> = 0V during irradiation.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

2.12.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified in Para. 2.6.1.

Unless otherwise stated the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

Unless otherwise specified the test methods and test conditions shall be as per the corresponding test defined in Para. 2.6.1, Room Temperature Electrical Measurements.

The parameters to be measured during irradiation testing, on completion of irradiation testing, after 24 hours anneal at Room Temperature and after 168 hours anneal at  $+100 \pm 3^{\circ}C$  are shown below.

Characteristics	Symbols	Limits			Units
		Drift Values $\Delta$	Absolute		
			Min	Max	
Drain-to-Source Voltage Note 1	$V_{DSS}$	+5% Note 2	N/A		V
Gate-to-Source Leakage Current 1	$I_{GSS1}$	-1.5	-	-100	nA
Gate-to-Source Leakage Current 2	$I_{GSS2}$	+1.5	100	-	nA
Drain Current	$I_{DSS}$	-1	-	-10	$\mu A$
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	+150%	-2	-4.5	V
Static Drain-to-Source On Resistance	$r_{DS(on)}$	-4% / +35%	-	0.3	$\Omega$
Source-to-Drain Diode Forward Voltage	$V_{SD}$	$\pm 5\%$	-	-1.5	V

**NOTES:**

1. Drain-to-Source Voltage measurements shall be made in accordance with [MIL-STD-750, Test Method 3405](#), with  $V_{GS} = 0V$  and  $I_D = -1mA$ .
2. Referred to an initial Drain-to-Source Voltage measurement made prior to the commencement of Total Dose Radiation Testing.



**APPENDIX 'A'**  
**AGREED DEVIATIONS FOR STMICROELECTRONICS (F)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.1.1, Deviations from the Generic Specification: Para. 8, Test Methods and Procedures	For qualification and qualification maintenance, or procurement of qualified or unqualified components, the following replacement test method specifications shall be used instead of the following ESCC Basic Specifications: <ul style="list-style-type: none"> <li>• No. 20500, External Visual Inspection: replaced by <a href="#">MIL-STD-750 Test Method 2071</a>.</li> <li>• No. 20900, Radiographic Inspection of Electronic Components: replaced by <a href="#">MIL-STD-750 Test Method 2076</a>.</li> <li>• No. 21400, Scanning Electron Microscope Inspection of Semiconductor Dice: replaced by <a href="#">MIL-STD-750 Test Method 2077</a>.</li> </ul>
Para. 2.1.1.1, Deviations from the Generic Specification: Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.
Para. 2.6.1, Room Temperature Electrical Measurements	The AC characteristics $C_{iss}$ , $C_{oss}$ , $C_{rss}$ , $Q_g$ , $Q_{gs}$ , $Q_{gd}$ , $t_{d(on)}$ , $t_r$ , $t_{d(off)}$ , $t_f$ and $t_{rr}$ may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot in accordance with STMicroelectronics "Acceptation wafers" internal procedure as specified in the PID, which includes AC ( $C_{iss}$ , $C_{oss}$ , $C_{rss}$ , $Q_g$ , $Q_{gs}$ , $Q_{gd}$ , $t_{d(on)}$ , $t_r$ , $t_{d(off)}$ , $t_f$ and $t_{rr}$ ) characteristic measurements per the Detail Specification.  A summary of the pilot lot testing shall be provided if required by the Purchase Order.

**ADDITIONAL DATA - STMICROELECTRONICS (F)**

**NB:** Heavy ions characterisation has been carried out on STRH40P10 devices. The STRH12P10 is based on the same technology and the same epitaxy. The results obtained on the STRH40P10 are considered transposable to the STRH12P10.

- (a) Derating for Space Application  
 These components are susceptible to Single Event Gate Rupture if operated in a space environment unless the following derating is applied:

$$V_{DS} \geq -60V \text{ when } V_{GS} = 2V$$

$$V_{DS} \geq -20V \text{ when } V_{GS} = 15V$$

The derating for space applications was originally obtained on STRH40P10 devices under the following test conditions. The testing was performed in a vacuum:

For  $V_{GS} = 2V$ ; location = RADEF (Jyväskylä, Finland):

Ion used = Kr

$$LET = 32MeV/(mg/cm^2)$$

$$\text{Energy} = 768MeV$$

$$\text{Range} = 94\mu m$$

For  $V_{GS} = 15V$ ; location = UCL (Louvain-la-Neuve, Belgium):

Ion used = Kr

LET =  $32.4MeV/(mg/cm^2)$

Energy = 756MeV

Range =  $92\mu m$

